TestConX™

Tutorial

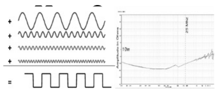
DoubleTree by Hilton
Mesa, Arizona
March 1-4, 2026

Signal Integrity & Power Integrity: Design, Modeling, Simulation, & Validation from an ATE User's Perspective

Noel Del Rio
Signal and Power Integrity Design

TestConX™

Mesa, Arizona ● March 1–4, 2026

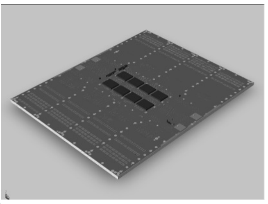


Noel Del Rio has over twenty-four Years of signal integrity (SI) and power integrity (PI) design, modeling, simulation and validation for ATE Load Boards and Application Boards

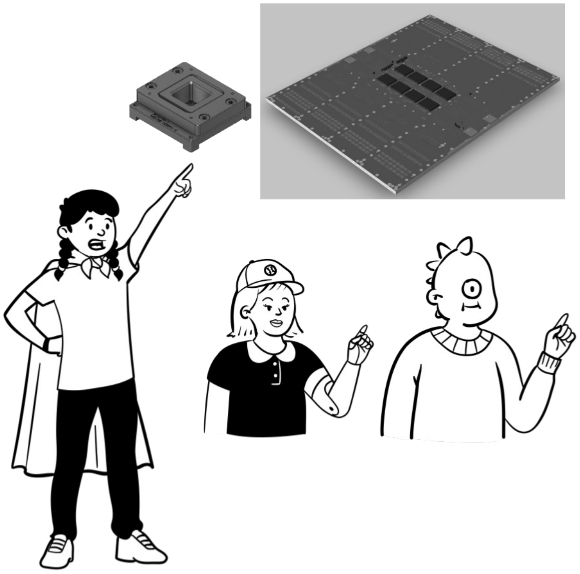
Device applications that he has worked on include CPUs, Network Processors, ATE Timing Generators, 5G Baseband, Mixed Signal, and Ultra Low Jitter Clock devices.

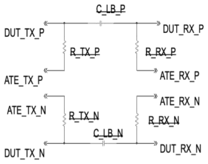
Noel has held important engineering positions at Intel, Teradyne, Silicon Labs, and NXP. He received as MS BSECE from Don Bosco Technical College in the Philippines.

- **Signal Integrity (Frequency Domain)**
  - Concept of Filter and Filter Design on ATE Test Hardware
  - Transmission Line Segment Integration
  - Intellectual Property Sensitivity (Multi-IP, Complex Performance Requirements, Advance HW Structures & Technologies, Multi-IP Sources)
  - Modeling, Simulation, Validation, **Transmission Line Segment Integration**
- **Power Integrity (Frequency Domain)**
  - Multi-Site ATE Load Board vs Single Site Application Board
  - Power Filter Design
  - Low Voltage high Current IPs
  - DC Resistance table, Power Delivery impedance profile (Frequency Domain)
  - Multi-IP & multi-die with varying Noise Floor Sensitivities
  - Sound Electrical Engineering Practices on stack-up and routing design
- **AI Design Opportunities for SI and PI**
  - Circuit Optimization and Integration
  - IP Protection

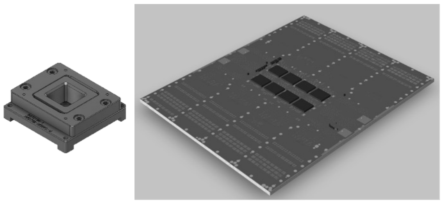


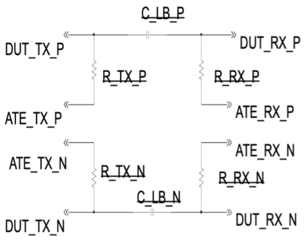
- **Why this is important?**
  - We are in the era of applications using different intellectual property (IP), different die geometries, and with more than one known good die (KGD) in a single a single package. Business units exercise the option of integrating different IPs from different IP providers to achieve the desired performance, functional technology, and cost as they are no longer limited to in-house IP. This creates the need to merge IPs with differing speed and power performance requirements. Test and product engineers are tasked with the delicate integration of complex devices under test (DUT), interposers, printed circuit boards, and support circuits. Along with the challenge of IP protection and security.
- **Who should be interested?**
  - Test and product engineers involved with or work on complex DUT and associated hardware
  - Hardware providers such as interposers (e.g. test socket), printed circuit board designers, and support board circuit providers.
  - Providers of test and measurement such as Automated Test Equipment, Vector Network Analyzers, etc.





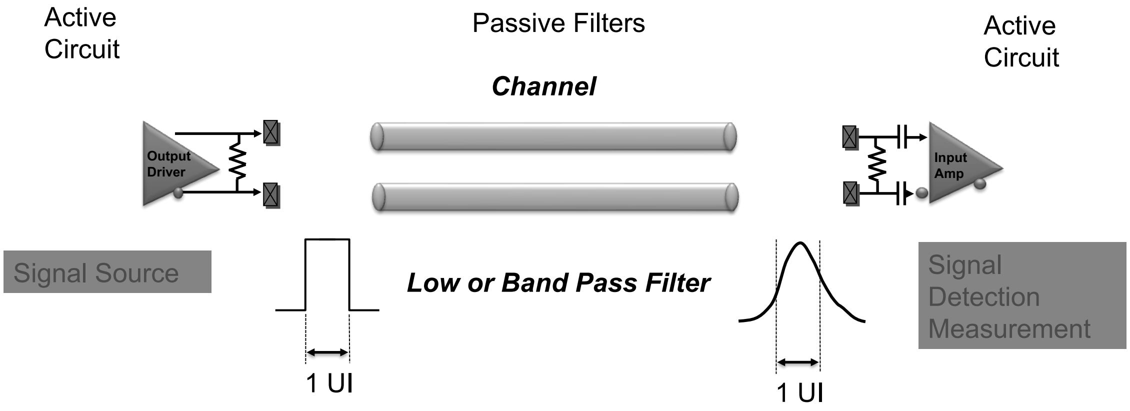
WHAT'S WITH ATE-HARDWARE ON SIGNAL & POWER INTEGRITY





INCAPABLE OF EXPLAINING ITSELF

AT FAULT BY DEFAULT



Active Circuit

Passive Filters

Channel

Active Circuit

Signal Source

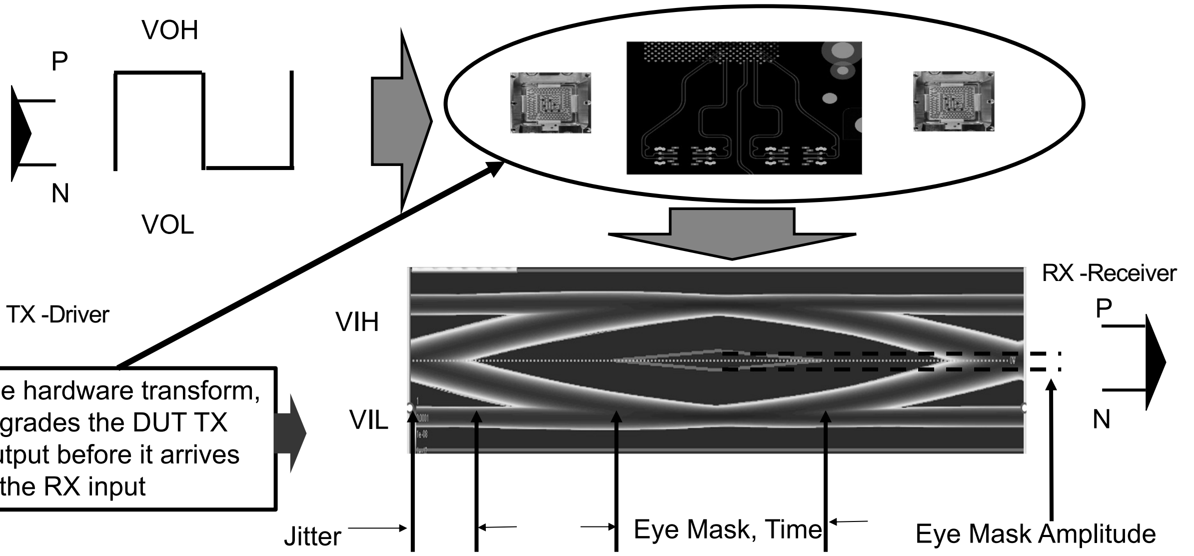
Low or Band Pass Filter

Signal Detection Measurement

1 UI

1 UI

ATE Loop Back Test



VOH

P

N

VOL

TX -Driver

The hardware transform, degrades the DUT TX Output before it arrives at the RX input

VIH

VIL

RX -Receiver

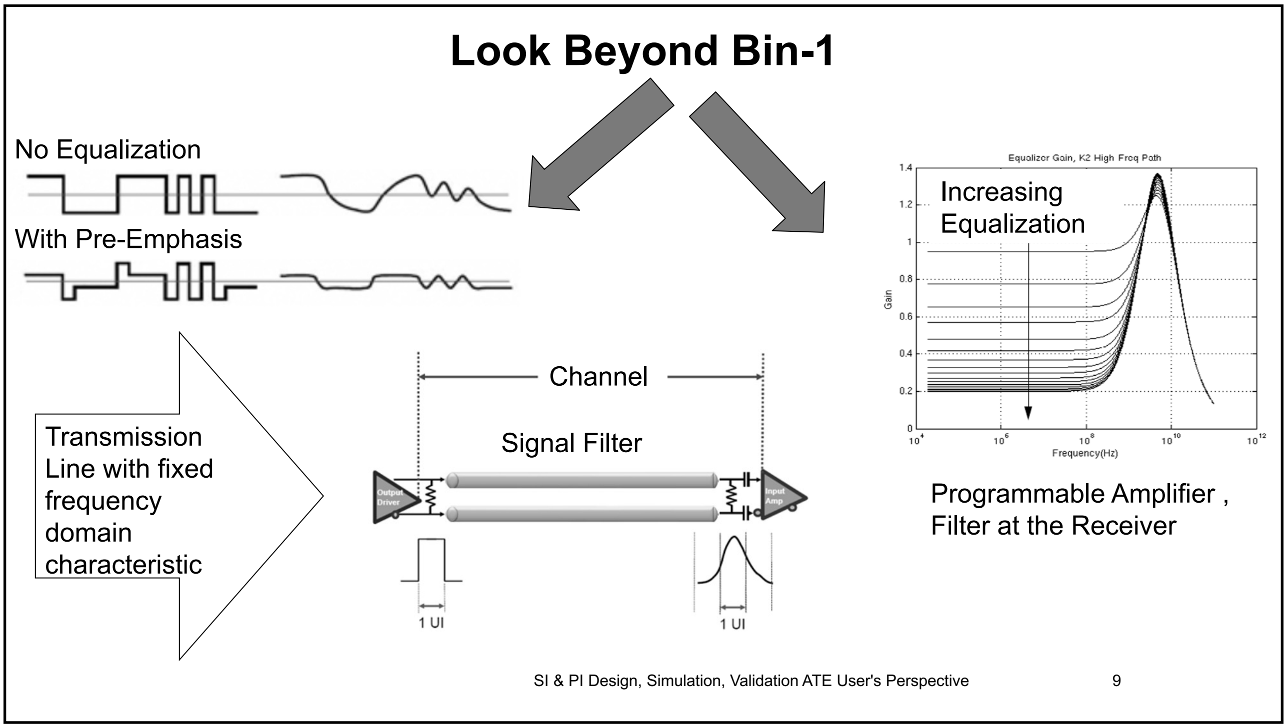
P

N

Jitter

Eye Mask, Time

Eye Mask Amplitude



Look Beyond Bin-1

No Equalization

With Pre-Emphasis

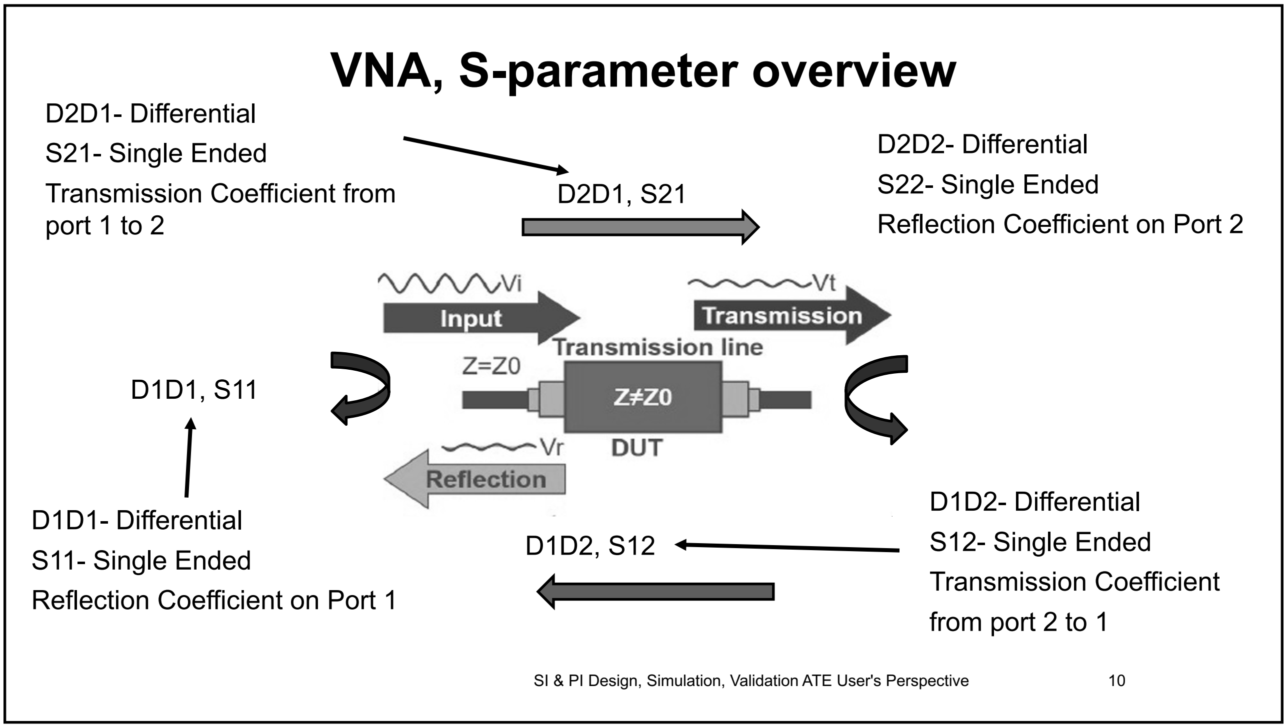
Transmission Line with fixed frequency domain characteristic

Channel

Signal Filter

Increasing Equalization

Programmable Amplifier , Filter at the Receiver



VNA, S-parameter overview

D2D1- Differential
S21- Single Ended
Transmission Coefficient from port 1 to 2

D2D1, S21

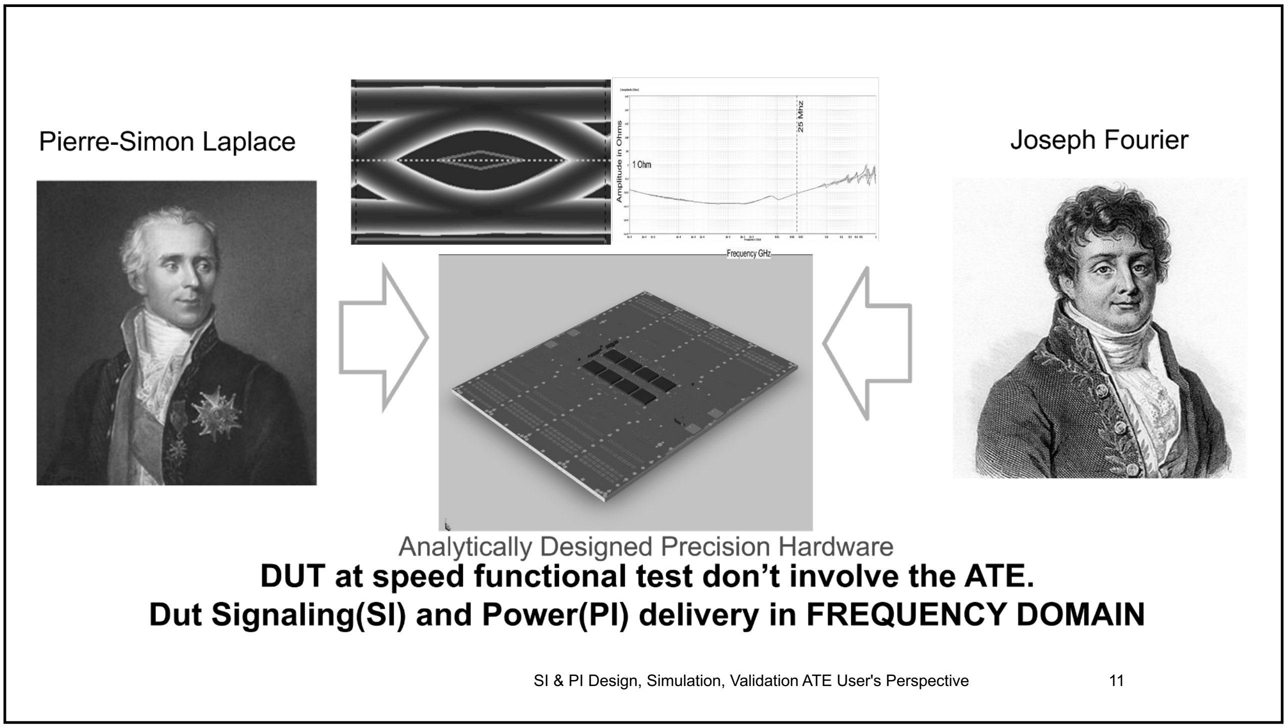
D2D2- Differential
S22- Single Ended
Reflection Coefficient on Port 2

D1D1, S11

D1D1- Differential
S11- Single Ended
Reflection Coefficient on Port 1

D1D2, S12

D1D2- Differential
S12- Single Ended
Transmission Coefficient from port 2 to 1

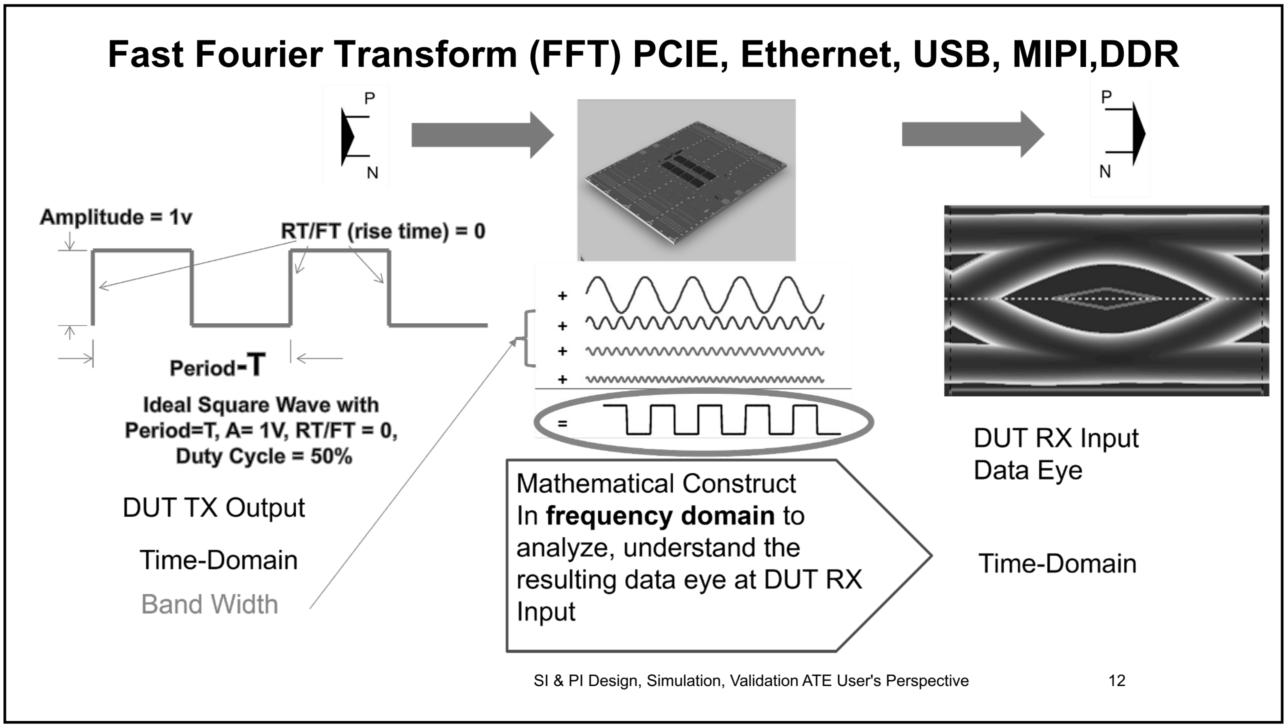


Pierre-Simon Laplace

Joseph Fourier

Analytically Designed Precision Hardware

DUT at speed functional test don't involve the ATE.
Dut Signaling(SI) and Power(PI) delivery in FREQUENCY DOMAIN



Fast Fourier Transform (FFT) PCIE, Ethernet, USB, MIPI,DDR

Amplitude = 1v

RT/FT (rise time) = 0

Period-T

Ideal Square Wave with
Period=T, A= 1V, RT/FT = 0,
Duty Cycle = 50%

DUT TX Output

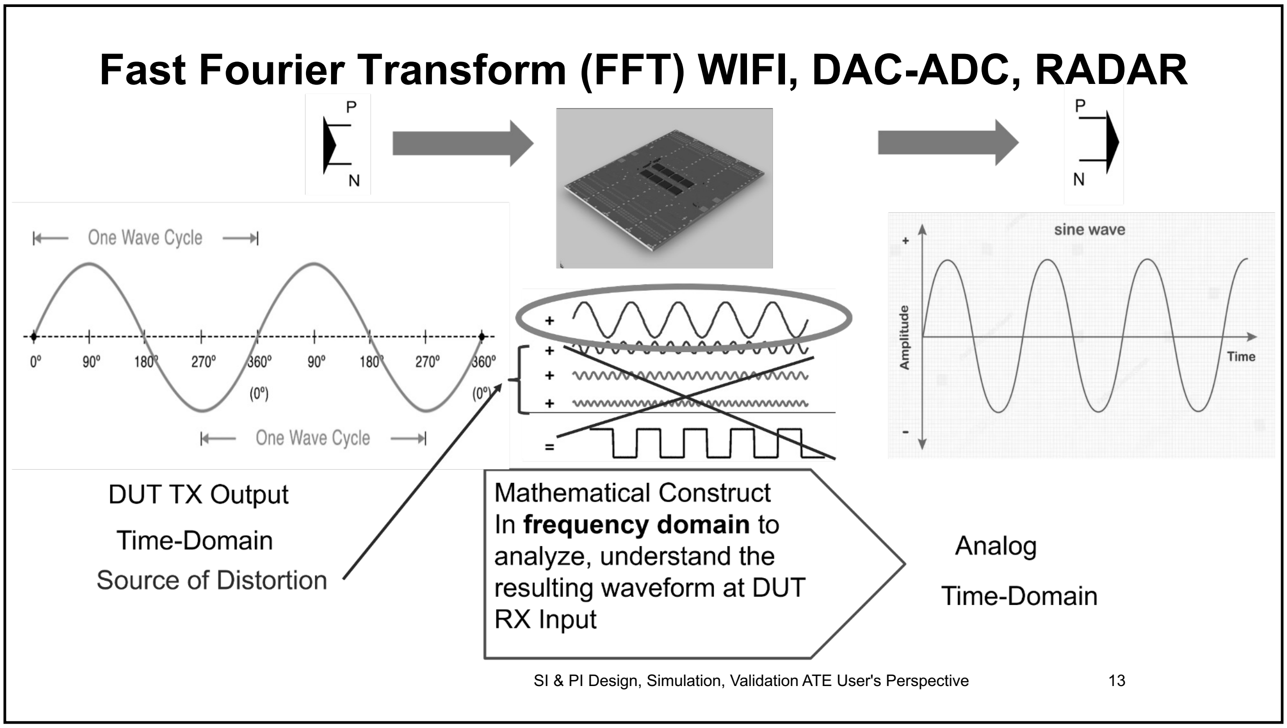
Time-Domain

Band Width

Mathematical Construct
In **frequency domain** to analyze, understand the resulting data eye at DUT RX Input

DUT RX Input
Data Eye

Time-Domain



Fast Fourier Transform (FFT) WIFI, DAC-ADC, RADAR

DUT TX Output

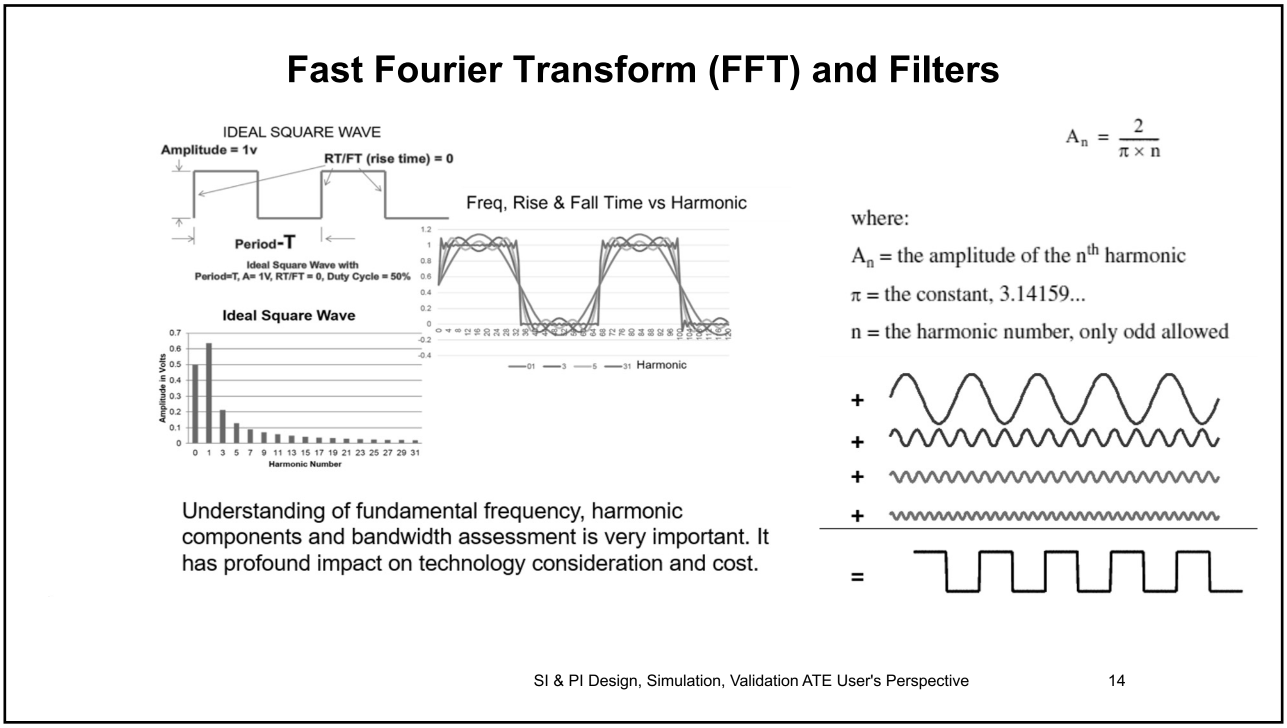
Time-Domain

Source of Distortion

Mathematical Construct
In **frequency domain** to analyze, understand the resulting waveform at DUT RX Input

Analog

Time-Domain



Fast Fourier Transform (FFT) and Filters

$$A_n = \frac{2}{\pi \times n}$$

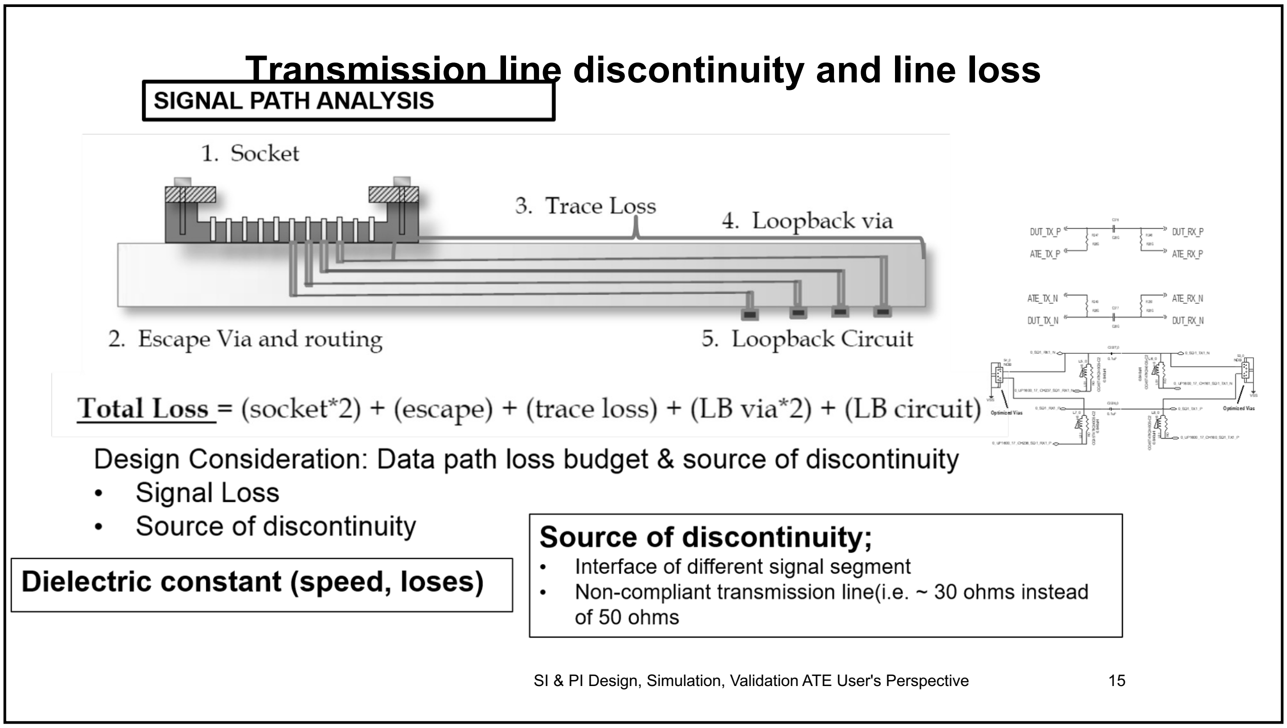
where:

A_n = the amplitude of the n^{th} harmonic

π = the constant, 3.14159...

n = the harmonic number, only odd allowed

Understanding of fundamental frequency, harmonic components and bandwidth assessment is very important. It has profound impact on technology consideration and cost.



Transmission line discontinuity and line loss

SIGNAL PATH ANALYSIS

Total Loss = (socket*2) + (escape) + (trace loss) + (LB via*2) + (LB circuit)

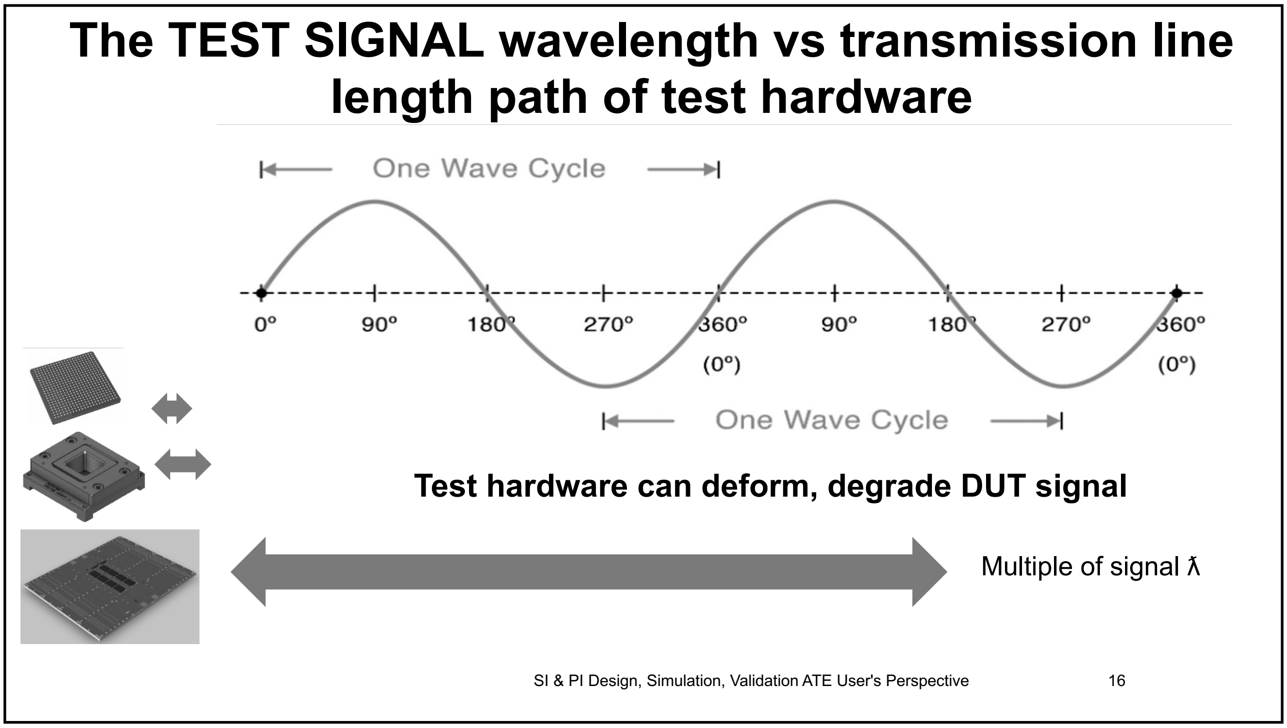
Design Consideration: Data path loss budget & source of discontinuity

- Signal Loss
- Source of discontinuity

Dielectric constant (speed, loses)

Source of discontinuity;

- Interface of different signal segment
- Non-compliant transmission line(i.e. ~ 30 ohms instead of 50 ohms

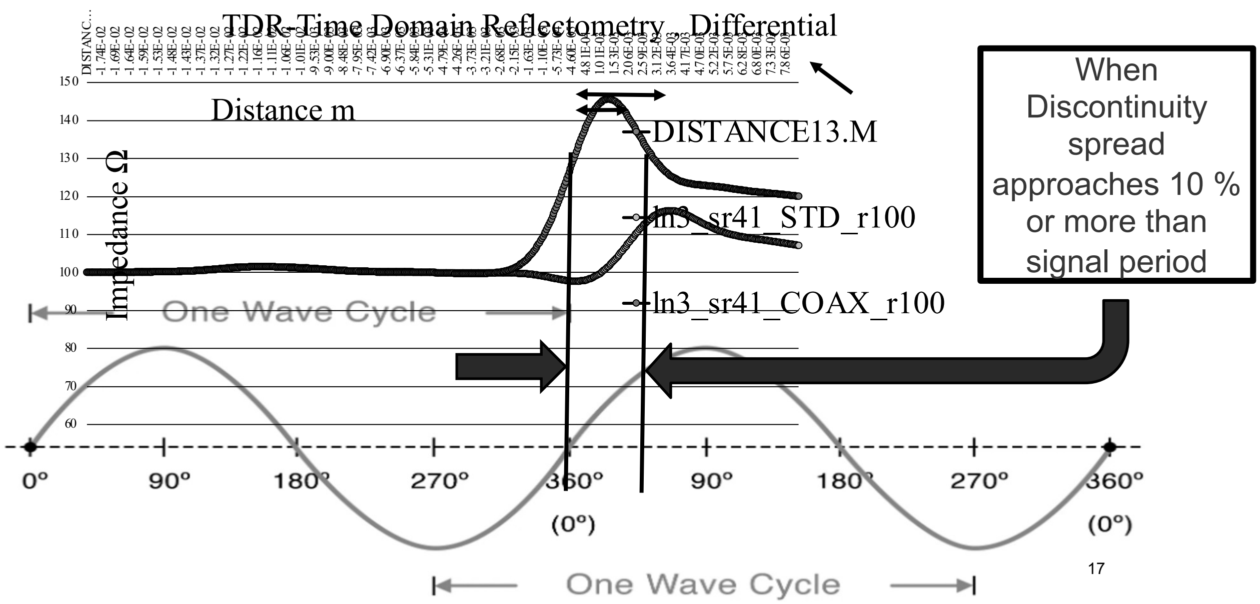


The TEST SIGNAL wavelength vs transmission line length path of test hardware

Test hardware can deform, degrade DUT signal

Multiple of signal ƛ

Impedance Anomalies- Discontinuities , When it matters ?

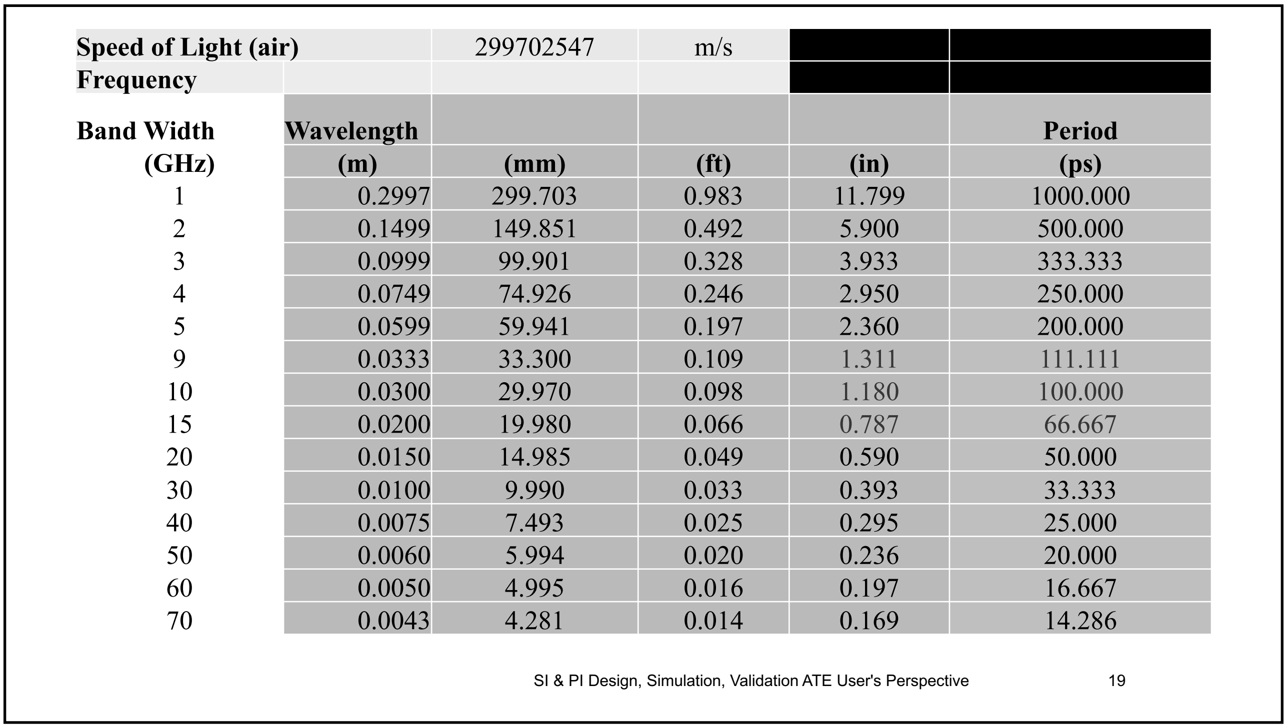


When Discontinuity spread approaches 10 % or more than signal period

Short wavelength signals to test hardware signal path physical dimension

IP Type	Model	Data Rate Gbps	ƛ (inches)	Period (ps)	Tr (ps)
PCIE	T	16	1.475	125.000	43.750
DDR	T	8	2.950	250.000	87.500
Ethernet	I/A	16	1.475	125.000	43.750
PCIE	I/A	10,16, 2.5	2.360	200.000(10G)	70.000
USB3	I	10	2.360	200.000	70.000
DDR	I/T/A	4	5.901	500.000	175.000
PCIE	L/A	28, 32, 45	(0.843), (0.738), (0.524)	71.429, 62.500, 44.444	25.000, 21.875, 15.556

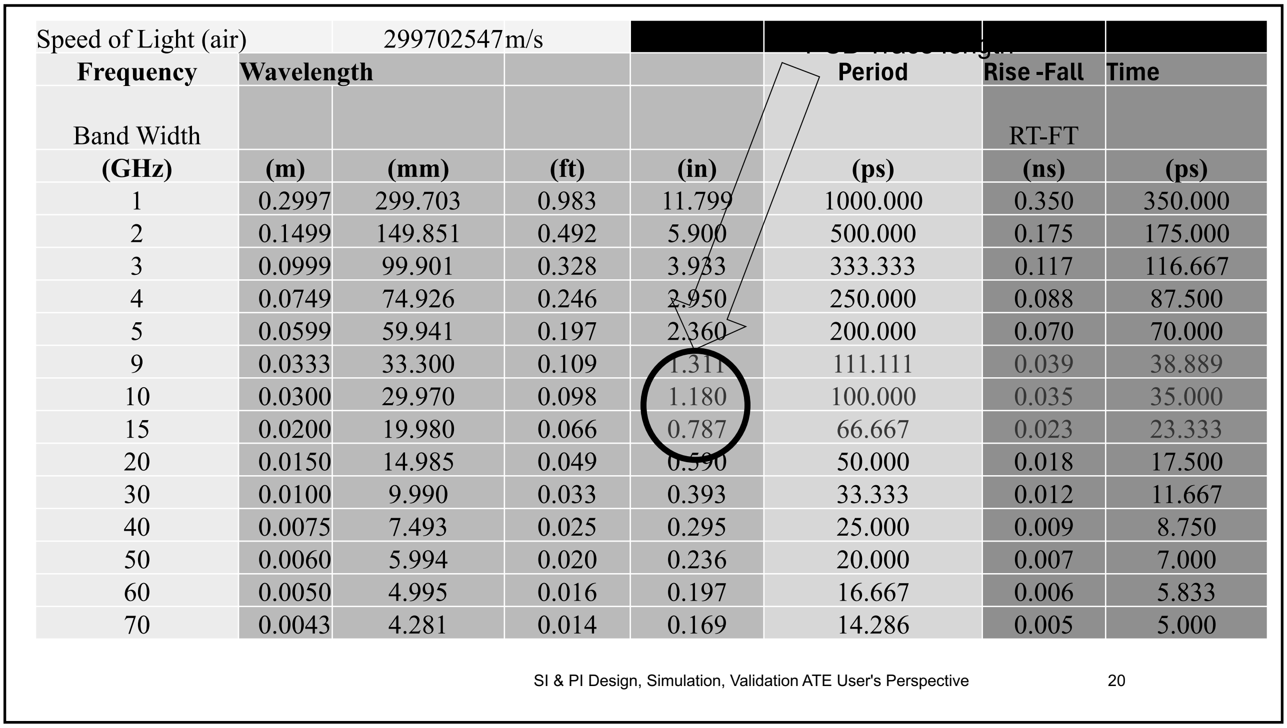
- Board Thickness is 0.300” +.
- Shortest trace length per segment is 0.900”.
- Typical Pogo pin is 0.157”.
- The length, spread of impedance anomalies must be less than Tr (Rise Time) before PS SI problems arises “Dr. Bugatin’s SI, PI Integrity .”



Speed of Light (air) | 299702547 | m/s

Frequency

Band Width (GHz)	**Wavelength (m)**	**(mm)**	**(ft)**	**(in)**	**Period (ps)**
1	0.2997	299.703	0.983	11.799	1000.000
2	0.1499	149.851	0.492	5.900	500.000
3	0.0999	99.901	0.328	3.933	333.333
4	0.0749	74.926	0.246	2.950	250.000
5	0.0599	59.941	0.197	2.360	200.000
9	0.0333	33.300	0.109	1.311	111.111
10	0.0300	29.970	0.098	1.180	100.000
15	0.0200	19.980	0.066	0.787	66.667
20	0.0150	14.985	0.049	0.590	50.000
30	0.0100	9.990	0.033	0.393	33.333
40	0.0075	7.493	0.025	0.295	25.000
50	0.0060	5.994	0.020	0.236	20.000
60	0.0050	4.995	0.016	0.197	16.667
70	0.0043	4.281	0.014	0.169	14.286

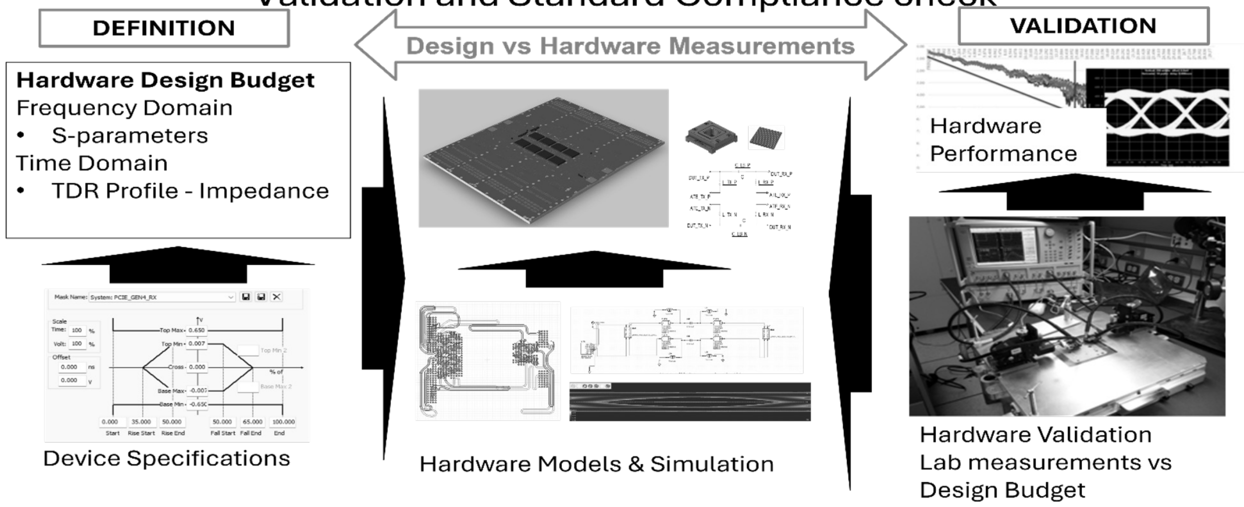


Speed of Light (air) | 299702547m/s

PCB Trace length

Frequency	**Wavelength**				**Period**	**Rise -Fall**	**Time**
Band Width						RT-FT	
(GHz)	**(m)**	**(mm)**	**(ft)**	**(in)**	**(ps)**	**(ns)**	**(ps)**
1	0.2997	299.703	0.983	11.799	1000.000	0.350	350.000
2	0.1499	149.851	0.492	5.900	500.000	0.175	175.000
3	0.0999	99.901	0.328	3.933	333.333	0.117	116.667
4	0.0749	74.926	0.246	2.950	250.000	0.088	87.500
5	0.0599	59.941	0.197	2.360	200.000	0.070	70.000
9	0.0333	33.300	0.109	1.311	111.111	0.039	38.889
10	0.0300	29.970	0.098	1.180	100.000	0.035	35.000
15	0.0200	19.980	0.066	0.787	66.667	0.023	23.333
20	0.0150	14.985	0.049	0.590	50.000	0.018	17.500
30	0.0100	9.990	0.033	0.393	33.333	0.012	11.667
40	0.0075	7.493	0.025	0.295	25.000	0.009	8.750
50	0.0060	5.994	0.020	0.236	20.000	0.007	7.000
60	0.0050	4.995	0.016	0.197	16.667	0.006	5.833
70	0.0043	4.281	0.014	0.169	14.286	0.005	5.000

Closed Loop Hardware Design Flow
Validation and Standard Compliance check



Hardware Design Budget
Frequency Domain
- S-parameters

Time Domain
- TDR Profile - Impedance

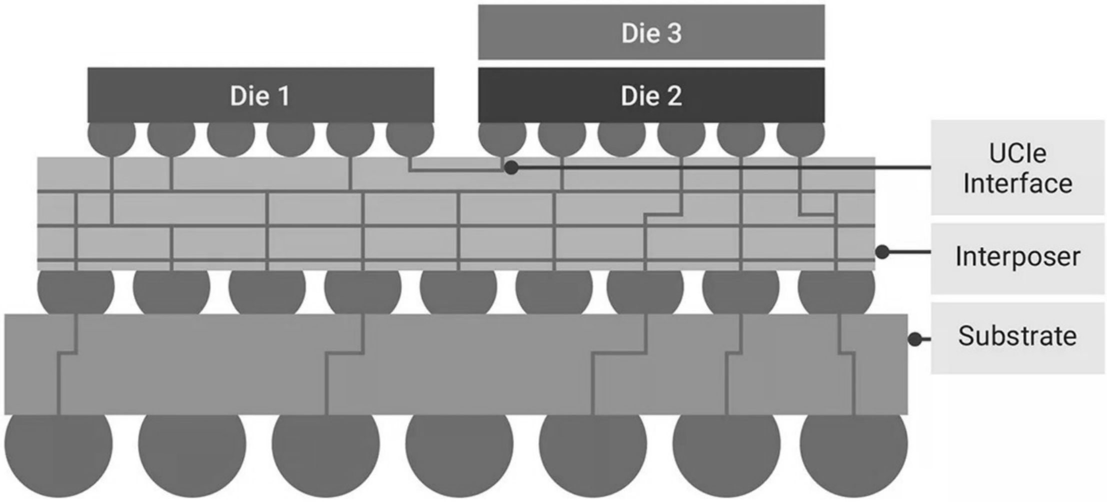
Device Specifications

Hardware Models & Simulation

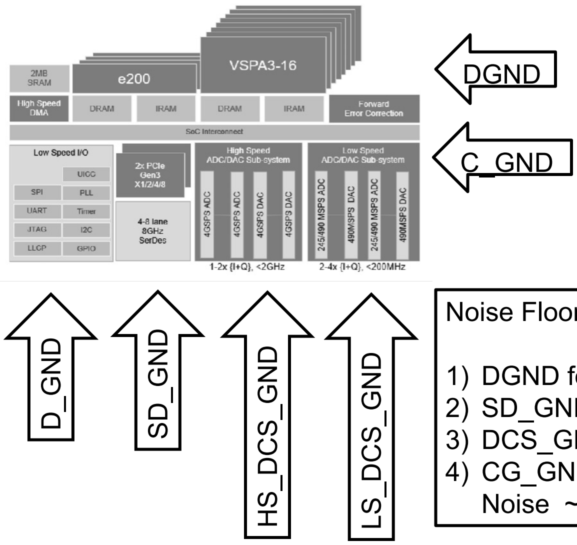
Hardware Performance

Hardware Validation
Lab measurements vs
Design Budget

Chiplets, Advanced Packaging, Integration of IPs



Typical Mixed Signal Device



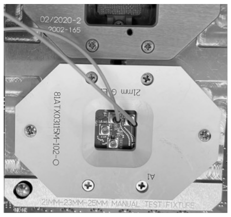
Different power, ground domain as function of IP

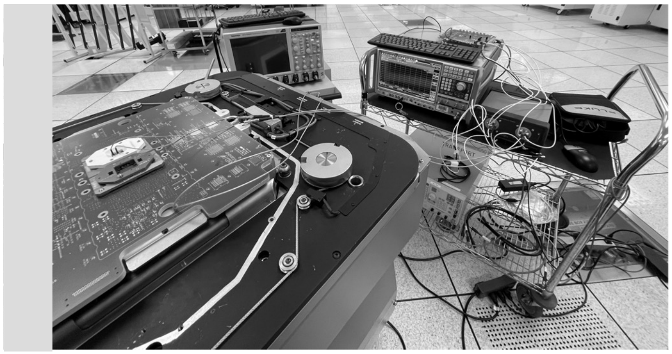
1) DGND for Digital Core, and I/Os
2) SD_GND for high speed serdes
3) DCS_GND(LS_DCS_GND, HS_DCS_GND) for ADC/DAC IPS, and I/Os
4) CG_GND for Low Jitter reference clock

Noise Floor sensitivity as a function of IP

1) DGND for Digital Core, and I/Os < (-20dBm)
2) SD_GND for high speed serdes < (-30dBm)
3) DCS_GND(LS_DCS_GND, HS_DCS_GND) < (-90dBm) or better
4) CG_GND for Low Jitter reference clock < (-140dBm), Phase Noise ~ 80femto seconds

DUT Signal, Clock, Noise Floor Measurement Setup at the test site





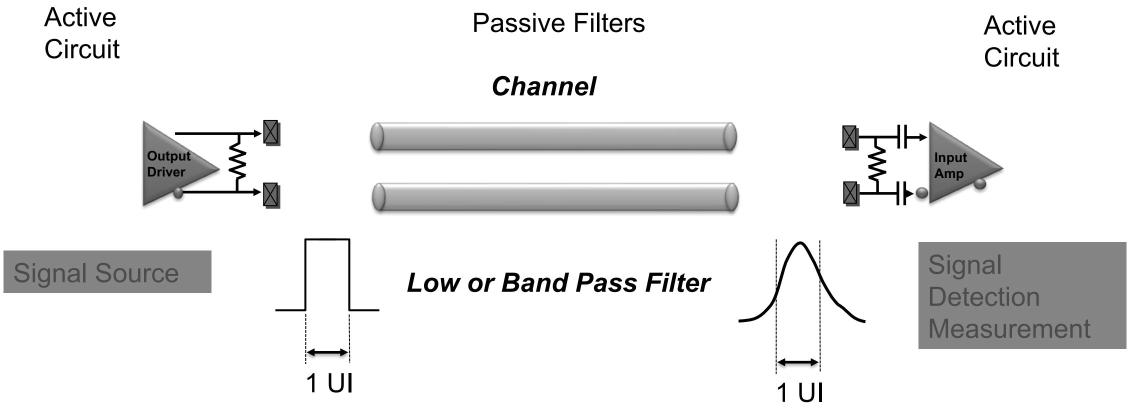
Measurements with Active Program, Patterns, Power Supplies

At the test site package balls

Noise, Noise Floor, Clock, ATE Signal, DUT Outputs

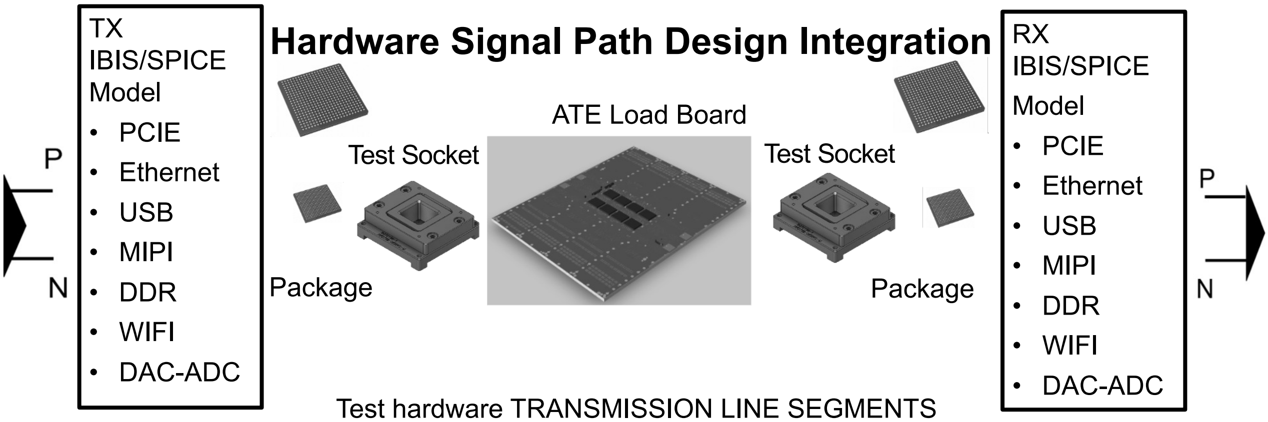
Questions ?

PASSIVE FILTERS
ATE PERSPECTIVE
TEST HARDWARE



ATE Loop Back Test

Hardware Signal Path Design Integration



TX
IBIS/SPICE
Model
- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

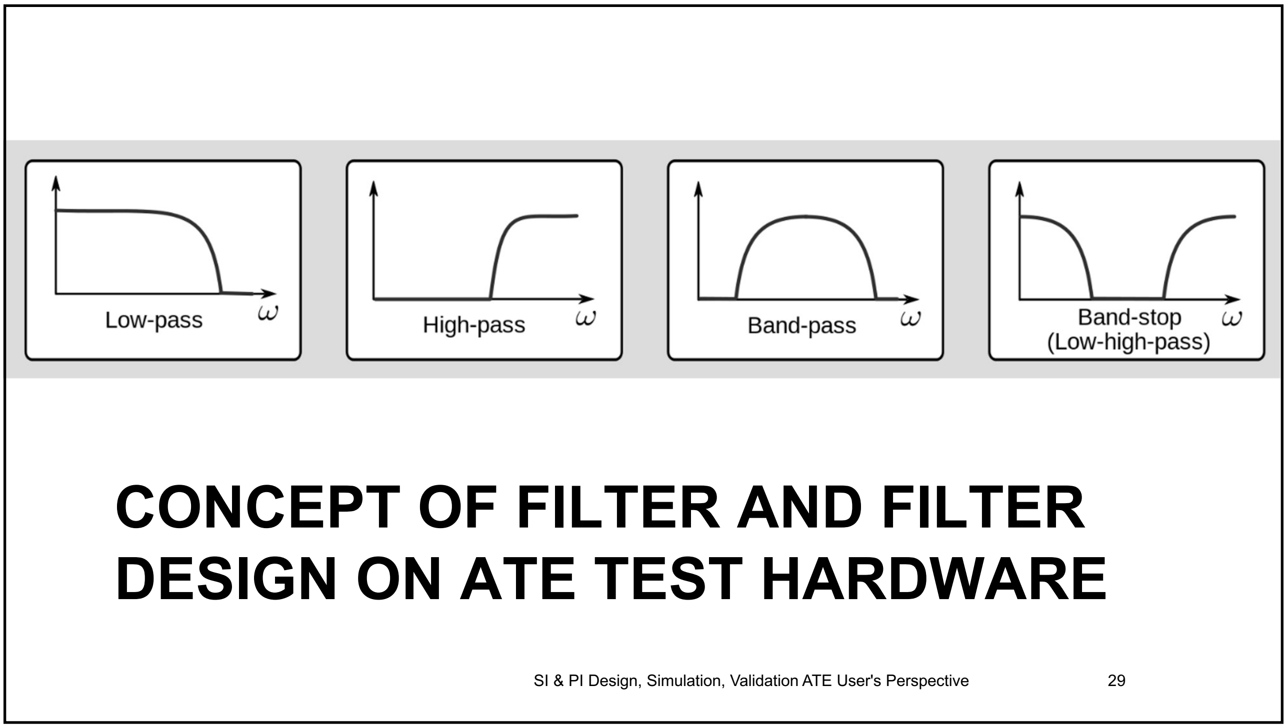
RX
IBIS/SPICE
Model
- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

Test hardware TRANSMISSION LINE SEGMENTS

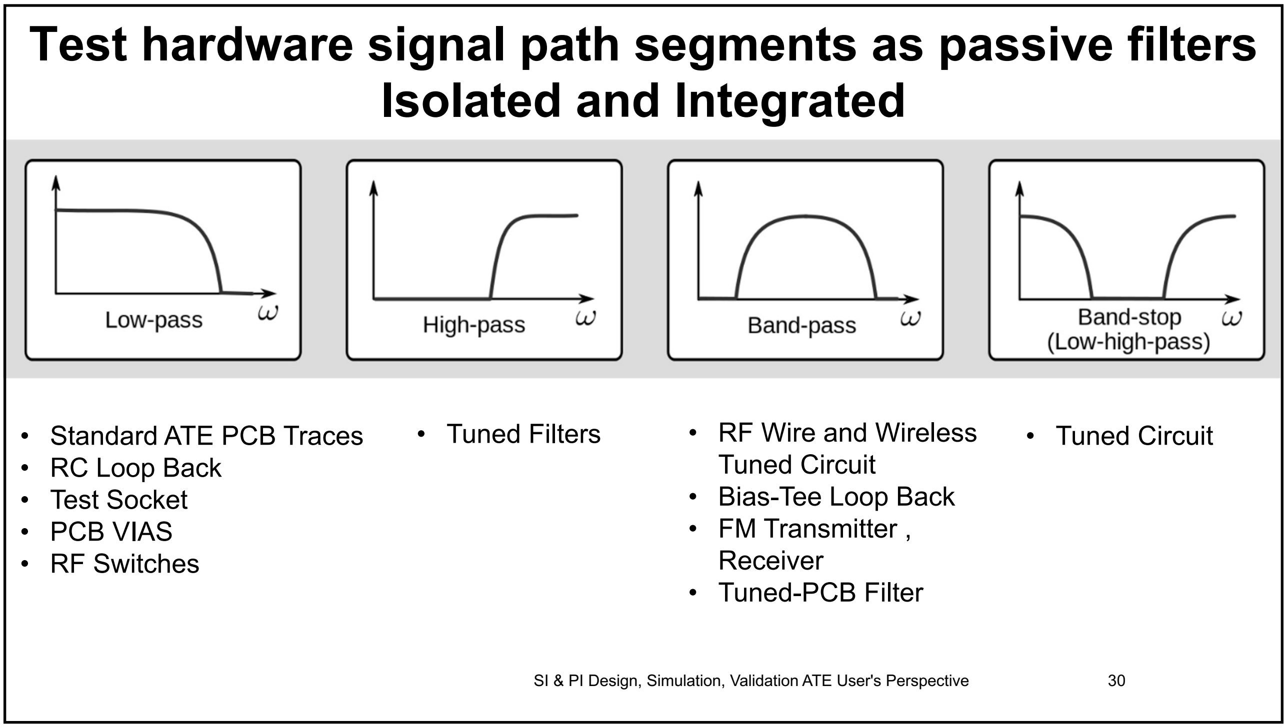
Format

Format

Functional, Speed, RF-Parametric test don’t involve the ATE



CONCEPT OF FILTER AND FILTER DESIGN ON ATE TEST HARDWARE



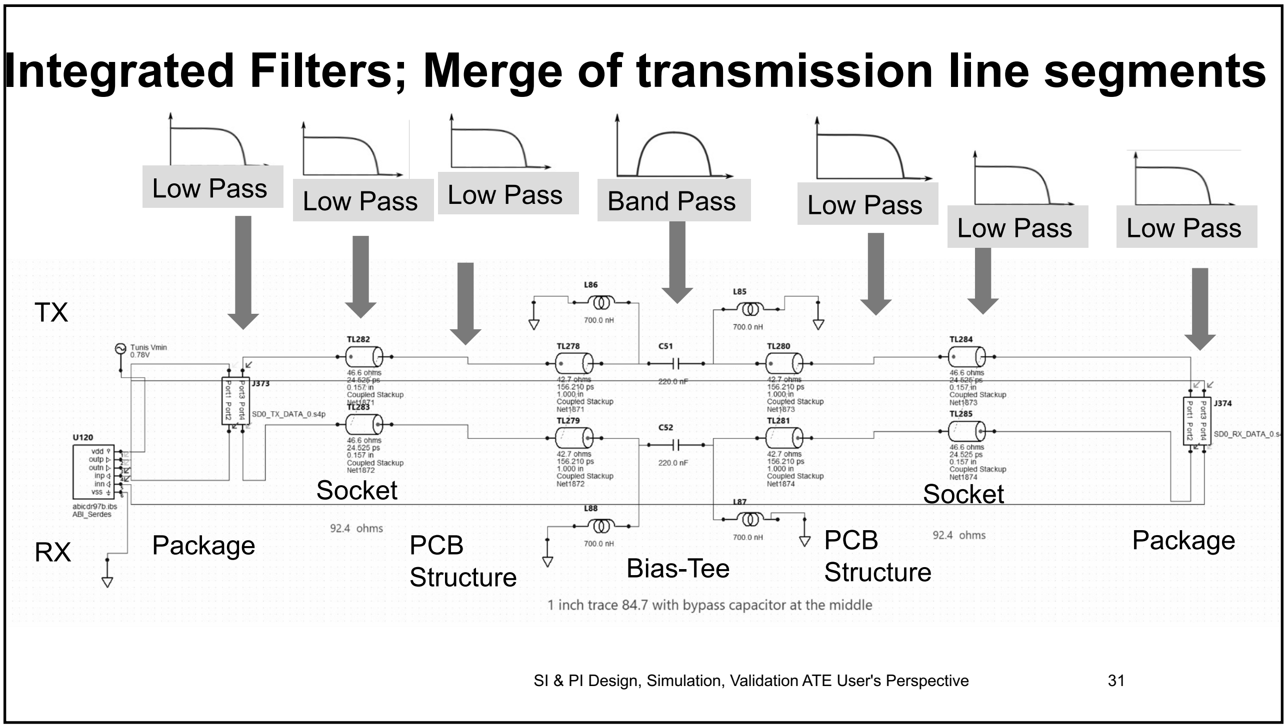
Test hardware signal path segments as passive filters Isolated and Integrated

- Standard ATE PCB Traces
- RC Loop Back
- Test Socket
- PCB VIAS
- RF Switches

- Tuned Filters

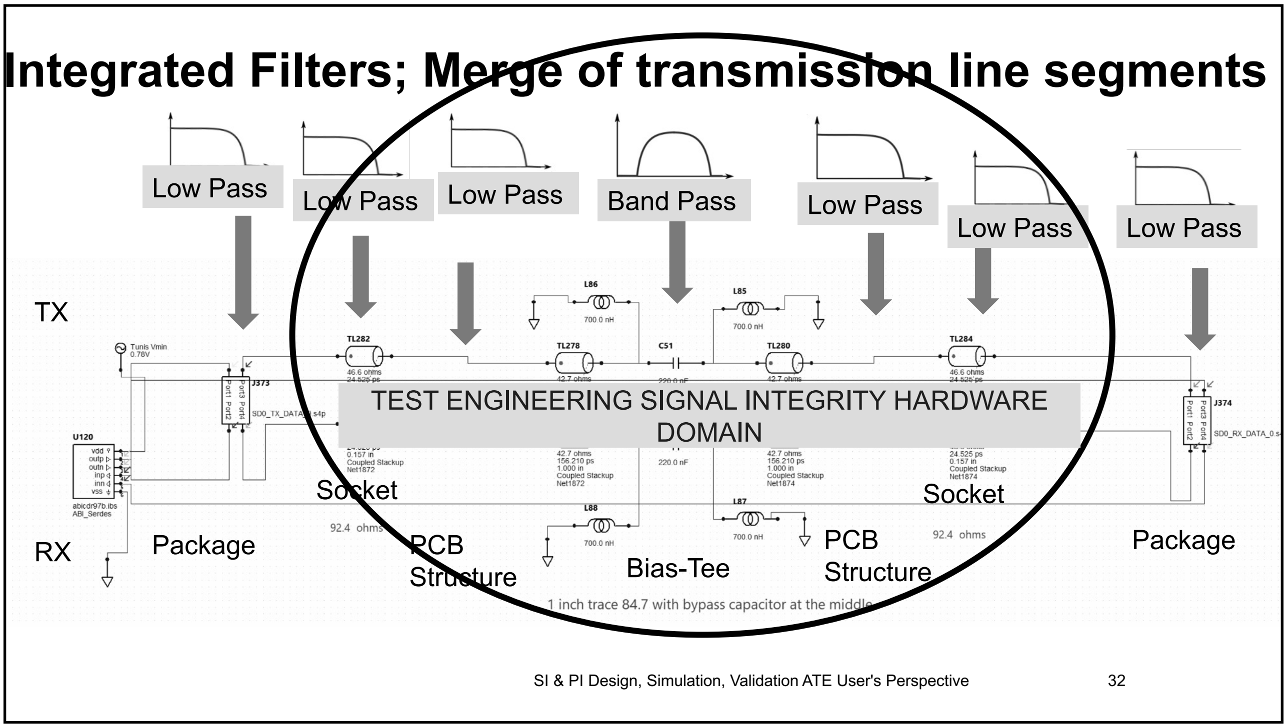
- RF Wire and Wireless Tuned Circuit
- Bias-Tee Loop Back
- FM Transmitter , Receiver
- Tuned-PCB Filter

- Tuned Circuit



Integrated Filters; Merge of transmission line segments

1 inch trace 84.7 with bypass capacitor at the middle



Integrated Filters; Merge of transmission line segments

1 inch trace 84.7 with bypass capacitor at the middle

LOOP BACK CIRCUITS

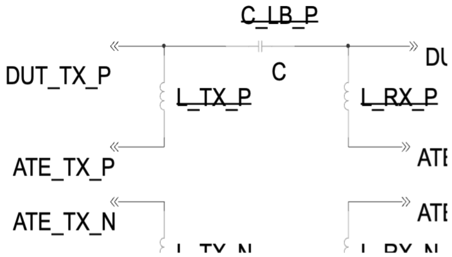
- LC or Bias-Tee (Inductor –Capacitor)
- RC (Resistor – Capacitor)
- RF Switches

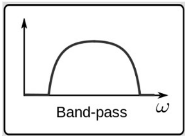
PASSIVE FILTERS

Band-Pass Filter: LC Loop Back Circuit

Serdes Loop Back Circuit

- Electrical link. A transmission line from DUT transmitter drivers to DUT receivers to facilitate self-test at specified data rate.
- A bypass-capacitor is required to eliminate the transmitter common-mode at the receiver input.
- The Inductor provides electrical link to ATE channel to facilitate structural, functional, and parametric type test.
- Inductor provides a high impedance isolation between DUT pin and ATE channel

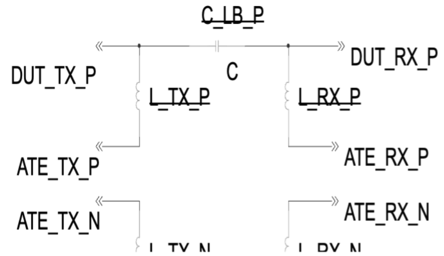


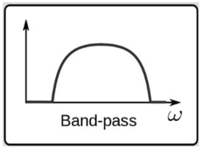


Band-Pass Filter: LC Loop Back Circuit Characteristics

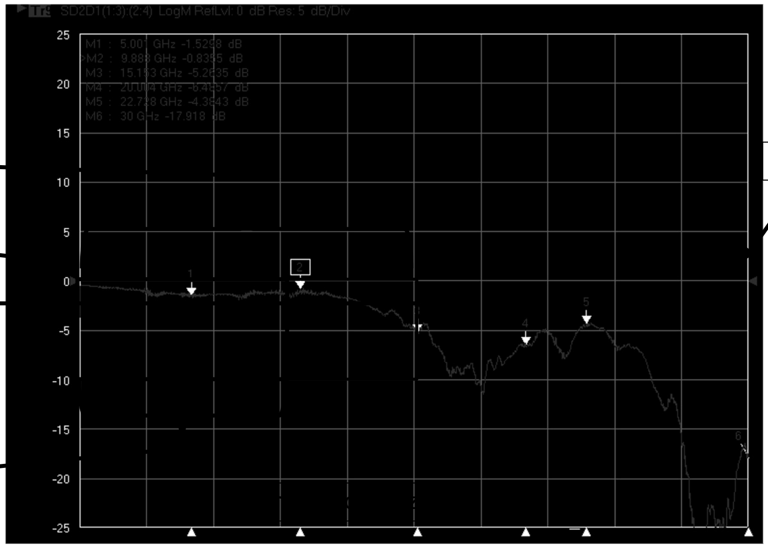
Characteristics

- Insertion Loss (S21, D2D1) starts at negative or very low power level at low frequency range. Inductive short at low frequency is ideal for parametric type testing
- Validated inductor broadband performance can contain impedance-change from TX-output to RX-input to required range(e.g. 10 ohms window)
- High reliability loop back circuit.
- Next to RC in small footprint for high I/O count devices (e.g. 64 Serdes lanes)
- Coil variability and non-linearity is common as a function of frequency





Band-Pass Filter: LC Loop Back Circuit



28G HW Pass Region

Power dBm

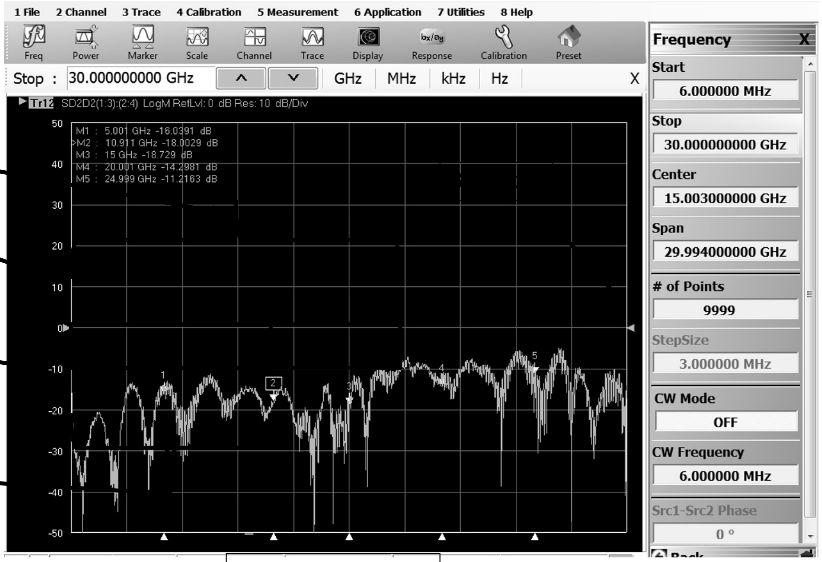
3dBm HW Budget

Short, low impedance @ Low Frequency

16G HW Pass Region

30 GHz

Band-Pass Filter: LC Loop Back Circuit



28 G HW Pass Region

Power dBm

-10dB HW Budget

16 G HW Pass Region

Frequency GHz

Stop : 30.000000000 GHz

```
Tr12 SD2D2(1:3):(2:4) LogM RefLvl: 0 dB Res: 10 dB/Div
 M1 :  5.001 GHz -16.0391 dB
>M2 :  10.911 GHz -18.0029 dB
 M3 :  15 GHz -18.729 dB
 M4 :  20.001 GHz -14.2981 dB
 M5 :  24.999 GHz -11.2163 dB
```

Frequency

Start: 6.000000 MHz

Stop: 30.000000000 GHz

Center: 15.003000000 GHz

Span: 29.994000000 GHz

\# of Points: 9999

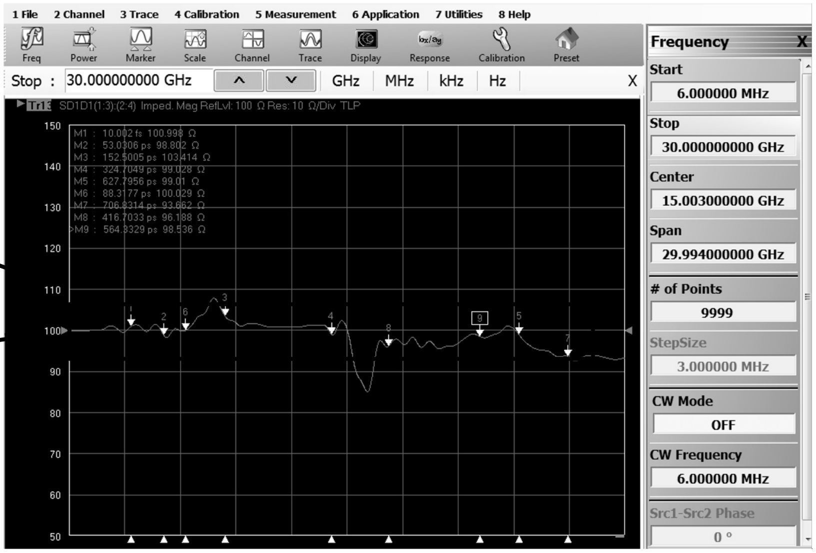
StepSize: 3.000000 MHz

CW Mode: OFF

CW Frequency: 6.000000 MHz

Src1-Src2 Phase: 0 °

Band-Pass Filter: LC Loop Back Circuit Impedance Profile



Good impedance profile from TX to RX

Impedance Ohms

10 Ohms HW Budget

Stop : 30.000000000 GHz

```
Tr13 SD1D1(1:3):(2:4) Imped. Mag RefLvl: 100 Ω Res: 10 Ω/Div TLP
 M1 :  10.002 fs  100.998 Ω
 M2 :  53.0306 ps  98.802 Ω
 M3 :  152.5005 ps  103.414 Ω
 M4 :  324.7049 ps  99.028 Ω
 M5 :  627.7956 ps  99.01 Ω
 M6 :  88.3177 ps  100.029 Ω
 M7 :  706.8314 ps  93.662 Ω
 M8 :  416.7033 ps  96.188 Ω
>M9 :  564.3329 ps  98.536 Ω
```

Frequency

Start: 6.000000 MHz

Stop: 30.000000000 GHz

Center: 15.003000000 GHz

Span: 29.994000000 GHz

\# of Points: 9999

StepSize: 3.000000 MHz

CW Mode: OFF

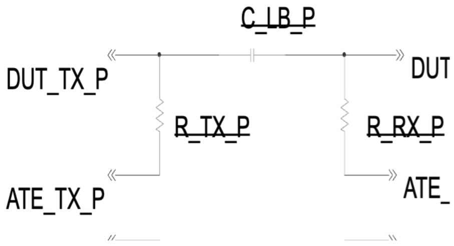
CW Frequency: 6.000000 MHz

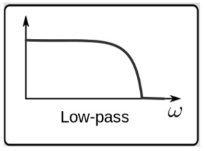
Src1-Src2 Phase: 0 °

Low Pass Filter: RC Loop Back Circuit

Serdes Loop Back Circuit

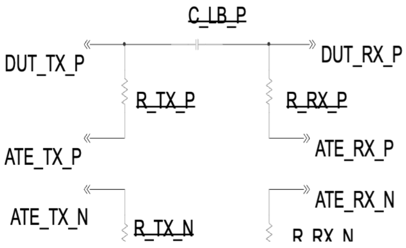
- Electrical link. A transmission line from DUT transmitter drivers to DUT receivers to facilitate self-test at specified data rate.
- A bypass-capacitor is required to eliminate the transmitter common-mode at the receiver input.
- The resistor provides a high impedance isolation between DUT pin and ATE channel

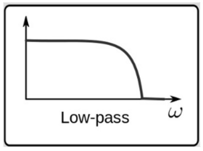




Low Pass Filter: RC Loop Back Circuit

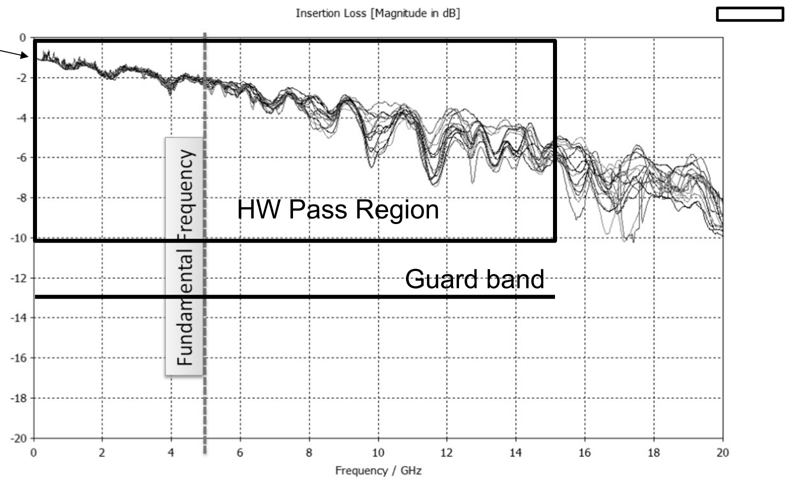
- Step function impedance profile from TX-output to RX-input defined by the resistance value of the filter
- Insertion loss starts are preset value at dc or frequency zero. Insertion loss start value is defined by the resistance of the filter
- Excellent linearity for the insertion loss(S21, D2D1) curve
- High reliability and less exposure to component failure
- Small footprint for high Serdes lane count (e.g. 64 lanes)
- Parametric test is a challenged with ATE-access limited by the series resistance

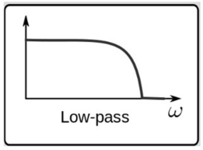




Low Pass Filter: RC Loop Back Circuit

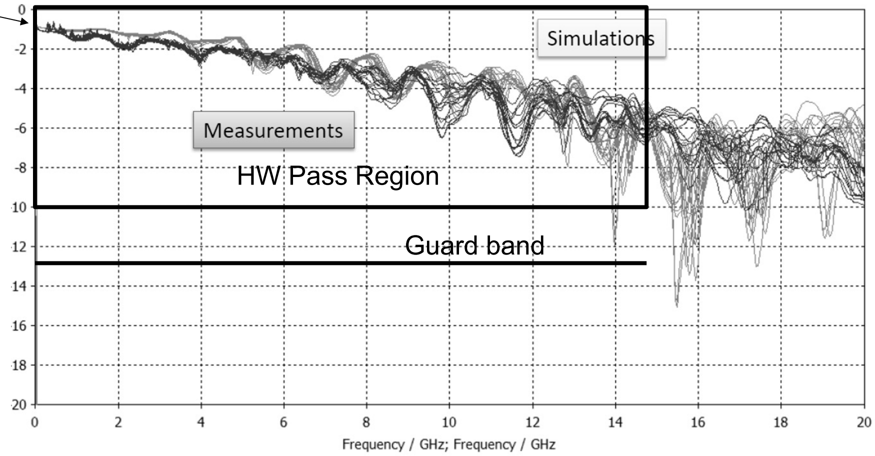
RC Profile
- Default signal loss at Frequency=0
- Loss magnitude is a function of the R-value on the loop back filter.

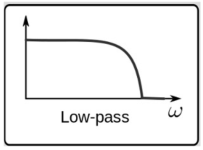


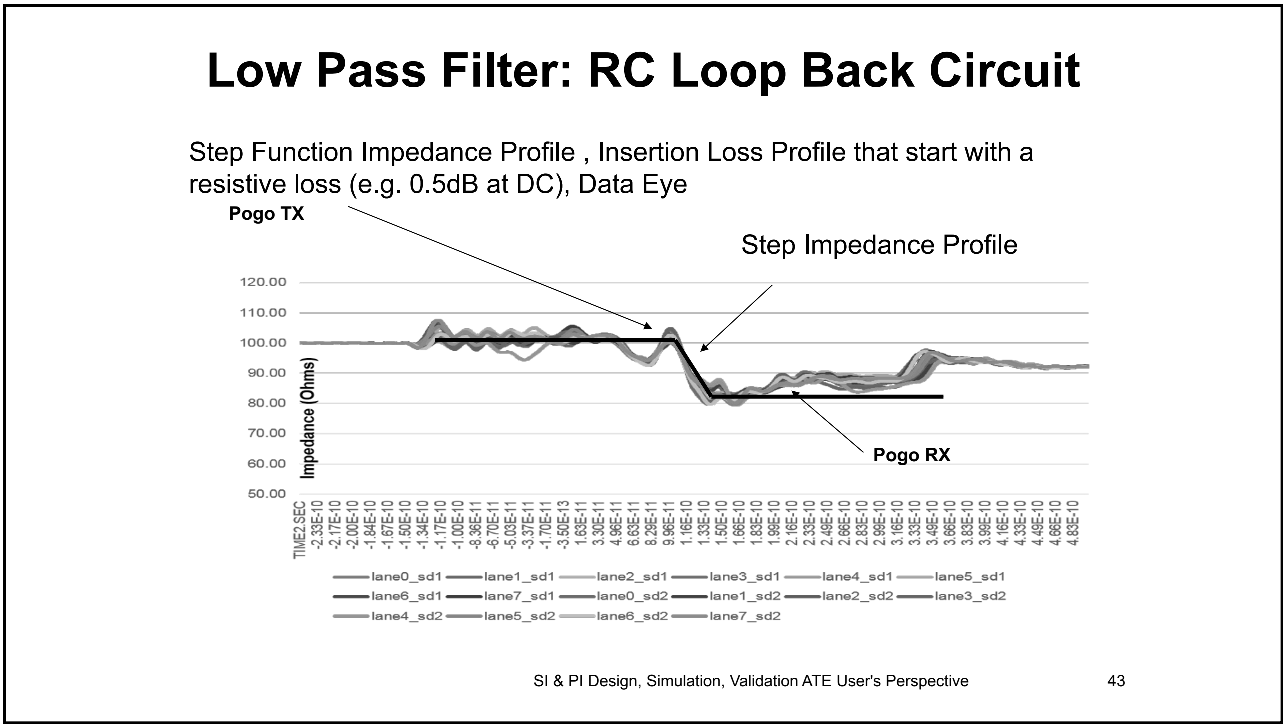


Low Pass Filter: RC Loop Back Circuit

RC Profile
- Default signal loss at Frequency=0
- Loss magnitude is a function of the R-value on the loop back filter.







Low Pass Filter: RC Loop Back Circuit

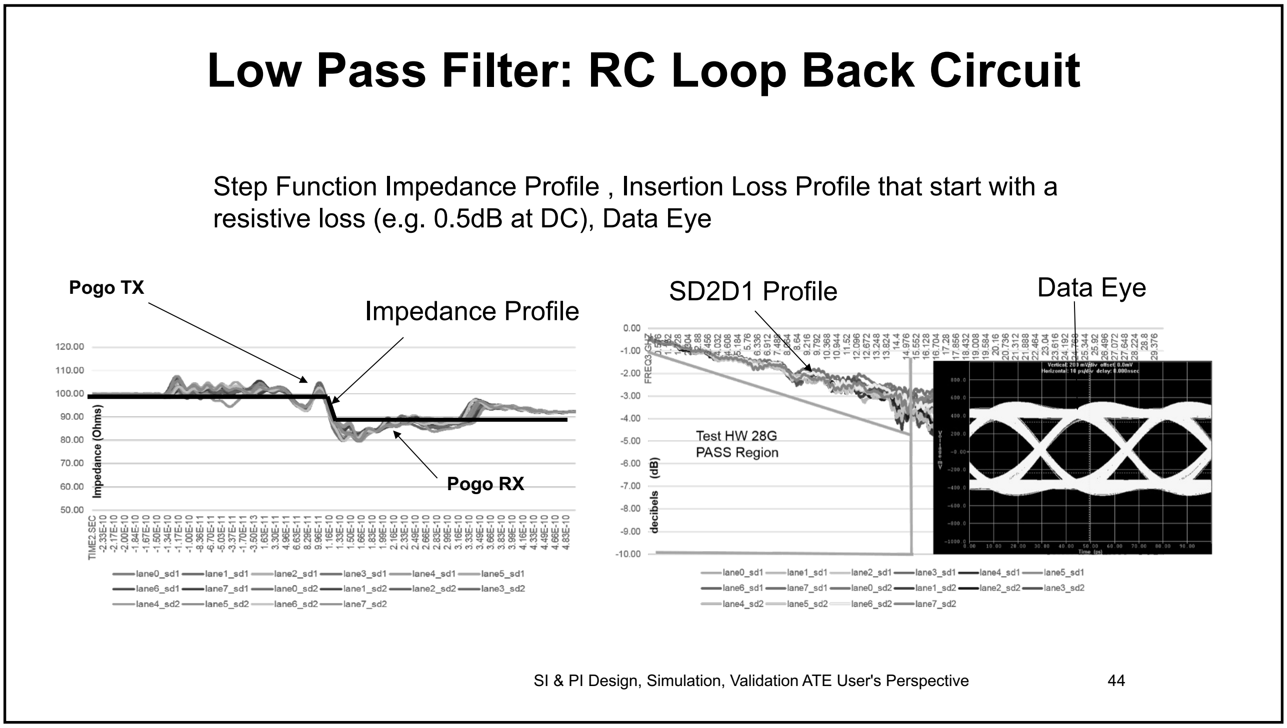
Step Function Impedance Profile , Insertion Loss Profile that start with a resistive loss (e.g. 0.5dB at DC), Data Eye

Pogo TX

Step Impedance Profile

Pogo RX

SI & PI Design, Simulation, Validation ATE User's Perspective



Low Pass Filter: RC Loop Back Circuit

Step Function Impedance Profile , Insertion Loss Profile that start with a resistive loss (e.g. 0.5dB at DC), Data Eye

Pogo TX

Impedance Profile

SD2D1 Profile

Data Eye

Pogo RX

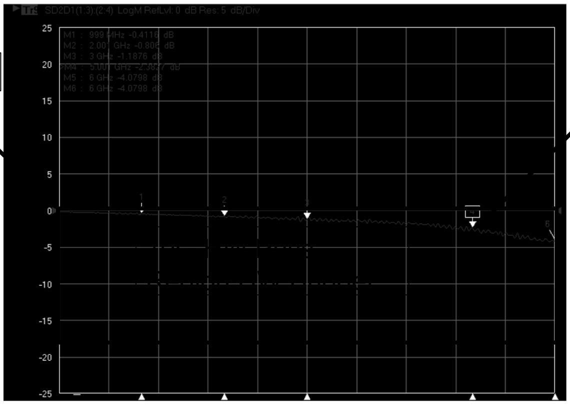
Test HW 28G
PASS Region

SI & PI Design, Simulation, Validation ATE User's Perspective

Low Pass Filter: RF Switch

Measured Insertion Loss D2D1

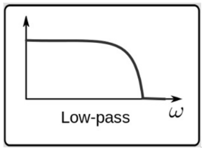
Power (dBm)



Frequency (GHz)

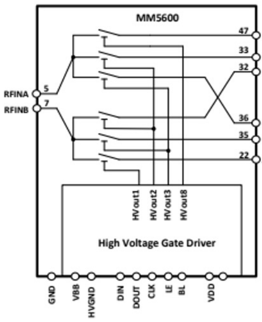
RF Differential Switch

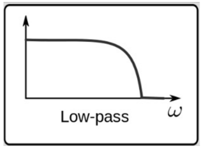
1. Low loss
2. Wideband performance better linearity
3. Small package mems switch that match differential trace



Low Pass Filter: RF Switch characteristic

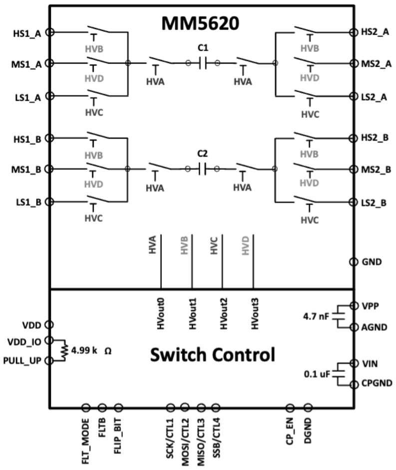
- Can support functional and parametric test with less constraints
- Broadband performance is dictated by switch specification
- Good Linearity for the insertion loss (S21, D2D1) curve
- RF switch life as declared by vendor
- MEMS RF switch small package footprint is ideal for match differential pair routing that don’t require change on trace spacing

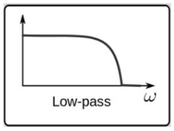




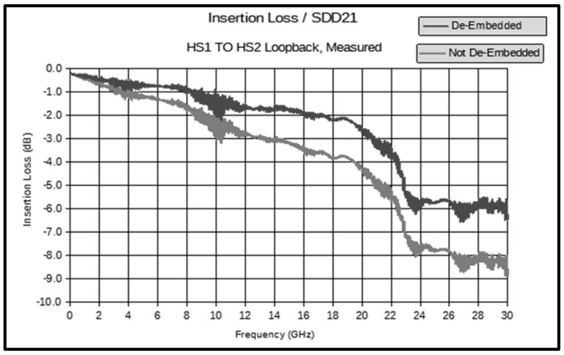
Low Pass Filter RF Switch MM5620

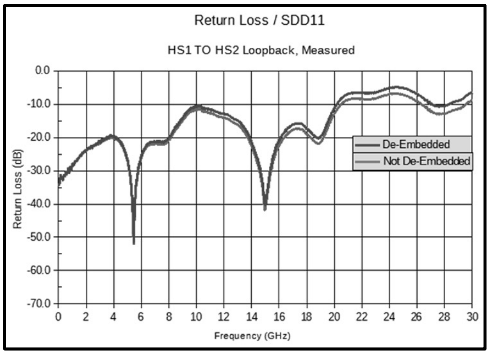
- Excellent eye performance for the PCIe 4/5/6
- Superior RF performances
- Supports 100% functional and parametric test
- Greater than 3 Billion electrical life cycles
- Integrated charge pump, high voltage driver, and AC coupling capacitors
- SPI or GPIO interface
- Fully support both high speed and DC sweep signal paths
- Smaller package size

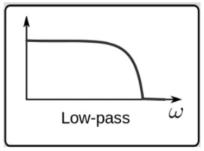




Low Pass Filter RF Switch MM5620



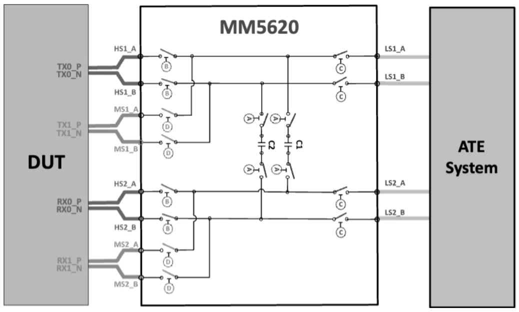


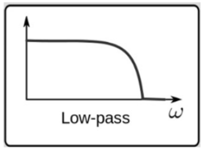


Measured SDD21, De-embedded
-1.85dB @ 16GHz

Measured SDD11, De-embedded
-22.1dB @ 16GHz

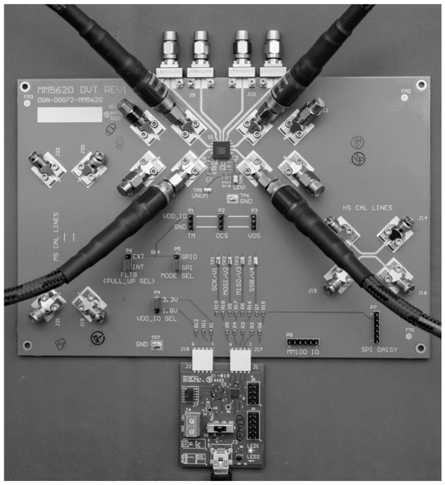
Low Pass Filter RF Switch MM5620



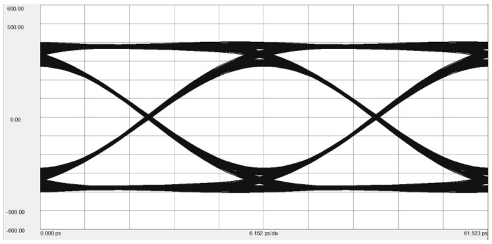


- Test Two PCIe 4/5/6 lanes at high-speed using ONE MM5620 device
  - TX0_X ← → RX0_X (HS1 ← → HS2) at speed test
  - TX1_X ← → RX1_X (MS1 ← → MS2) at speed test
- – LS signals can be shared for low frequency and DC sweep test
- Two transmitters can be ALWAYS ON to reduce the test time
- Fully bi-directional signal paths

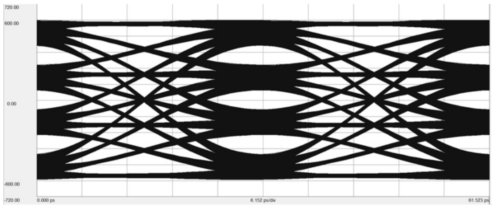
Low Pass Filter RF Switch MM5620



MM5620 evaluation board



PCIe Gen5: +/-400mV, NRZ, 32 GBps, PRBS 2^{15}-1



PCIe Gen6: +/-600mV, PAM4,32GBaud (64GBps), PRBS 2^{15}-1

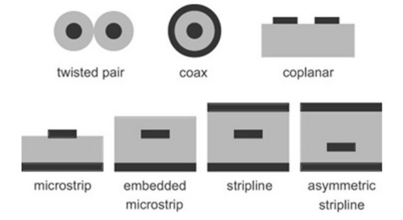
LOOP BACK CIRCUITS

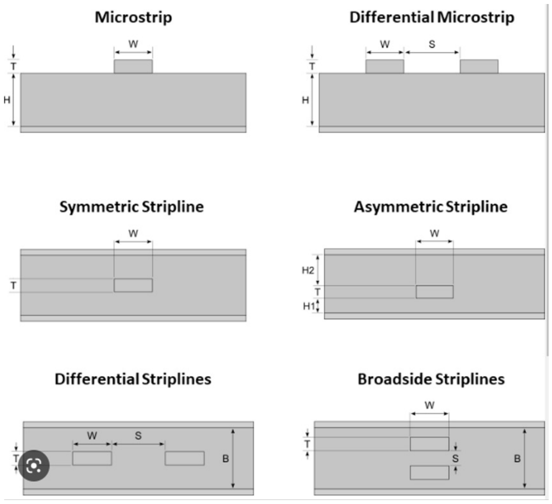
- PCB Structures
- Test Socket
- Device Package

PASSIVE FILTERS

Passive Filters : Signal path, medium (wired transmission line)

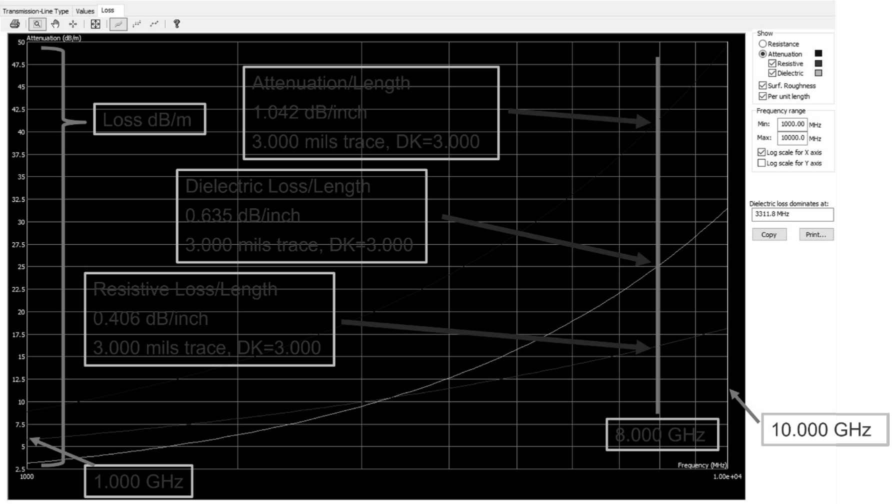
Uniform Transmission line (Wired medium)





- We move different types of signal to the test hardware from the socket through the loadboard
- Asymmetric configuration is commonly used or applied
- Stripline is highly recommended for SI considerations for Analog RF, High Speed digital

Low Pass Filter PCB Differential Trace



Min: 1000.00 MHz

Max: 10000.0 MHz

☑ Log scale for X axis

☐ Log scale for Y axis

Dielectric loss dominates at: 3311.8 MHz

Loss dB/m

Attenuation/Length
1.042 dB/inch
3.000 mils trace, DK=3.000

Dielectric Loss/Length
0.635 dB/inch
3.000 mils trace, DK=3.000

Resistive Loss/Length
0.406 dB/inch
3.000 mils trace, DK=3.000

1.000 GHz

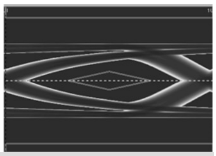
8.000 GHz

10.000 GHz

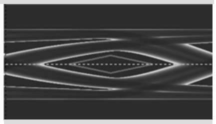
Trace Loss per length as a function of frequency

- 1 Oz, 3mils width strip line
- DK=3
- Dielectric loss curve
- Resistive loss curve as function of trace geometries such as width, and thickness

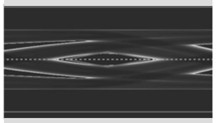
Low Pass Filter PCB Differential Trace



Trace length = 2 inches



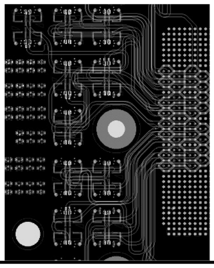
Trace length = 3 inches



Trace length = 4 inches

Shrinking Data Eye as function of trace length

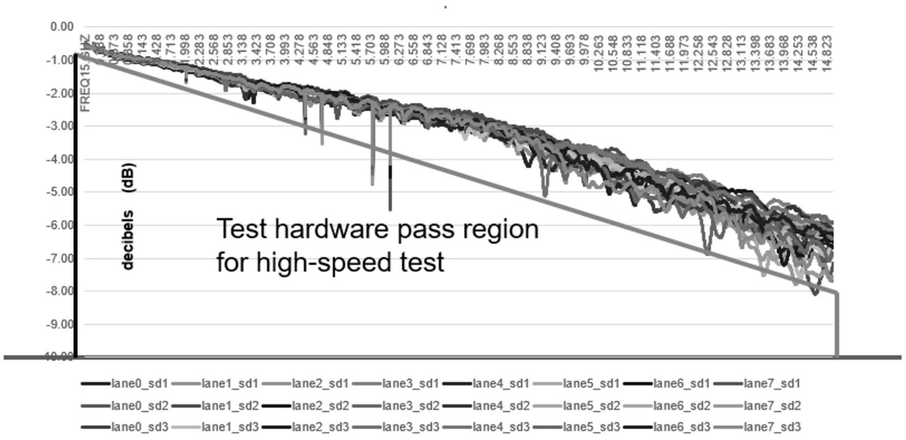
- RC Loop back circuit
- Same dielectric dk=3
- Same thickness 1oz
- Same width= 3mils



PCB trace, vias, pads, dielectric

- Electrical link of the different segment of the signal path
- Physical geometries have profound impact on transmission line performance in frequency and time domain
- PCB Interconnects such as vias, pads are the common source of discontinuity
- Dielectric constant and physical geometries of the structure dominates the signal loss along the signal path

Low Pass Filter PCB Trace Loss

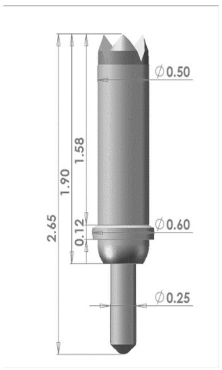


Test hardware pass region
for high-speed test

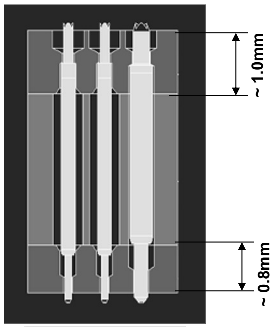
Low Pass Filter PCB Trace Loss

- The biggest source of signal power is the PCB trace.
- Loss as a function of frequency and length
- Geometrical Loss
- Dielectric Loss
- Skin Effect

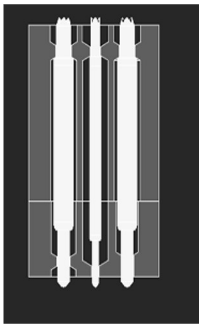
Low Pass Filter Test Socket

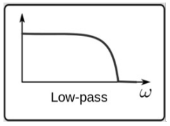


Conventional Coaxial
Limited Coax Structure

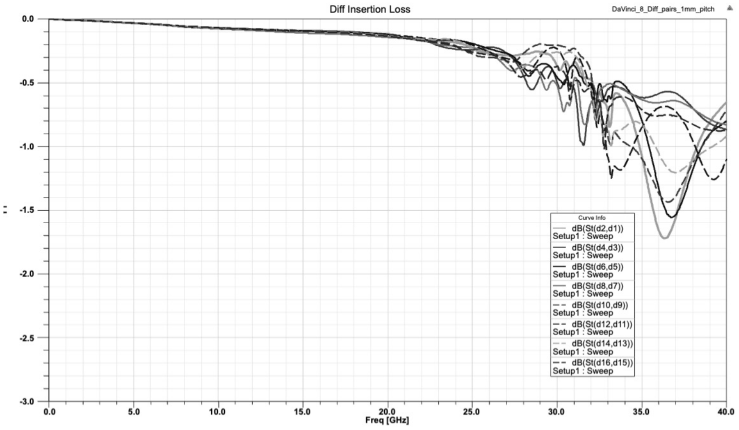


Coaxial
Optimized Coax Structure

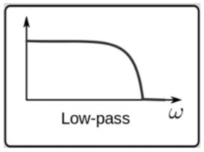




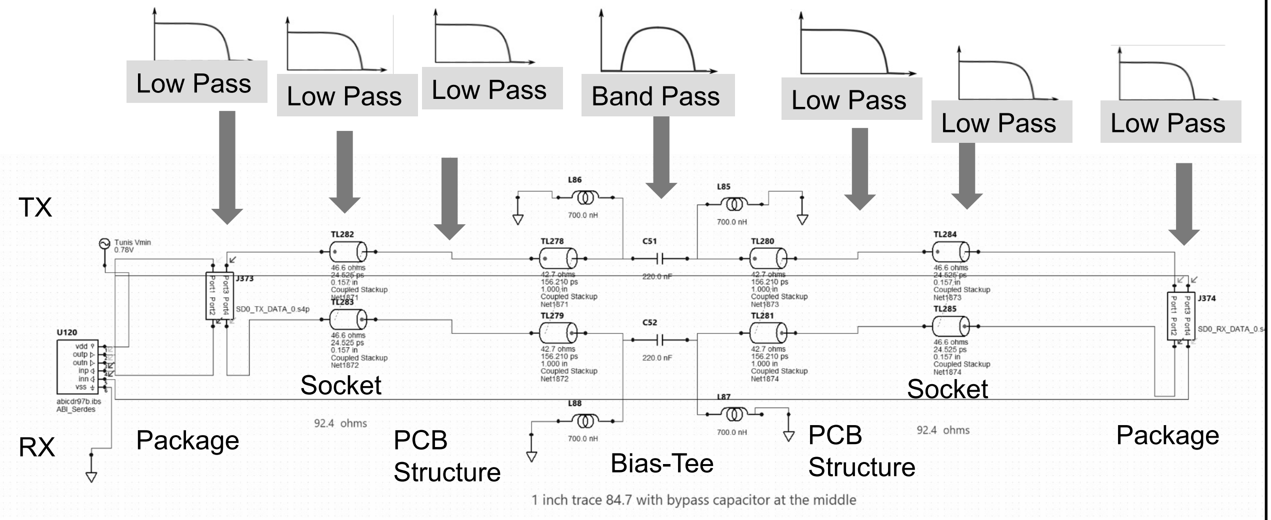
Low Pass Filter Test Socket



- Low loss transmission line segment in general due to geometrical considerations.
- Critical source of discontinuity or impedance mismatch.
  - Integration with the Package
  - Integration with the PCB

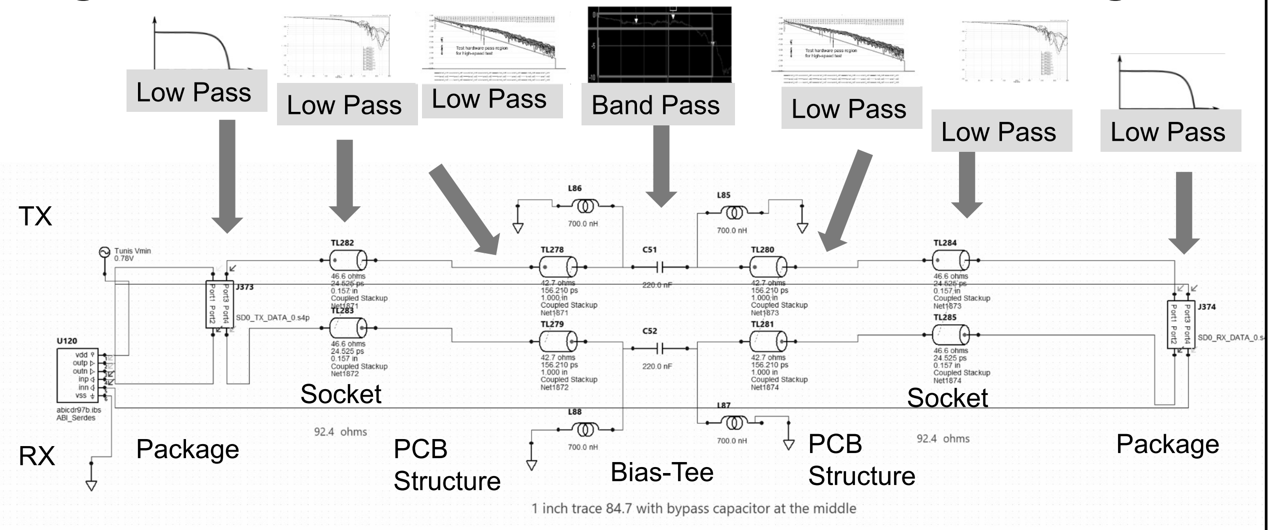


Integrated Filters; Merge of transmission line segments



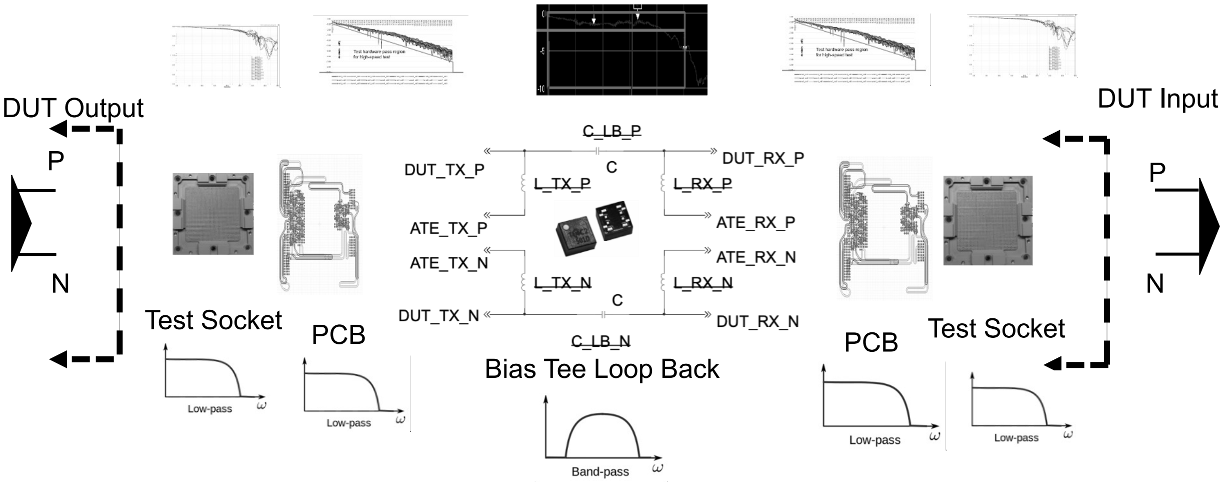
1 inch trace 84.7 with bypass capacitor at the middle

Integrated Filters; Models of transmission line segments



1 inch trace 84.7 with bypass capacitor at the middle

Integrated Filters; Physical World , Real Hardware


DUT Output

P

N

Test Socket

PCB

C_LB_P

DUT_TX_P

C

L_TX_P

ATE_TX_P

ATE_TX_N

L_TX_N

DUT_TX_N

C

C_LB_N

DUT_RX_P

L_RX_P

ATE_RX_P

ATE_RX_N

L_RX_N

DUT_RX_N

Bias Tee Loop Back

PCB

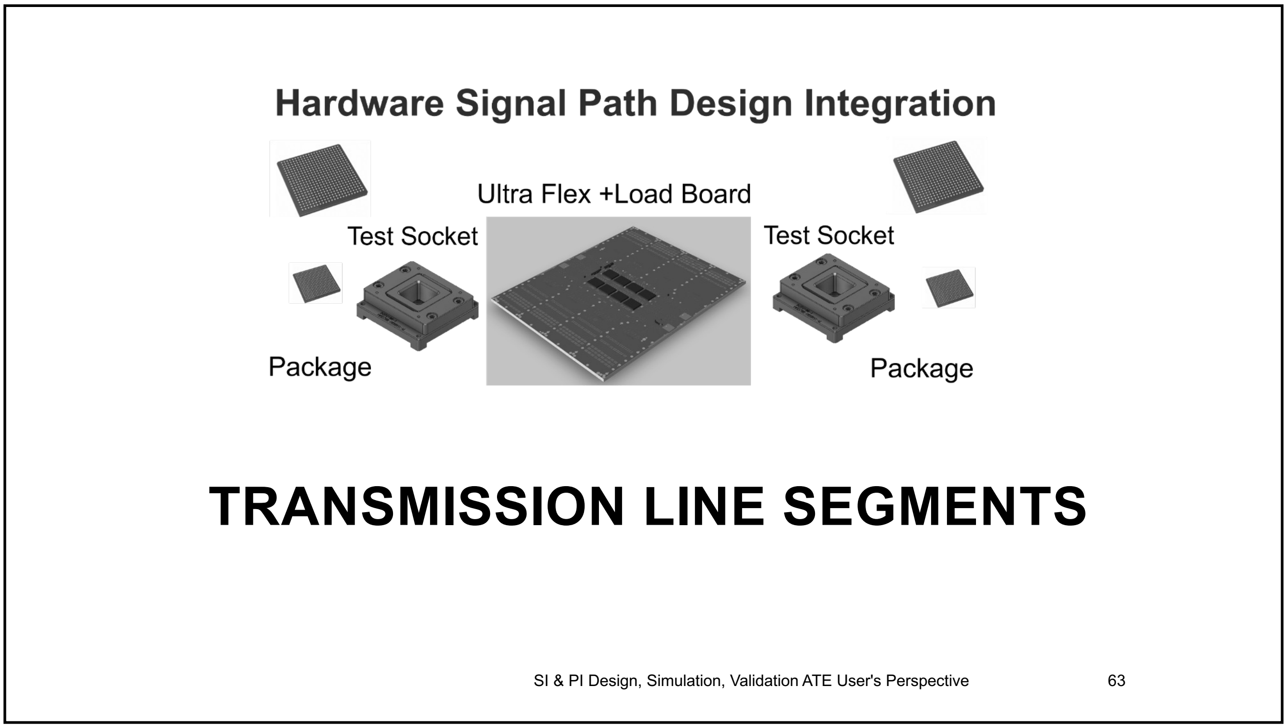
Test Socket

DUT Input

P

N

Questions ?



Hardware Signal Path Design Integration

Ultra Flex +Load Board

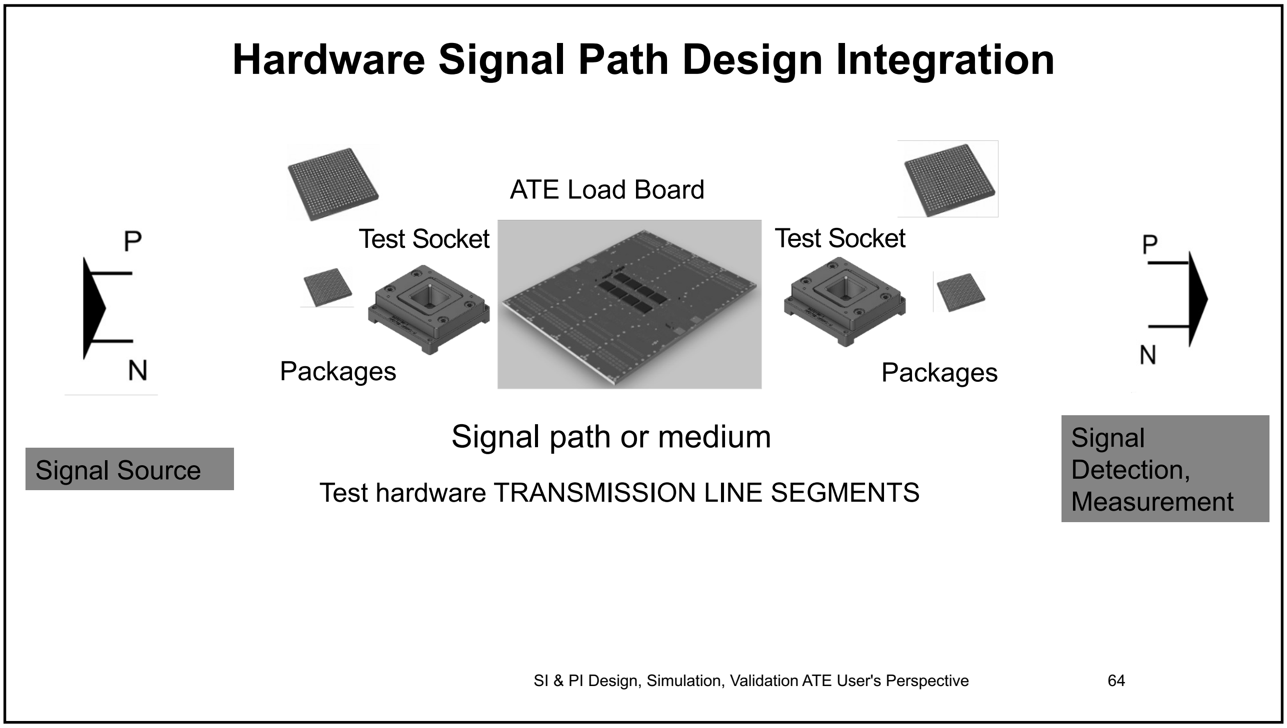
Test Socket

Test Socket

Package

Package

TRANSMISSION LINE SEGMENTS



Hardware Signal Path Design Integration

ATE Load Board

Test Socket

Test Socket

P

N

Packages

Packages

P

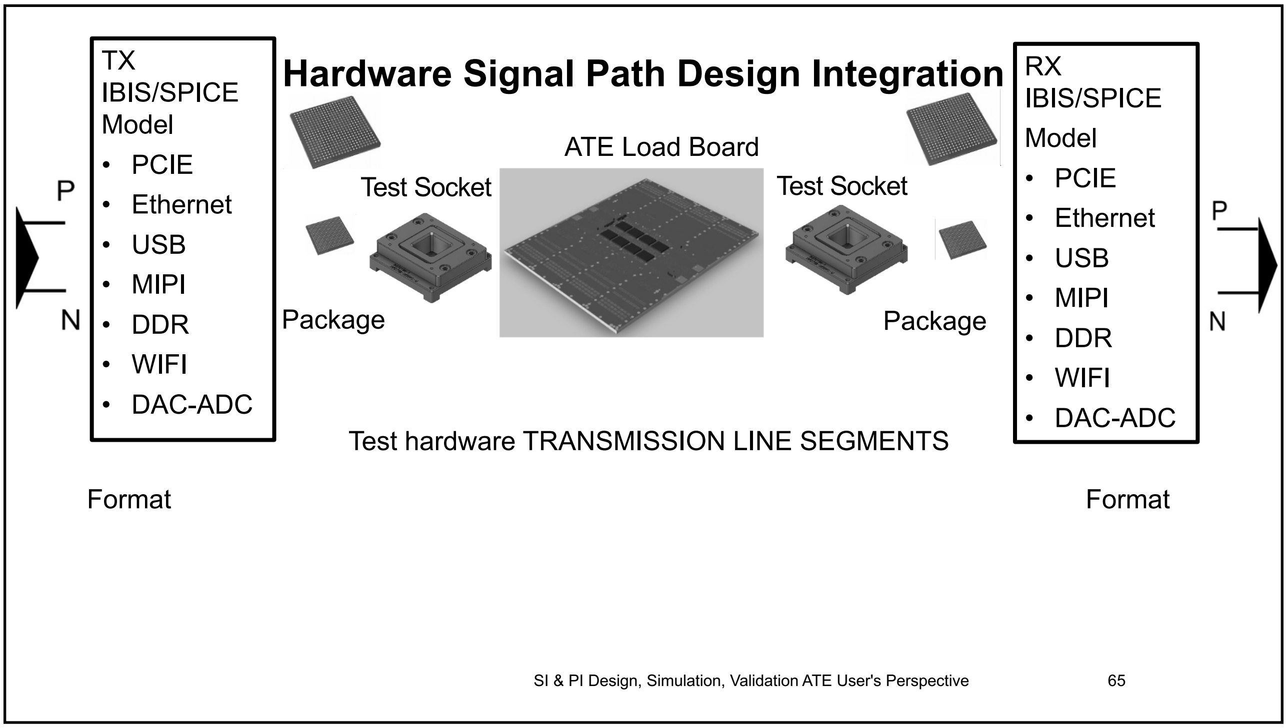
N

Signal path or medium

Signal Source

Test hardware TRANSMISSION LINE SEGMENTS

Signal Detection, Measurement



Hardware Signal Path Design Integration

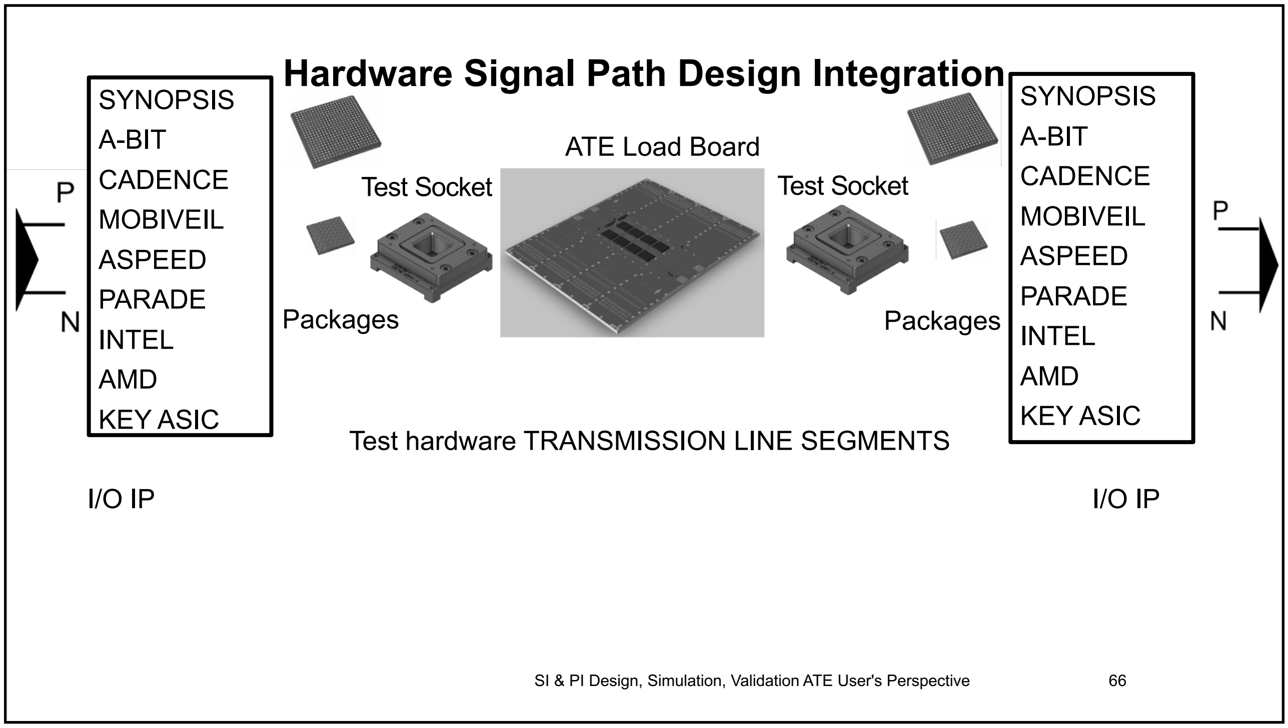
TX IBIS/SPICE Model
- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

RX IBIS/SPICE Model
- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

Test hardware TRANSMISSION LINE SEGMENTS

Format

Format



Hardware Signal Path Design Integration

SYNOPSIS
A-BIT
CADENCE
MOBIVEIL
ASPEED
PARADE
INTEL
AMD
KEY ASIC

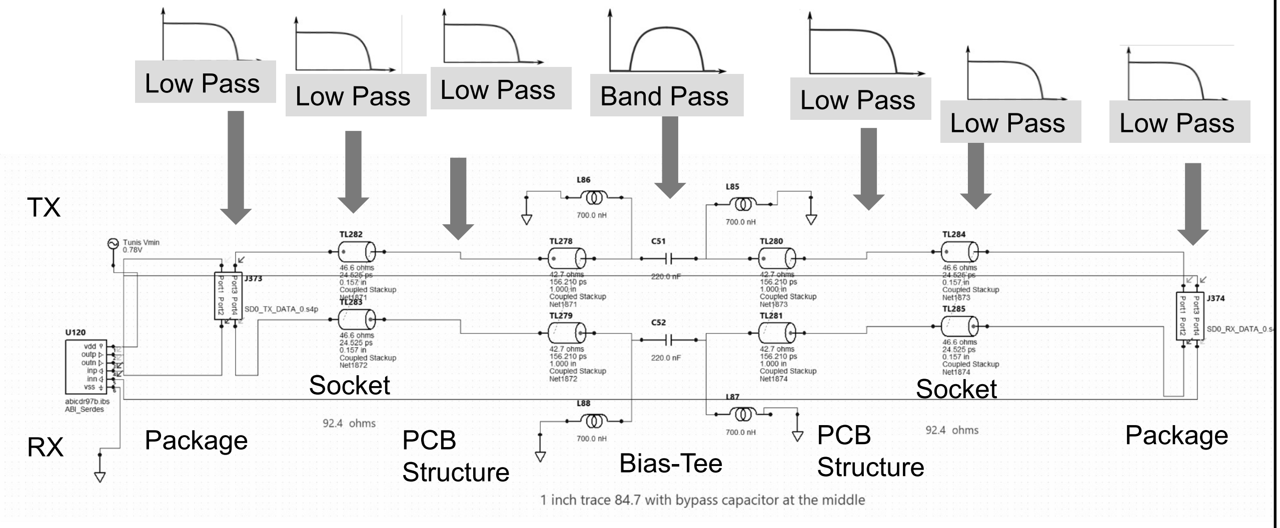
SYNOPSIS
A-BIT
CADENCE
MOBIVEIL
ASPEED
PARADE
INTEL
AMD
KEY ASIC

Test hardware TRANSMISSION LINE SEGMENTS

I/O IP

I/O IP

Integrated Filters; Merge of transmission line segments



1 inch trace 84.7 with bypass capacitor at the middle

ATE Hardware Transmission Line Parametric Design Guidelines

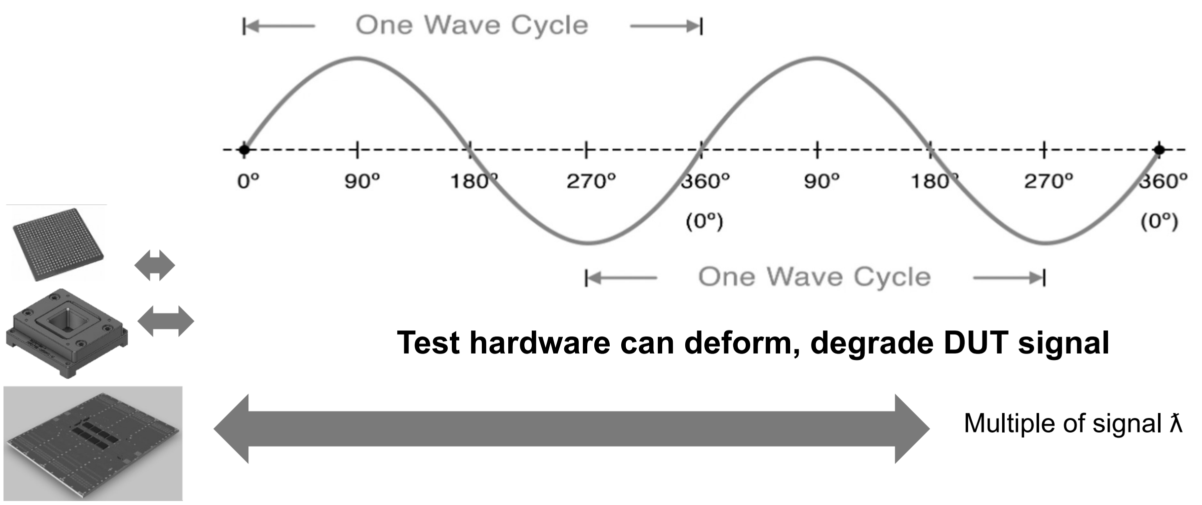
Design Guidelines

- IP Test Guide (e.g. PCIE GEN4)
  - From IP Providers
  - I/O Design
  - Application & Validation
- Electrical Design Rules
  - Frequency Domain S-Parameters
  - Time Domain : Impedance
- USE Case : Application Specific Requirements
  - ATE Board
  - Application Board

IP specific Data Rate & Impedance

IP Type	Model	Impedance (Diff) (Specifications)	Data Rate	Modeled, Simulated best results Impedance range
PCIE	T	85 Ω	16 Gbps	85 Ω to 90 Ω
DDR	T	80 Ω(40 Ω SE)	8 Gbps	90 Ω to 100 Ω
Ethernet	I/A	85 Ω 100 Ω	16 Gbps	85 Ω to 90 Ω
PCIE	I/A	85 Ω/100 Ω	10,16, 2.5 Gbps	85 Ω to 90 Ω)
USB3	I	90 Ω	10 Gbps	90 Ω
DDR	I/T/A	80 Ω (40 Ω SE)	4 Gbps	90 Ω to 100 Ω
PCIE	L/A	100 Ω 85 Ω	28,32,45 Gbps	85 Ω to 100 Ω
MIPI	L	100 Ω	11,20 Gbps	100 Ω

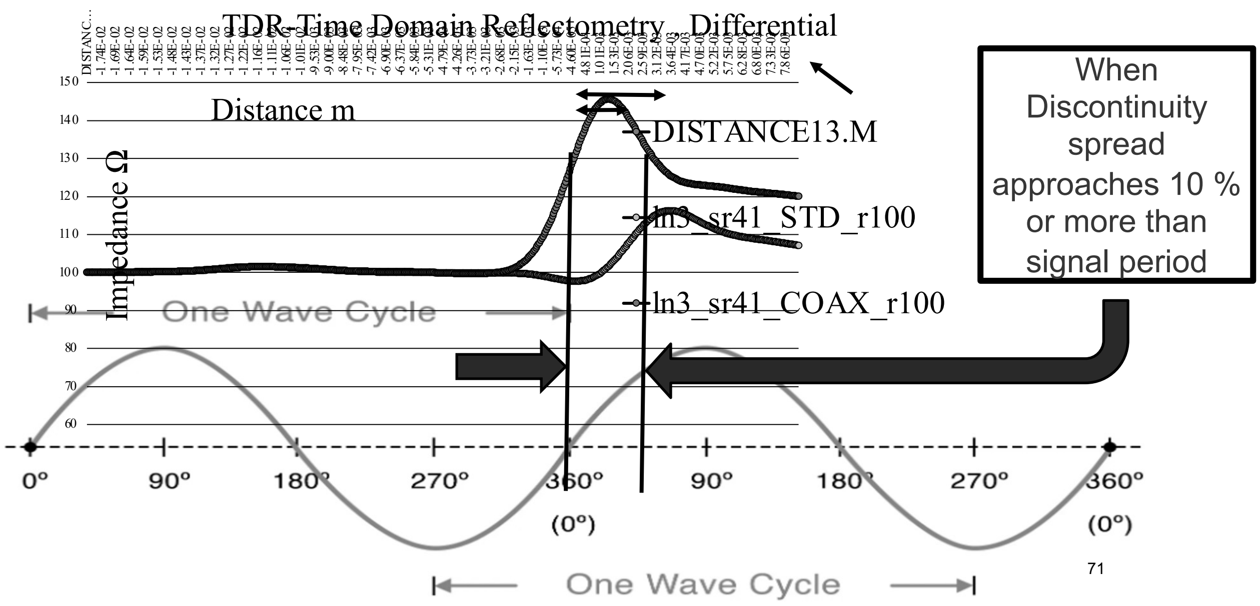
The TEST SIGNAL wavelength vs transmission line length path of test hardware



Test hardware can deform, degrade DUT signal

Multiple of signal ƛ

Impedance Anomalies- Discontinuities , When it matters ?



When Discontinuity spread approaches 10 % or more than signal period

Short wavelength signals to test hardware signal path physical dimension

IP Type	Model	Data Rate Gbps	λ (inches)	Period (ps)	Tr (ps)
PCIE	T	16	1.475	125.000	43.750
DDR	T	8	2.950	250.000	87.500
Ethernet	I/A	16	1.475	125.000	43.750
PCIE	I/A	10,16, 2.5	2.360	200.000(10G)	70.000
USB3	I	10	2.360	200.000	70.000
DDR	I/T/A	4	5.901	500.000	175.000
PCIE	L/A	28, 32, 45	(0.843), (0.738), (0.524)	71.429, 62.500, 44.444	25.000, 21.875, 15.556

- Board Thickness is 0.300” +.
- Shortest trace length per segment is 0.900”.
- Typical Pogo pin is 0.157”.
- The length, spread of impedance anomalies must be less than Tr (Rise Time) before PS SI problems arises “Dr. Bugatin’s SI, PI Integrity .”

ATE Test Hardware Design Challenges

- Multi-IP providers(e.g. Synopsis, Cadence, etc.) per device to device. With measurable performance differences even in compliance to similar industry, I/O standard (e.g. PCIE GEN4).
- Different process technology (e.g. 5nm, 16nm) as a function of I/O and associated IP.
- Complex PCB Load board design and structure
  - More layers 70 to 82+, with board thickness > 300 mils
  - IP specific Layers
  - Complex power and ground design
  - Noise Floor sensitivity of specific Ips
    - Digital Core
    - Analog, Mixed Signal

ATE Test Hardware Design Challenges

- IP Specific Impedances per layer
  - PCIE Layer : 80 to 90 Ω Differential Impedance
  - DDR5 Layer: 80 Ω Differential Impedance
  - USB Layer : 90 Ω Differential Impedance
  - UFS Layer : 100 Ω Differential Impedance
- The need to identify a common impedance that is not to compromise yield applicable to all IP.
- The possibility of needing a multi-impedance test socket as a function of IP and data rate.

IP modeling, simulation results with PRBS-31 for the complete signal path (Ip-package-socket-pcb)

IP Type	Model	Impedance (Diff) (Specifications)	Data Rate	Modeled, Simulated best results Impedance range (Ohms)	Point of Measurements
PCIE	T	85 Ohms	16G	(85Ohms)- 90 Ohms	External
DDR	T	80 Ohms(40 Ohms SE)	8G	90 Ohms to 100 Ohms	Internal
Ethernet	I	85 Ohms	16G	85 Ohms to (90 Ohms)	External
PCIE	I	85 Ohms	10G	85 Ohms to (90 Ohms)	External
USB3	I	90 Ohms	10G	90 Ohms	External
DDR	I	80 Ohms (40 Ohms SE)	4G	90 Ohms to 100 Ohms	Internal
PCIE	L	100 Ohms	28/32G	90 Ohms to 100 Ohms	External

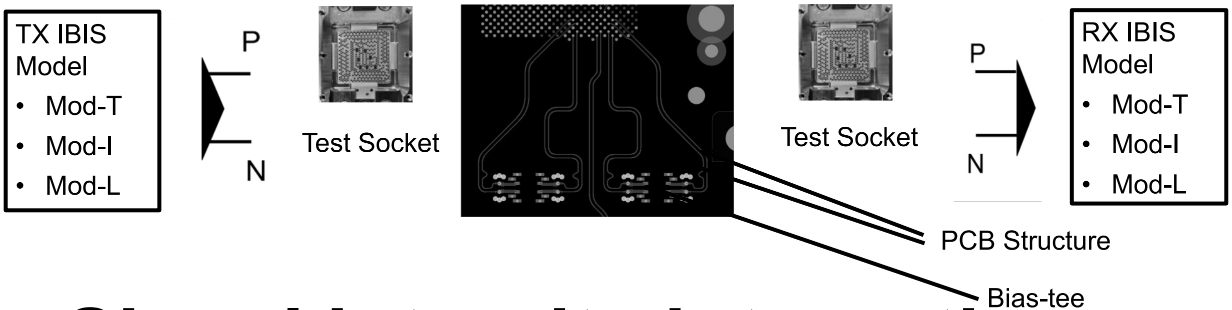
Over 160 circuit permutations modeled

What we learned from modeling and simulation results

SI-Design for SOC with IP Specific Impedance

Modeling and simulation results:

- Compliance to IP specific impedance provided the best results. Specifically for short-wavelength IPS.
- Model-T PCIE simulations indicated best performance at 90 Ohms vs the 85 Ohms recommended.
- Slower data rate or longer wavelength IPs can be made to operate at acceptable deviation with tolerable consequences (e.g. Model-I Ethernet from 85 Ohms to 90 Ohms)



TX IBIS Model
- Mod-T
- Mod-I
- Mod-L

P

N

Test Socket

Test Socket

P

N

RX IBIS Model
- Mod-T
- Mod-I
- Mod-L

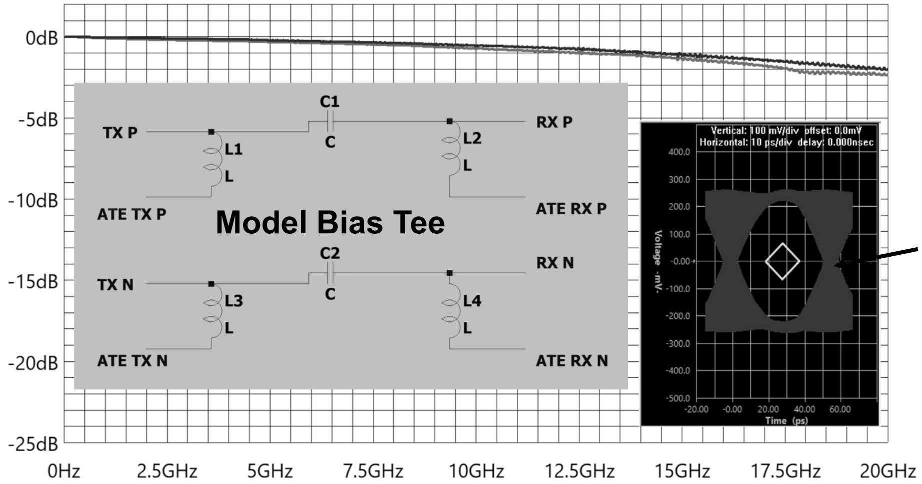
PCB Structure

Bias-tee

Signal integrity integration by segment

Model:Bias-Tee V3

S2D1 INSERTION LOSS



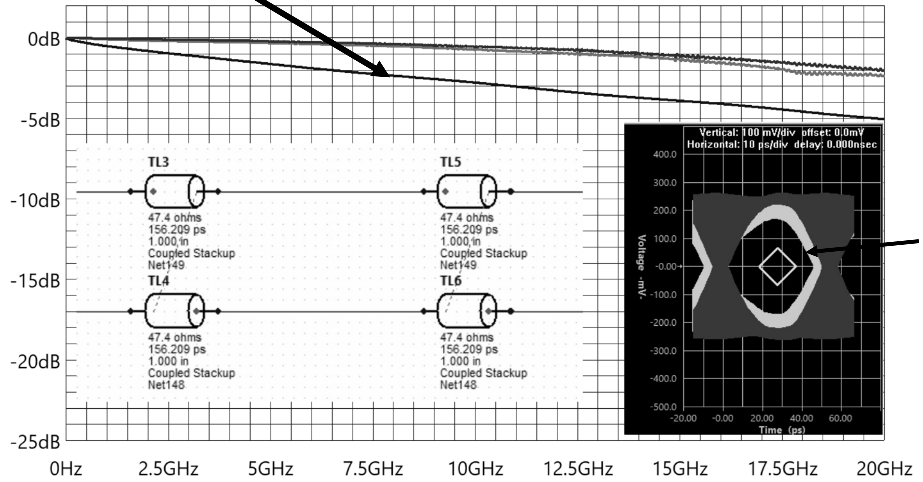
Date Eye

Model: Differential Trace 2x 1 inch 3 mils wide

D2D1 INSERTION LOSS

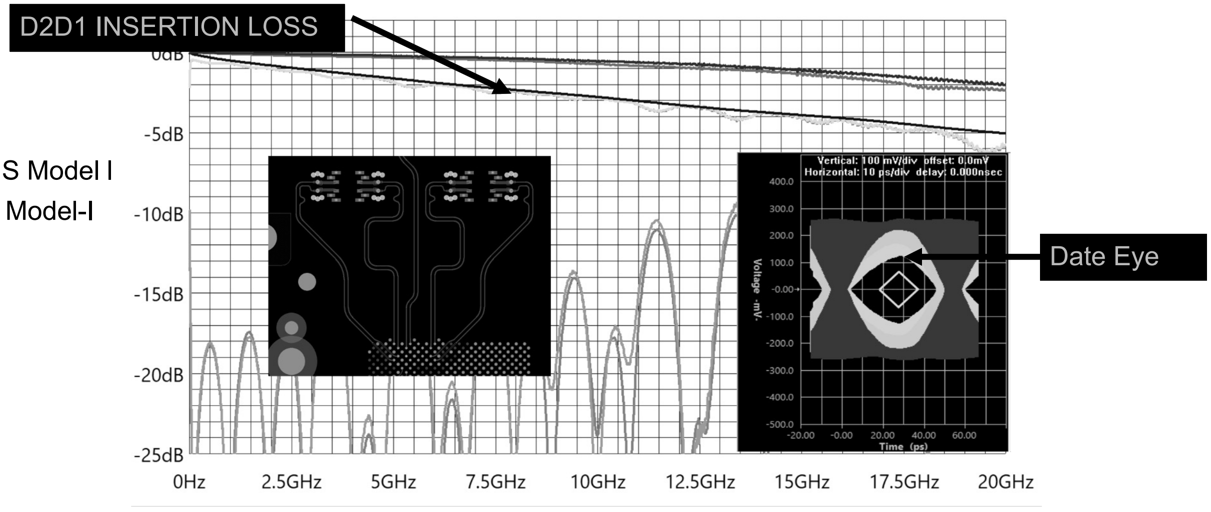
IBIS Model I

- Model-I



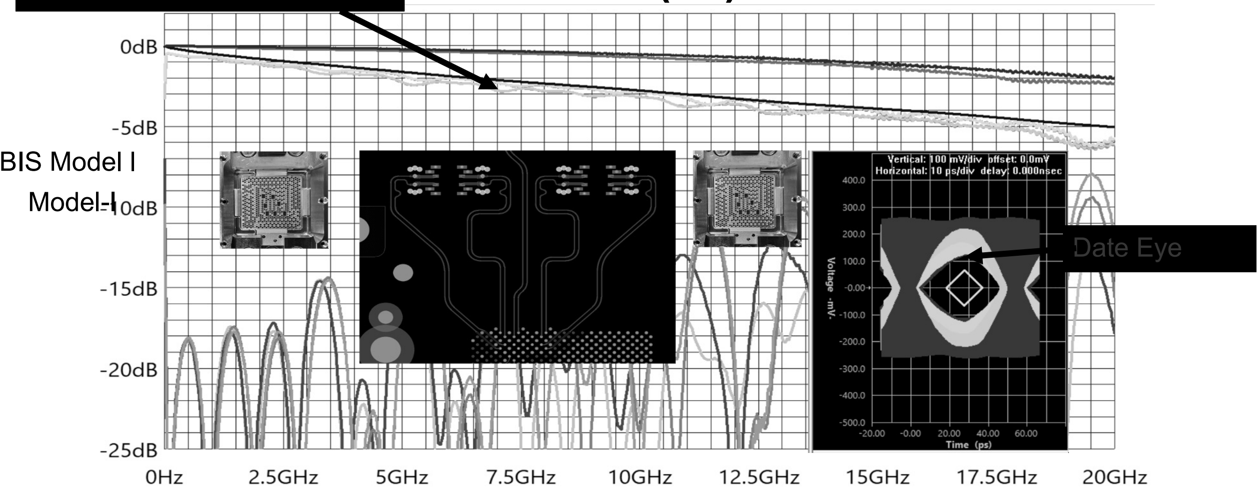
Date Eye

Model: Bias-Tee & Differential Trace 2x 1 inch



IBIS Model I
- Model-I

Model:Bias-Tee V3, Differential Trace(2x), Test Socket (2x)



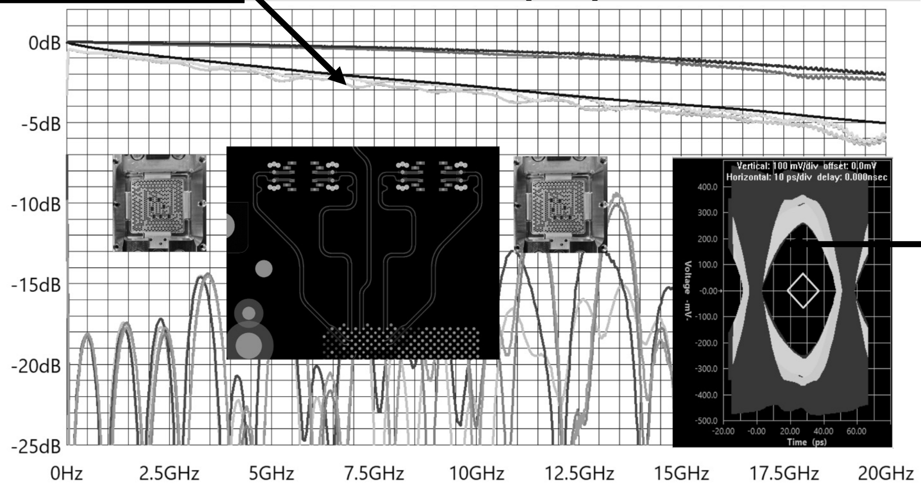
IBIS Model I
- Model-I

Signal integrity
same hardware different I/O
Ibis models

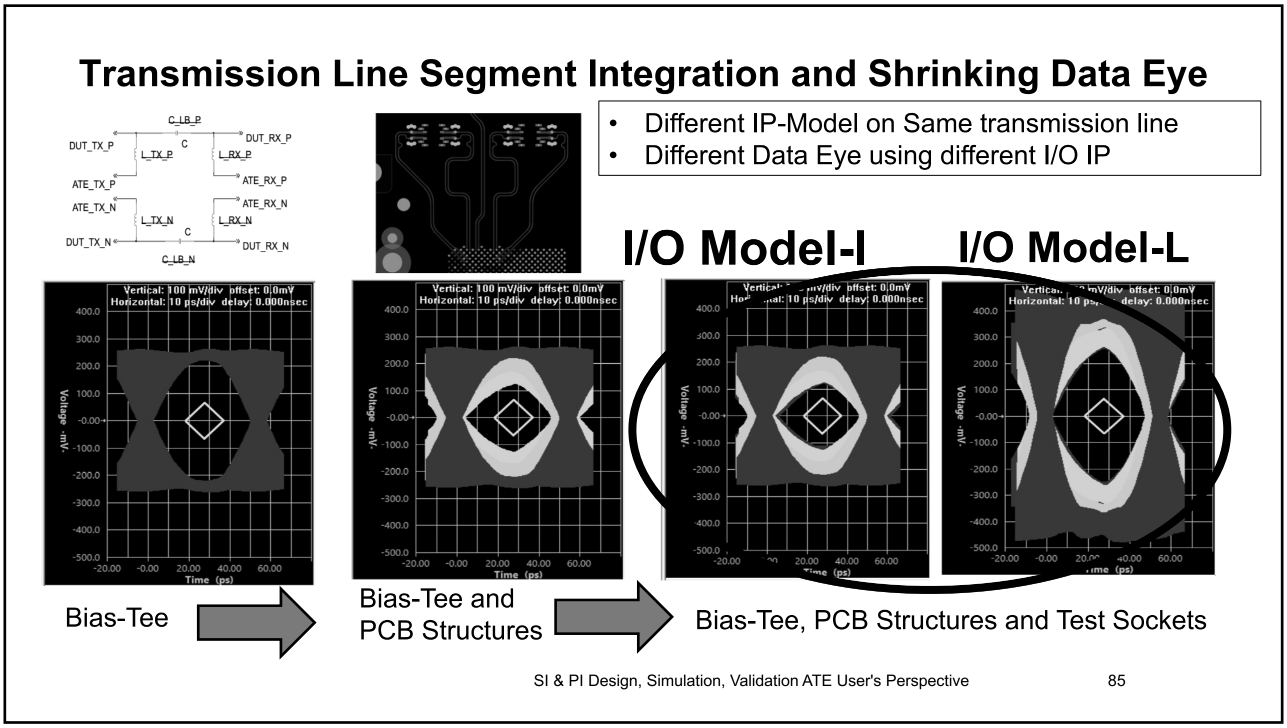
Model:Bias-Tee V4, Differential Trace(2x), Test Socket (2x)

D2D1 INSERTION LOSS

IBIS Model
- Model-T



Date Eye



Transmission Line Segment Integration and Shrinking Data Eye

- Different IP-Model on Same transmission line
- Different Data Eye using different I/O IP

I/O Model-I **I/O Model-L**

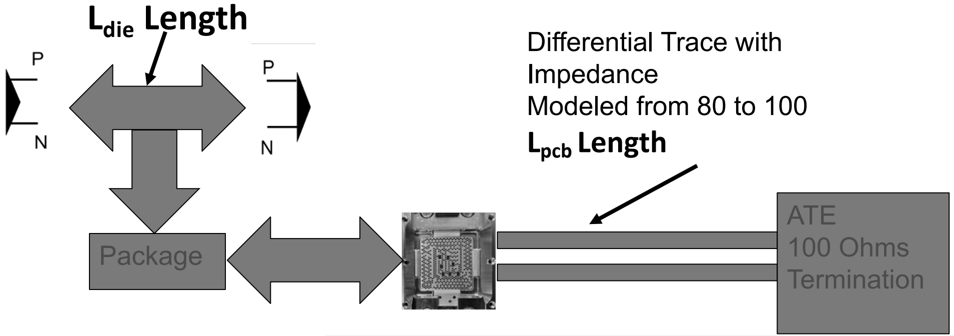
Bias-Tee → Bias-Tee and PCB Structures → Bias-Tee, PCB Structures and Test Sockets

ATE Transmission Line Segment(Filter) Integration

- Each segment has unique frequency and time domain characteristic.
- PCB Trace length is the biggest source of signal LOSS as a function of FREQUENCY and LENGTH.
- IP models from different providers are unique frequency domain and time domain characteristics. Can't be assume to produce similar performance given compliance to similar I/O Standard (e.g. PCIE Gen4, Gen5…etc.).
  - Different IP Providers (e.g. model I , T) compliant to similar I/O Standard are to result to different performance. Different Data-Eye.
  - It is not recommended to make assumption to expect similar performance
    - Similar use case
    - With different IP Provider - Model

DDR termination modeling, Simulation, Circuit Optimization.

DDR Simplified Model Representation In-die measurement (Model-Simulation)



L_{pcb} >>>> L_{die}

At signal wavelength of interest, The DDR data eye is dominated by the Impedance of the PCB trace, at 80 Ohms to 100 Ohms.

DDR Circuit Optimization

Design Consideration & Optimization

- Internal or IN-DIE Data-Eye measurement during test.
- External termination is required at the Package I/O pins.
- **Termination Impedance Optimization**
  - 80 Ω to 100 Ω vs Data-Eye Width and Amplitude
  - 5 GHz to 10 GHz
  - Data-Eye Width and Amplitude increase with Termination Impedance from >80 Ω to 95 Ω. Actual termination board impedance was set between 93 Ω and 95 Ω.
  - Three weeks of 24x7 modeling-simulation runs.

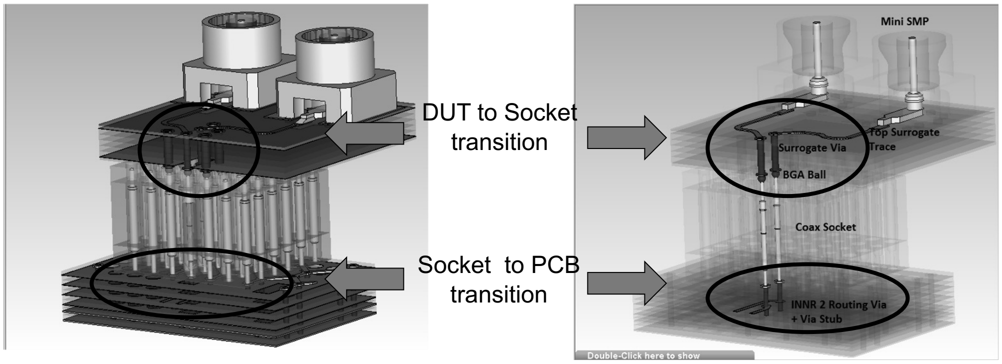
DDR Validation

DDR Data Eye Validation

- ATE Device IN-DIE measurements correlated with circuit simulation results.
- Validated on two Devices DDR implementation.

Complications, intricacies of test socket design and integration

Test Socket Integration Challenges

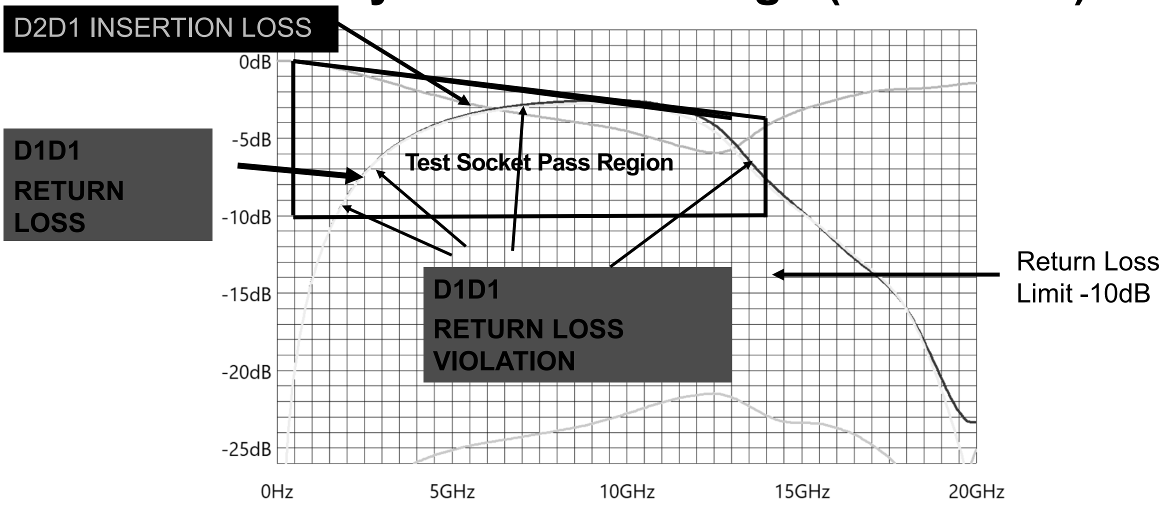


DUT to Socket transition

Socket to PCB transition

At 28+ Gbps, transition to/from socket as important as socket!!!

Low performance test socket (High return loss)
Poorly conceived design (Assumed!)



D2D1 INSERTION LOSS

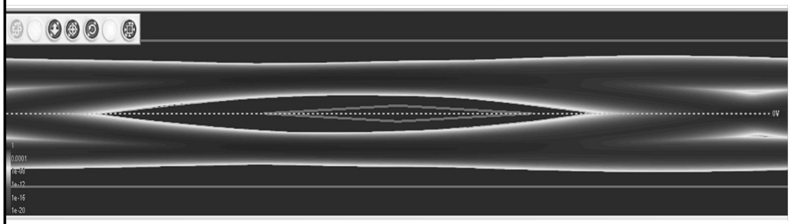
D1D1
RETURN LOSS

Test Socket Pass Region

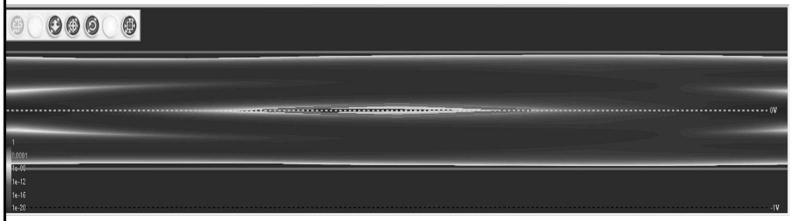
D1D1
RETURN LOSS VIOLATION

Return Loss
Limit -10dB

Low performance test socket (High return loss)
PRBS-31 @18G Data Eye

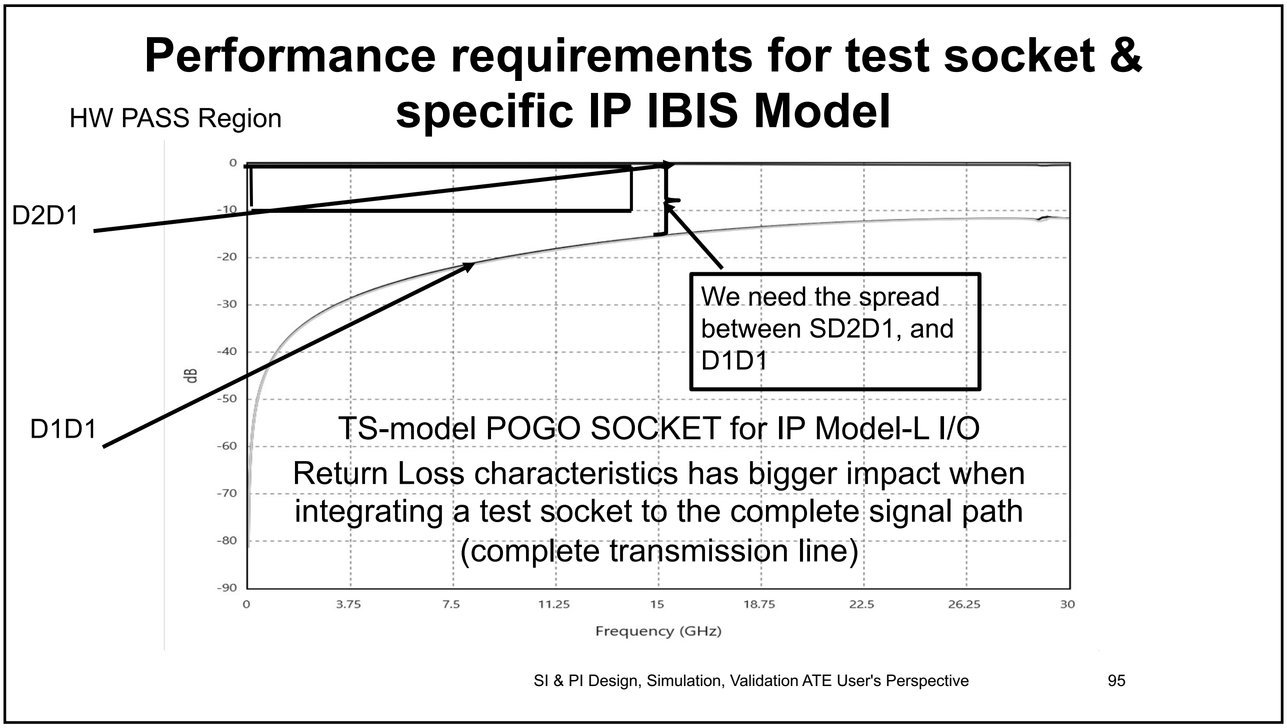


W/ Equalization
Barely Pass



Eyes Wide Shut

W/O
Equalization

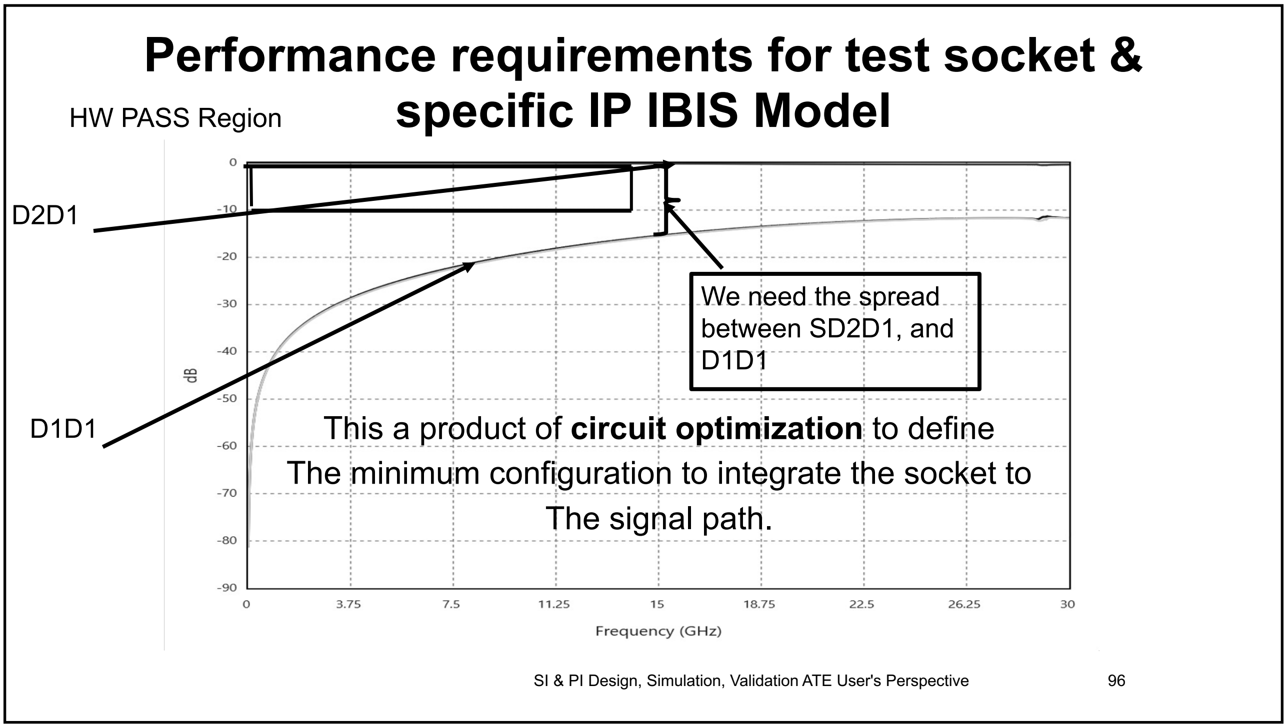


Performance requirements for test socket & specific IP IBIS Model

We need the spread between SD2D1, and D1D1

TS-model POGO SOCKET for IP Model-L I/O

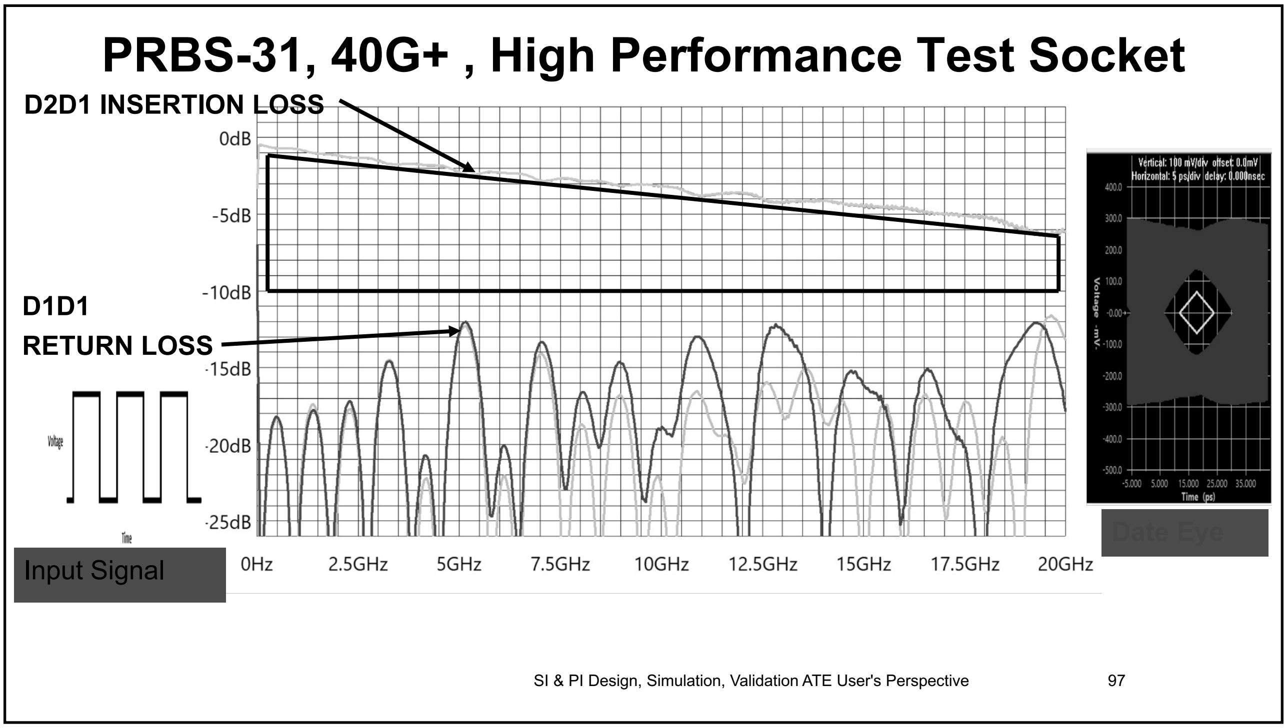
Return Loss characteristics has bigger impact when integrating a test socket to the complete signal path (complete transmission line)



Performance requirements for test socket & specific IP IBIS Model

We need the spread between SD2D1, and D1D1

This a product of **circuit optimization** to define
The minimum configuration to integrate the socket to
The signal path.



PRBS-31, 40G+ , High Performance Test Socket

SI-Design for SOC with IP Specific Impedance

Test Socket Summary, Comments:

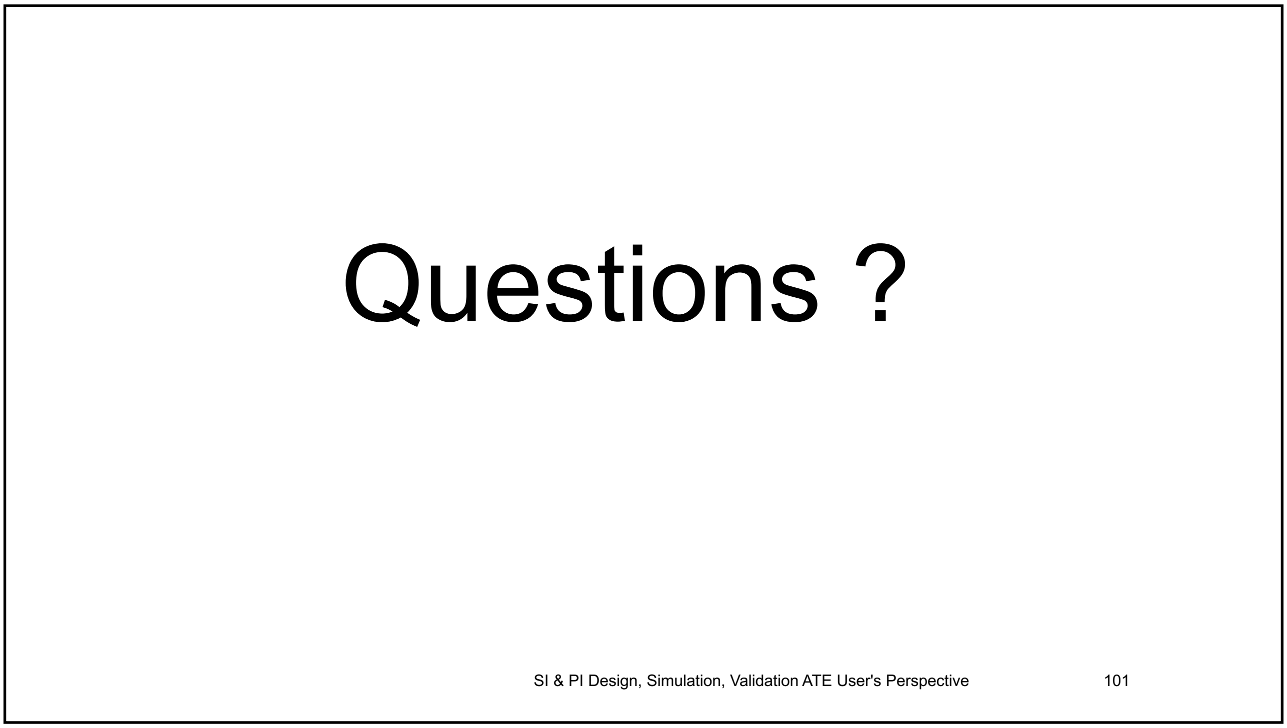
- There is a general lack of knowledge on the impact of test socket on the transmission line segment.
- The impact of contact-zones and its integration to the transmission line hardware is another less understood process in SI design.
- Test socket degrades as a function of insertion count. Design budget to account from Cycle=0 to Cycle=Replacement.
- Test Socket electrical parameters is recommended to be after complete circuit integration & optimization.

Critical Entities of Test Hardware Transmission Line Performance(Aside from geometries & dielectric)

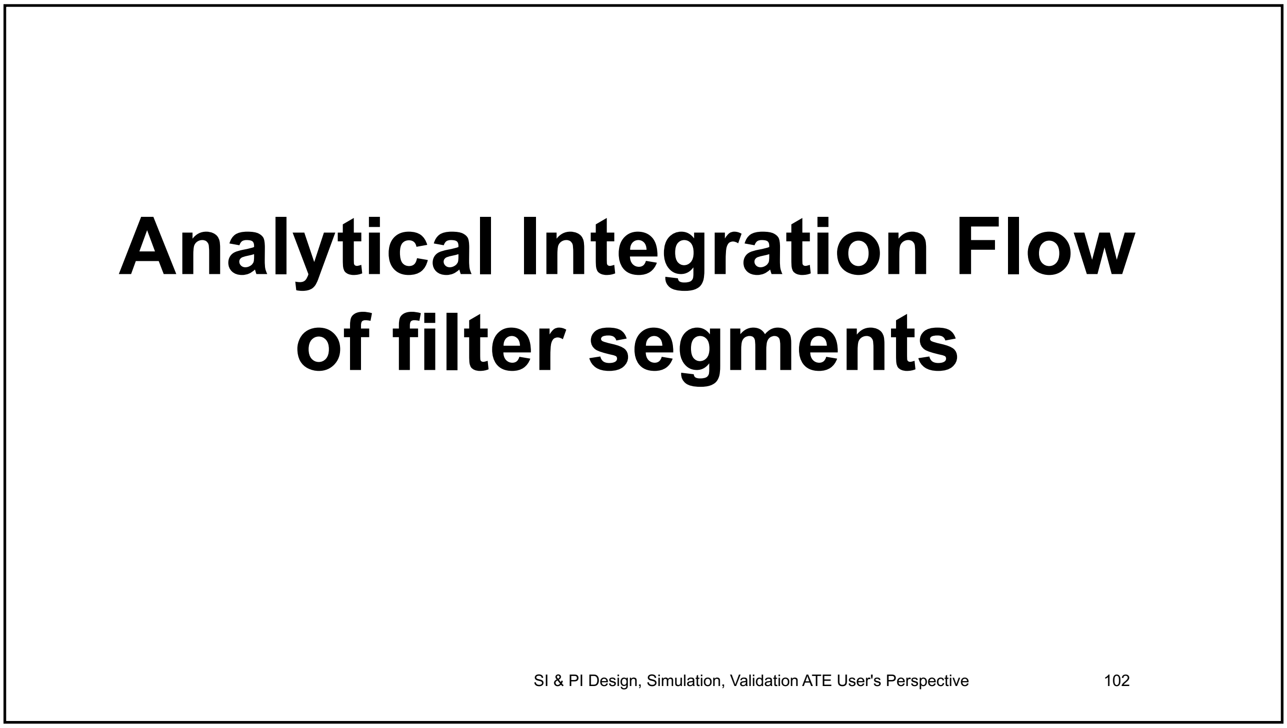
- IP Specific IBIS Models as a function of
  - I/O Standards, Technology
  - IP Provider
  - Geometry
- As function of wavelength discontinuity needs to be contained and managed for the entire signal path segment.
- Transition Zones between signal segments are common source of discontinuity.

Critical Entities of Test Hardware Transmission Line Performance(Aside from geometries & dielectric)

- IP Specific Impedance on a single SOC is here and future of SOC Products.
- One size fits all impedance is less applicable with increasing data-rate (shorter wavelength)
- IP I/O Models as function of technology, IP providers have profound impact on the data-eye after transmission line.
- Test Socket design and SI-Integration is an area for improvement.



Questions ?



Analytical Integration Flow of filter segments

Start

Define Device Performance Requirement & I/O

Define Frequency & Time Domain Parameters

IP Type	Model	Impedance (Diff) (Specifications)	Data Rate
PCIE	T	85 Ω	16 Gbps
DDR	T	80 Ω(40 Ω SE)	8 Gbps
Ethernet	I/A	85 Ω 100 Ω	16 Gbps
PCIE	I/A	85 Ω/100 Ω	10,16, 2.5 Gbps
USB3	I	90 Ω	10 Gbps
DDR	I/T/A	80 Ω (40 Ω SE)	4 Gbps
PCIE	L/A	100 Ω 85 Ω	28,32,45 Gbps
MIPI	L	100 Ω	11,20 Gbps

Start

Define Device Performance Requirement & I/O

Define Frequency & Time Domain Parameters

Identify, rank I/O parameters

IP Type	Model	Impedance (Diff) (Specifications)	Data Rate
PCIE	L/A	100 Ω 85 Ω	28,32,45 Gbps
MIPI	L	100 Ω	11,20 Gbps
PCIE	I/A	85 Ω/100 Ω	10,16, 2.5 Gbps
PCIE	T	85 Ω	16 Gbps
Ethernet	I/A	85 Ω 100 Ω	16 Gbps
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PCIE	I/A	85 Ω/100 Ω	10,16, 2.5 Gbps
PCIE	T	85 Ω	16 Gbps
Ethernet	I/A	85 Ω 100 Ω	16 Gbps
USB3	I	90 Ω	10 Gbps
DDR	T	80 Ω(40 Ω SE)	8, 4 Gbps

- Highest data rate
- Impedance Range 85Ω to 100Ω
- USB3 has always been 90Ω
- DDR has the lowest Impedance at 80Ω
- DDR has the highest pin count or number of pins

Impedance requirement spread of 80Ω to 100Ω

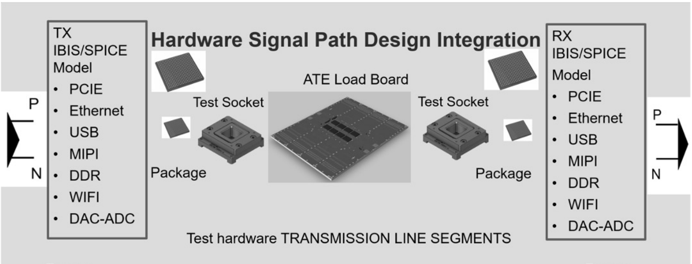
Start

Define Device Performance Requirement & I/O

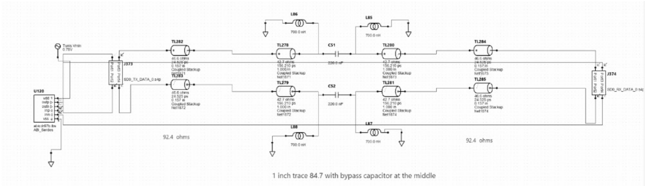
Define Frequency & Time Domain Parameters

Identify, rank I/O parameters

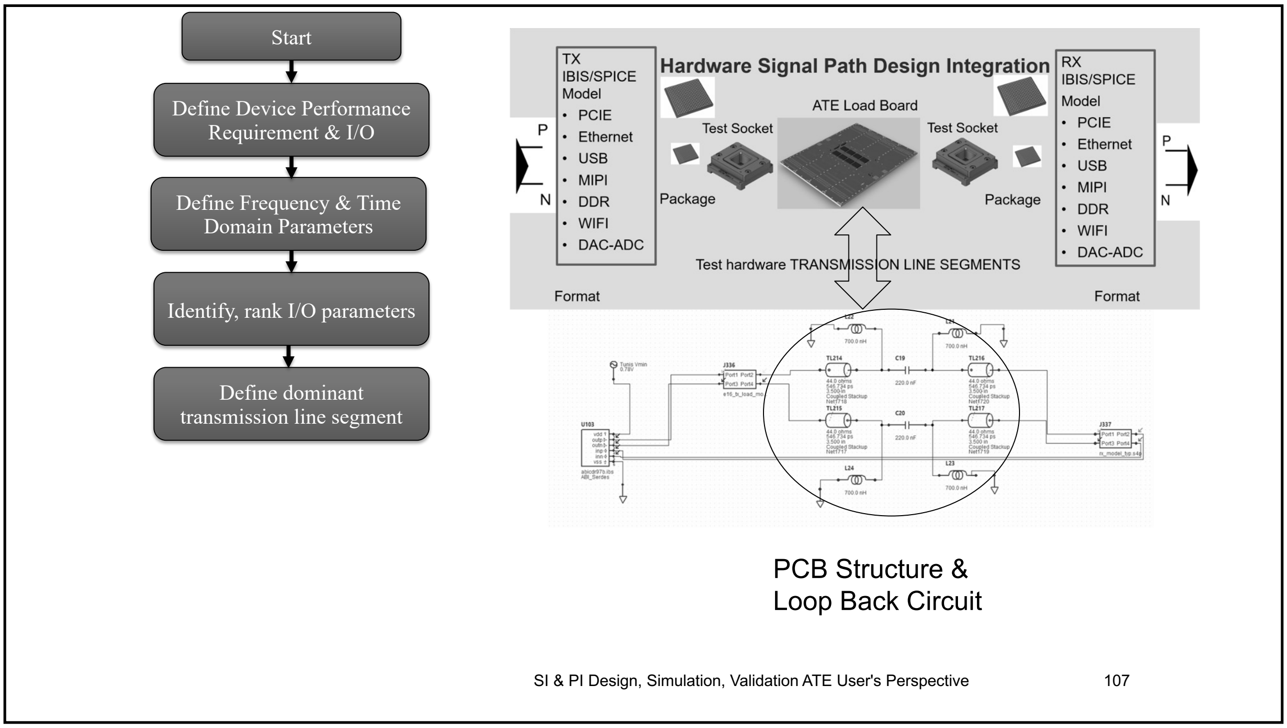
Define dominant transmission line segment



Physical Hardware



Electrical Model 3D Structures



Start

Define Device Performance Requirement & I/O

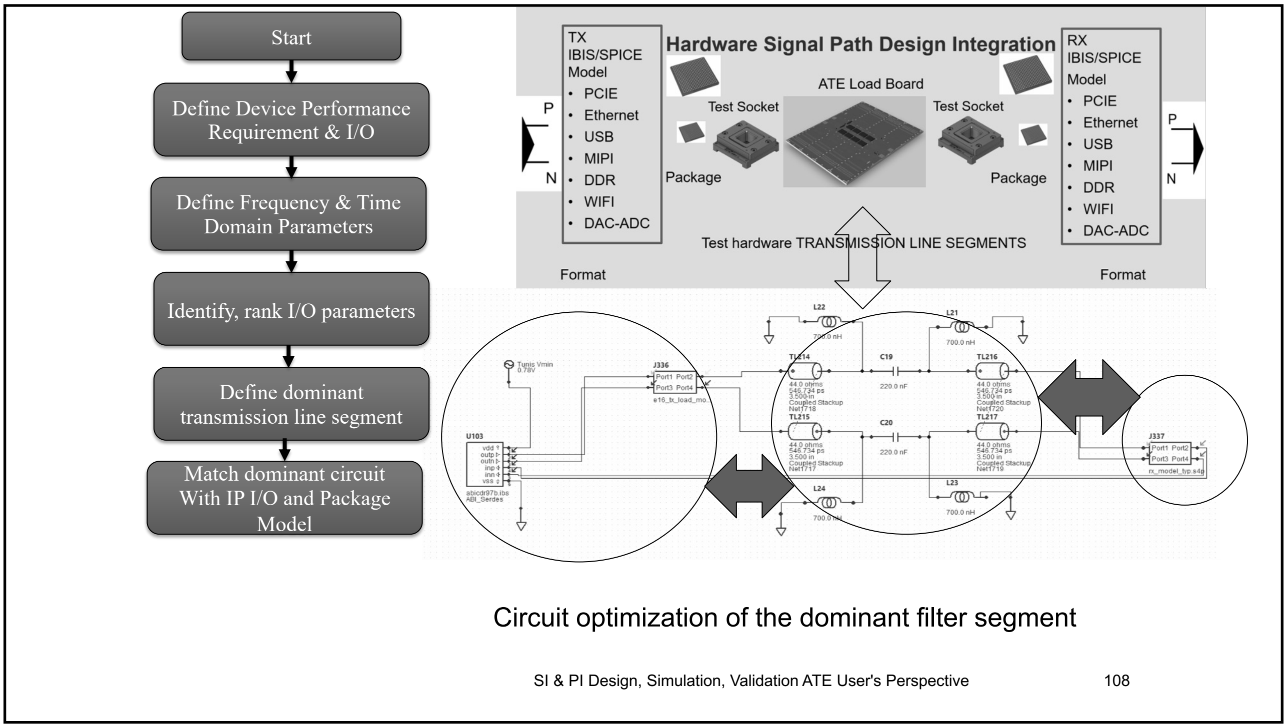
Define Frequency & Time Domain Parameters

Identify, rank I/O parameters

Define dominant transmission line segment

PCB Structure & Loop Back Circuit

SI & PI Design, Simulation, Validation ATE User's Perspective 107



Start

Define Device Performance Requirement & I/O

Define Frequency & Time Domain Parameters

Identify, rank I/O parameters

Define dominant transmission line segment

Match dominant circuit With IP I/O and Package Model

Circuit optimization of the dominant filter segment

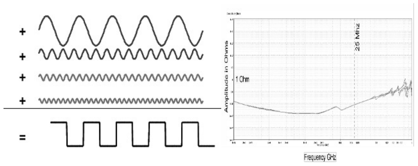
SI & PI Design, Simulation, Validation ATE User's Perspective 108

Questions ?

Transmission Line Segment Circuit Optimization

TestConX™

Mesa, Arizona ● March 1–4, 2026



Circuit Optimization

- I/O PCIE Gen-4
- Test pattern PRBS-31
- Test rate or Data Rate = 18G
- Equalization = Disabled
- DFE : Decision Feedback Equalization = 8
- CLTE : Continuous Linear Test Equalization = Enabled
- Impedance Sweep: 75Ω to 95Ω
- Test Parameter
  - Data Eye Width
  - Date Amplitude

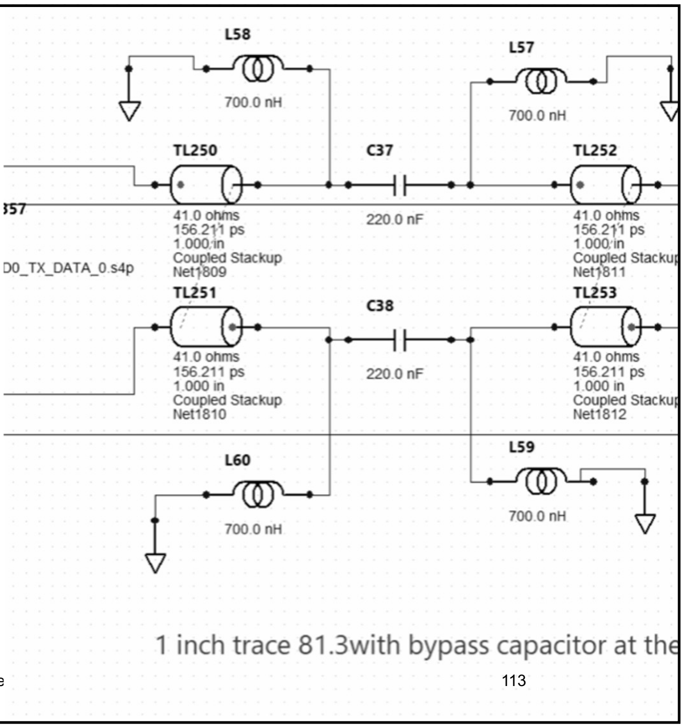
Circuit Optimization

EDA Tools of the trade

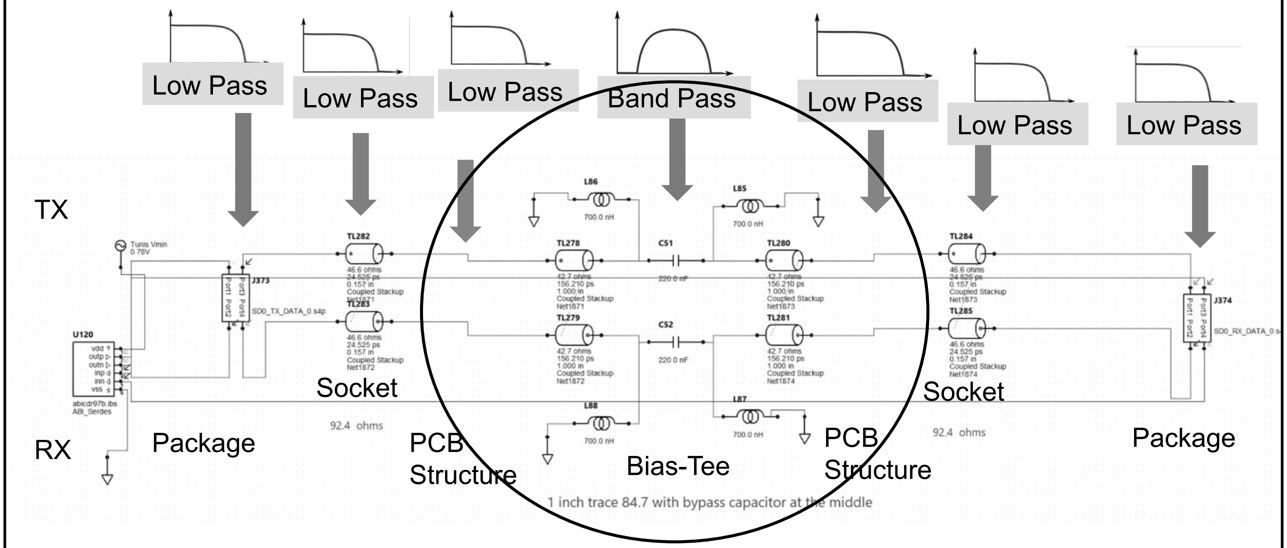
- 3D Modeling
  - HFSS
  - Clarity
  - ADS
  - Hyperlynx
- Integration
  - Hyperlynx
  - ADS
  - Matlab
  - Sigrity

IMPEDANCE SWEEP

Circuit Optimization



Integrated Filters; Merge of transmission line segments

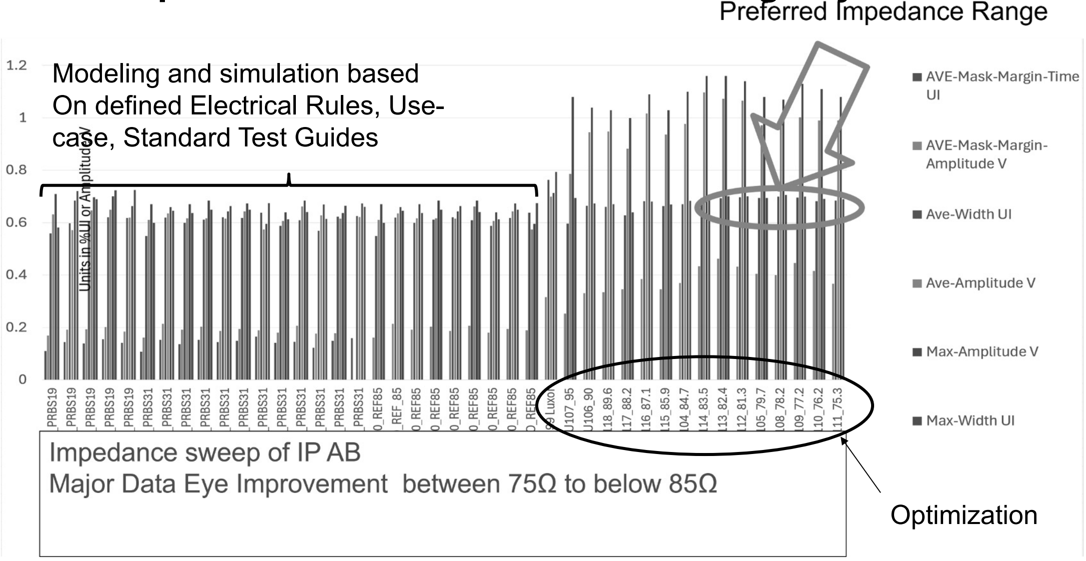


Impedance Ω	EQUAL	DFE	CTLE	PRBS-18G	AVE WITDH UI
75.3	DISABLED	8	ENABLED	31	0.68434
76.2	DISABLED	8	ENABLED	31	0.6822381
77.2	DISABLED	8	ENABLED	31	0.695934
78.2	DISABLED	8	ENABLED	31	0.700082
79.7	DISABLED	8	ENABLED	31	0.694472
81.3	DISABLED	8	ENABLED	31	0.696682
82.4	DISABLED	8	ENABLED	31	0.693272
83.5	DISABLED	8	ENABLED	31	0.694203
84.7	DISABLED	8	ENABLED	31	0.67063
85.9	DISABLED	8	ENABLED	31	0.662831
87.1	DISABLED	8	ENABLED	31	0.681367
88.2	DISABLED	8	ENABLED	31	0.628318
89.6	DISABLED	8	ENABLED	31	0.661124
90.0	DISABLED	8	ENABLED	31	0.664665

Load Board IMPEDANCE SWEEP

- Loop Back Circuit adjusted to 80 Ω +5, -5Ω.
- Load Board model is now 80 Ω.
- Original setting 85 Ω.
- Focus, priority on Data Eye Width.
- Data-Eye Mask violation 99%+ related to Data Eye Width.
- Flat or consistent response between 75.0 Ω and below 85.0 Ω.
- Lowest DFE value to pass 18G, PRBS-31 is 8 (T-Socket).
- IP Specific or Unique case

Impedance Profile – Focus on Average Eye Width

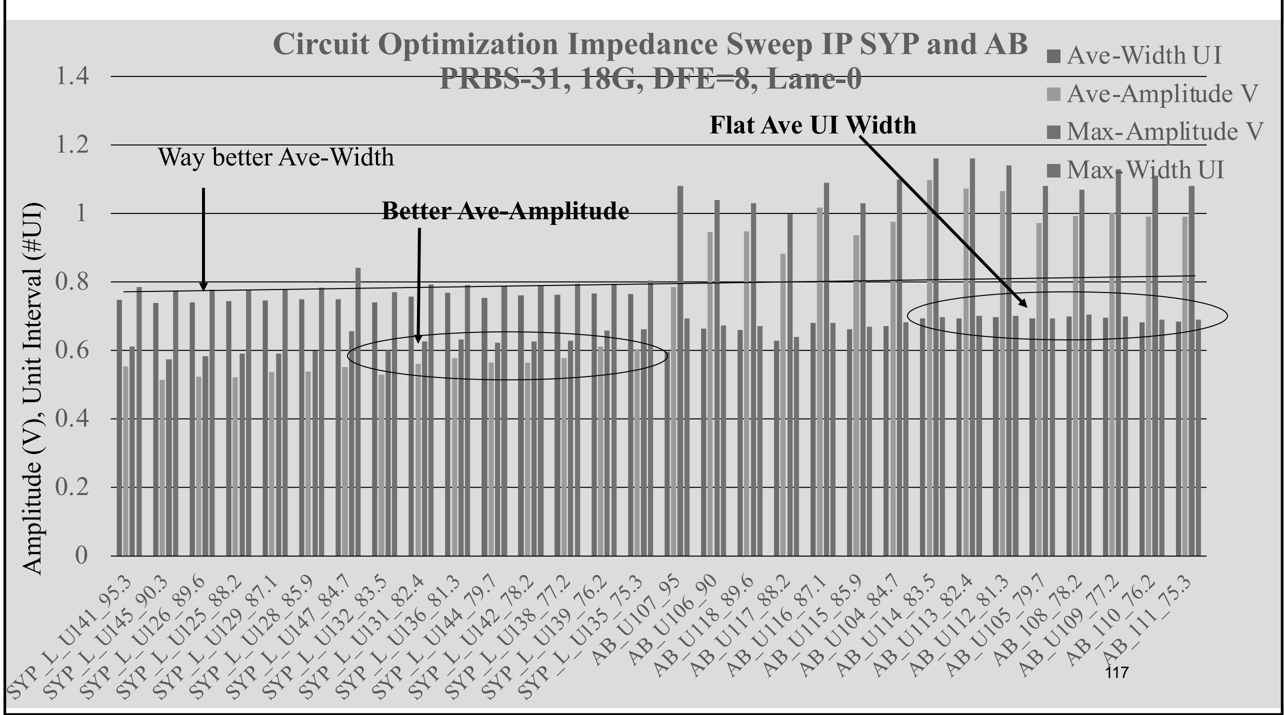


Preferred Impedance Range

Modeling and simulation based On defined Electrical Rules, Use-case, Standard Test Guides

Impedance sweep of IP AB
Major Data Eye Improvement between 75Ω to below 85Ω

Optimization

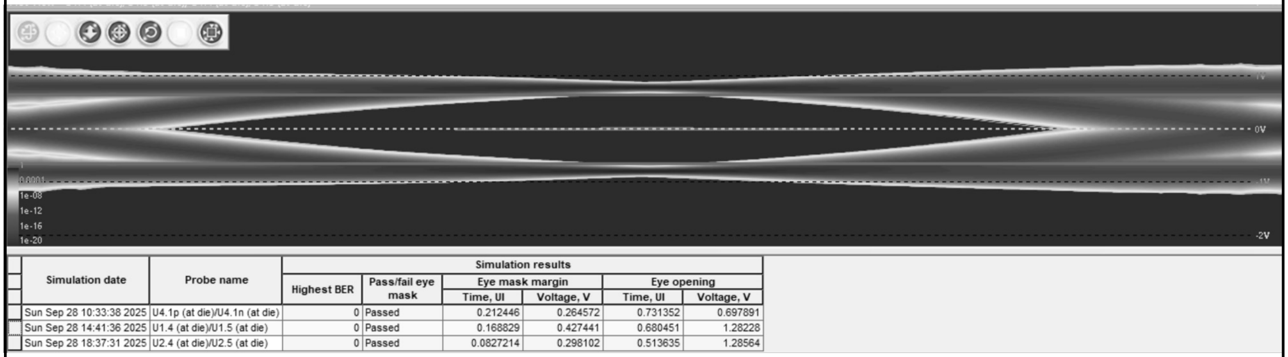


Circuit Optimization Impedance Sweep on the same loop back circuit

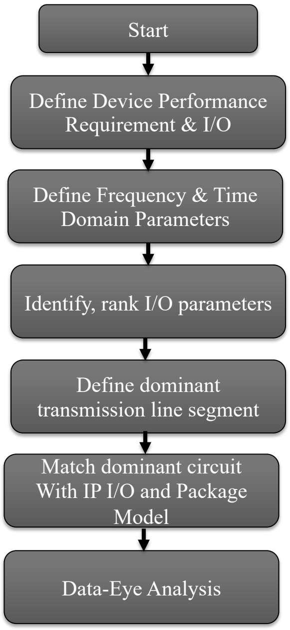
IP PCIE	IP Spec Impedance (Ω)	E-Design Rules (Ω)	Optimization results (Ω)	Critical Parameters	Equalization	DFE	CTLE
AB	85	85	80	Ave UI Width	NA	8	Enabled
SYP	85	85	80	Date Eye Amplitude is challenged or limited	NA	8	Enabled
FS	100	100	93-95	No peculiarities No Pre or Post Signal Processing needed	NA	NA	NA

- Optimization is highly recommended other than following default values.
- Transmission line performance is influenced by key factors (e.g. IP, Package, Circuits)
- Transmission line segment integration is needed to confirm compatibility of the complete circuit.

PCIE , 18G, DUT Package, Trace Impedance 80 Ohms DFE=64



Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Sun Sep 28 10:33:38 2025	U4.1p (at die)/U4.1n (at die)	0	Passed	0.212446	0.264572	0.731352	0.697891
Sun Sep 28 14:41:36 2025	U1.4 (at die)/U1.5 (at die)	0	Passed	0.168829	0.427441	0.680451	1.28228
Sun Sep 28 18:37:31 2025	U2.4 (at die)/U2.5 (at die)	0	Passed	0.0827214	0.298102	0.513635	1.28564


Start

Define Device Performance Requirement & I/O

Define Frequency & Time Domain Parameters

Identify, rank I/O parameters

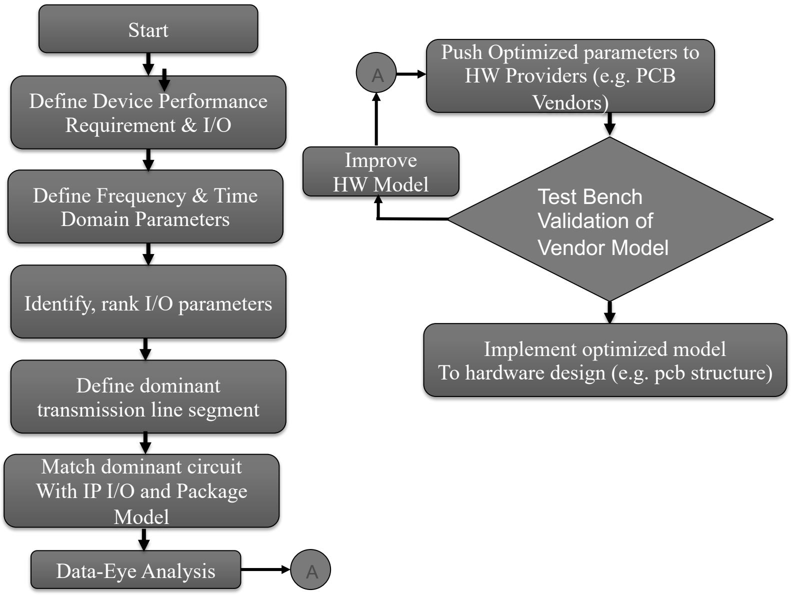
Define dominant transmission line segment

Match dominant circuit With IP I/O and Package Model

Data-Eye Analysis

Data Eye Analysis

- No assumption and or guess work. Use Data from simulation results.
- Look for definitive unique performance gain that stands out.
- Look for consistency among on Data-Eye Parameters.
- Optimize circuits
  - Per I/O Type
  - Per I/O models-provider
- Identify potential common parameter range (e.g. I/O impedance) applicable to most if not all I/O technology to simplify hardware design.



Start

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Data-Eye Analysis

A

A

Push Optimized parameters to HW Providers (e.g. PCB Vendors)

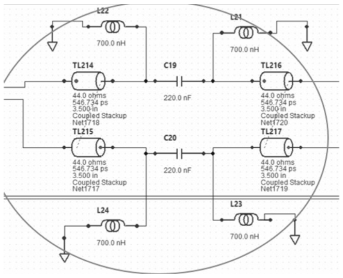
Test Bench Validation of Vendor Model

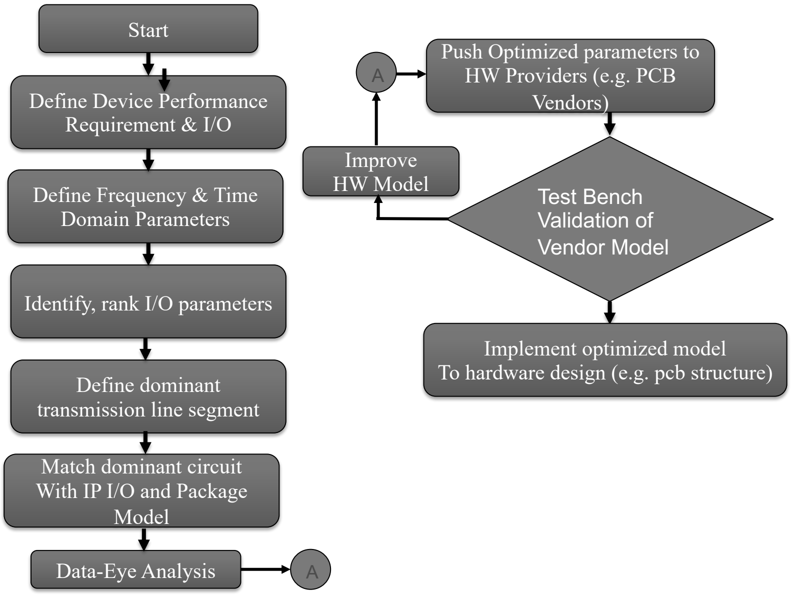
Improve HW Model

Implement optimized model To hardware design (e.g. pcb structure)

PCB Model Adjustment to optimized parameters

Cross check adjusted HW model to test-bench to match Data Eye Results





Start

Define Device Performance Requirement & I/O

Define Frequency & Time Domain Parameters

Identify, rank I/O parameters

Define dominant transmission line segment

Match dominant circuit With IP I/O and Package Model

Data-Eye Analysis

A

A

Push Optimized parameters to HW Providers (e.g. PCB Vendors)

Test Bench Validation of Vendor Model

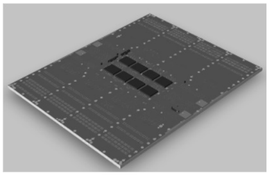
Improve HW Model

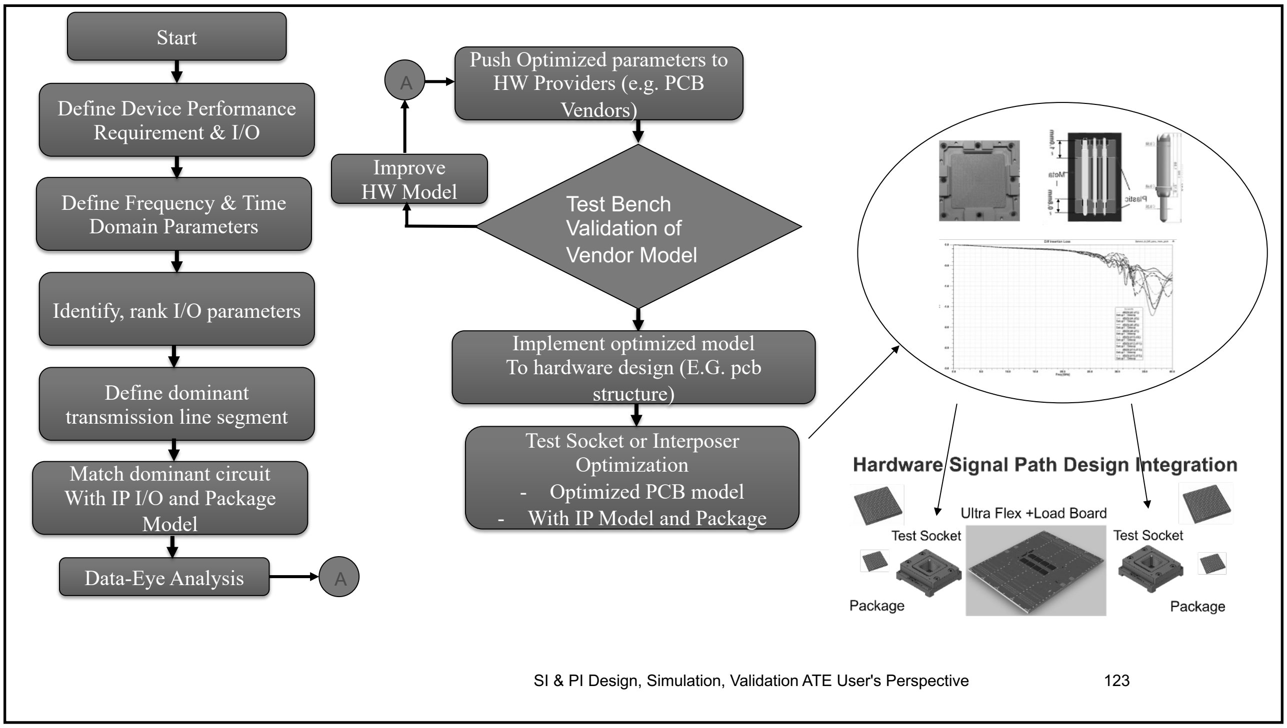
Implement optimized model To hardware design (e.g. pcb structure)

PCB Model Adjustment to optimized parameters

Cross check adjusted HW model to test-bench to match Data Eye Results

Update design files to reflect optimize transmission line parameter





Start

Define Device Performance Requirement & I/O

Define Frequency & Time Domain Parameters

Identify, rank I/O parameters

Define dominant transmission line segment

Match dominant circuit With IP I/O and Package Model

Data-Eye Analysis

Improve HW Model

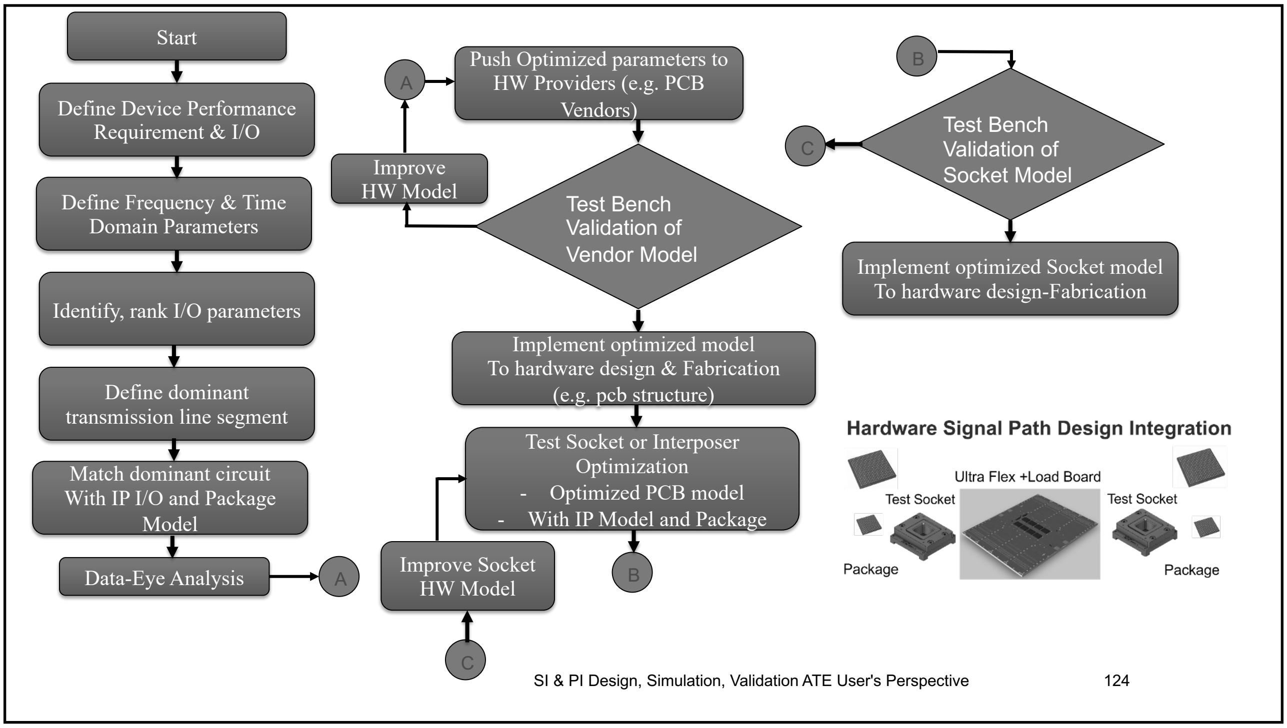
Push Optimized parameters to HW Providers (e.g. PCB Vendors)

Test Bench Validation of Vendor Model

Implement optimized model To hardware design (E.G. pcb structure)

Test Socket or Interposer Optimization
- Optimized PCB model
- With IP Model and Package

Hardware Signal Path Design Integration



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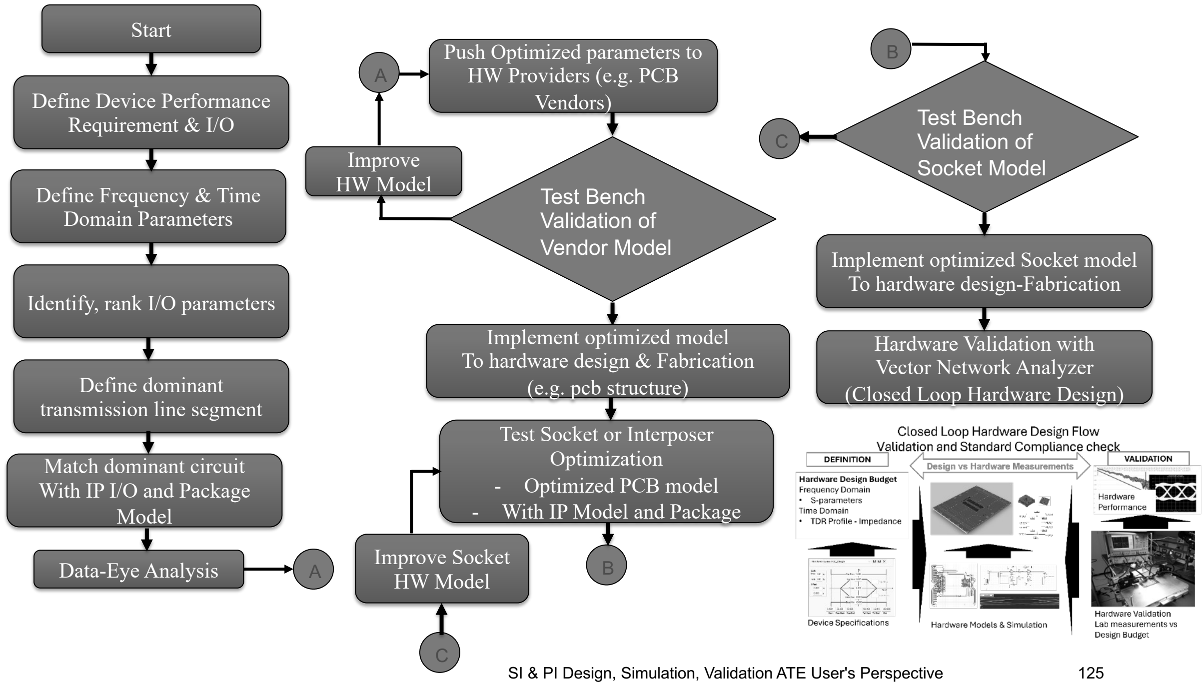
Improve Socket HW Model

Test Bench Validation of Socket Model

Implement optimized Socket model To hardware design-Fabrication

Hardware Signal Path Design Integration



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A

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- With IP Model and Package

Improve Socket HW Model

B

C

Test Bench Validation of Socket Model

Implement optimized Socket model To hardware design-Fabrication

Hardware Validation with Vector Network Analyzer (Closed Loop Hardware Design)

Circuit Optimization Summary

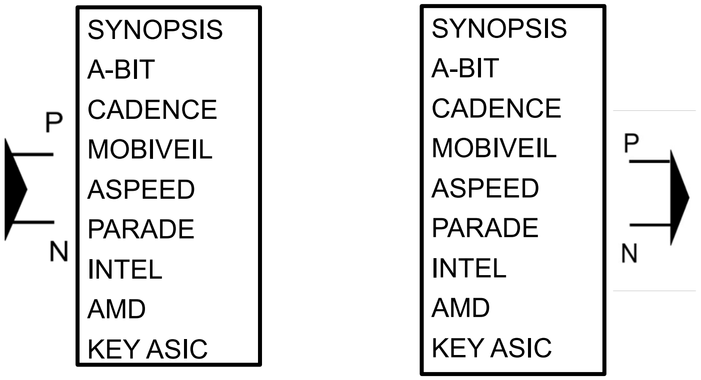
Critical to circuit optimization

- IP models for Drivers & Receivers.
- Clear definition of HW Design Budget.
  - Clear definition of performance target in frequency and time domain.
  - Clear definition of performance guard band.
- IP 3D and or frequency models of HW providers (e.g. PCB, Test Socket, Components, Support circuits).
- Closed Loop Hardware validation strategy

Circuit Optimization Summary

Critical to circuit optimization

- IP IBIS models for Drivers & Receivers. NOT GENERIC IBIS MODELS



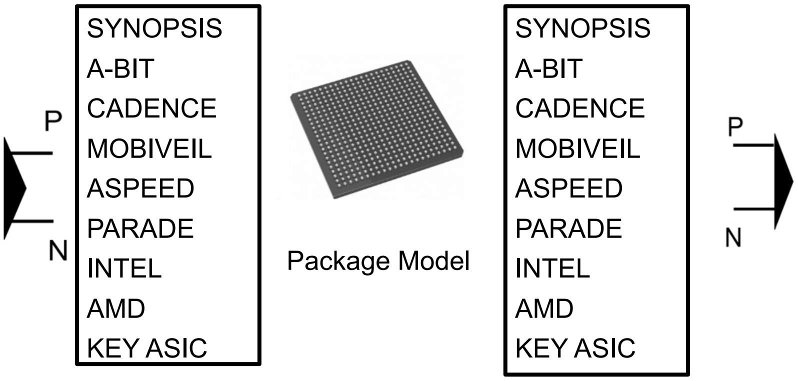
SYNOPSIS
A-BIT
CADENCE
MOBIVEIL
ASPEED
PARADE
INTEL
AMD
KEY ASIC

SYNOPSIS
A-BIT
CADENCE
MOBIVEIL
ASPEED
PARADE
INTEL
AMD
KEY ASIC

Circuit Optimization Summary

Critical to circuit optimization

- IP models for Drivers & Receivers and Associated Package



SYNOPSIS
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ASPEED
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INTEL
AMD
KEY ASIC

Package Model

SYNOPSIS
A-BIT
CADENCE
MOBIVEIL
ASPEED
PARADE
INTEL
AMD
KEY ASIC

Circuit Optimization Summary

Critical to circuit optimization

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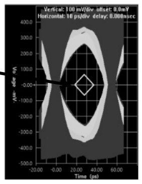
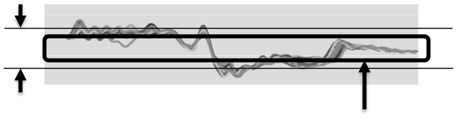
  - Clear definition of performance target in frequency and time domain.
  - Clear definition of performance guard band.

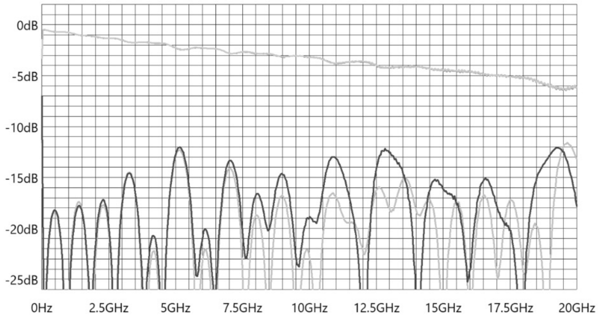
Data Eye Mask Guard Band



10Ω Impedance Spread



Device Impedance Range



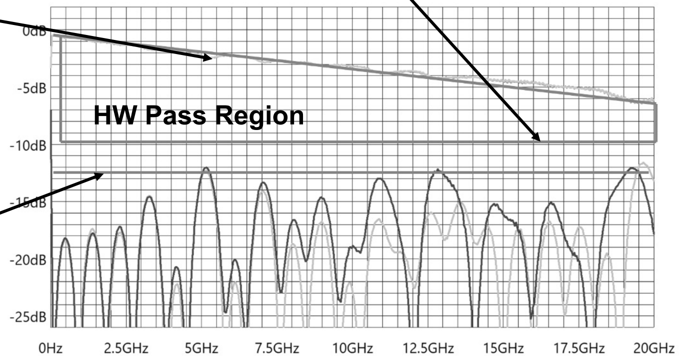
Circuit Optimization : HW Design Budget

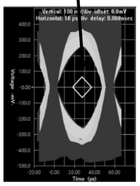
Loss Curve Slope
- PCB Trace Length
- Dielectric
- Geometry (W-H)
- Loss / (Length-Frequency)

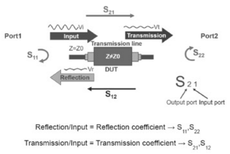
Hardware Guard Band

Return Loss HW Limit

Data Eye Mask Guard Band







Reflection/Input = Reflection coefficient → S_{11},S_{22}

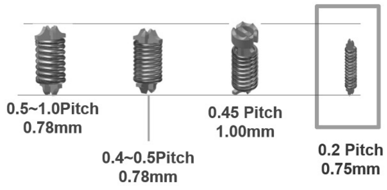
Transmission/Input = Transmission coefficient → S_{21},S_{12}

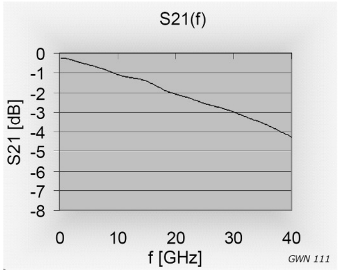
There is no guess work or assumption
Analytically Defined Design Budget

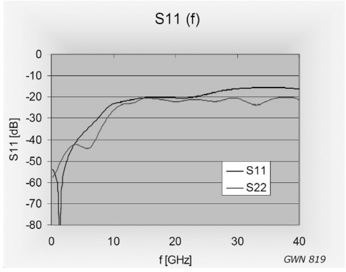
Circuit Optimization Summary

Critical to circuit optimization

- IP 3D and or frequency models of HW providers (Test Socket).





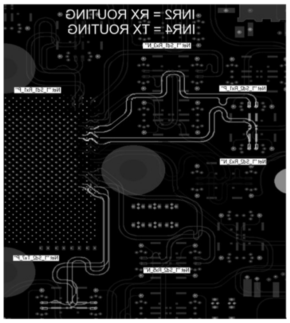


Circuit Optimization Summary

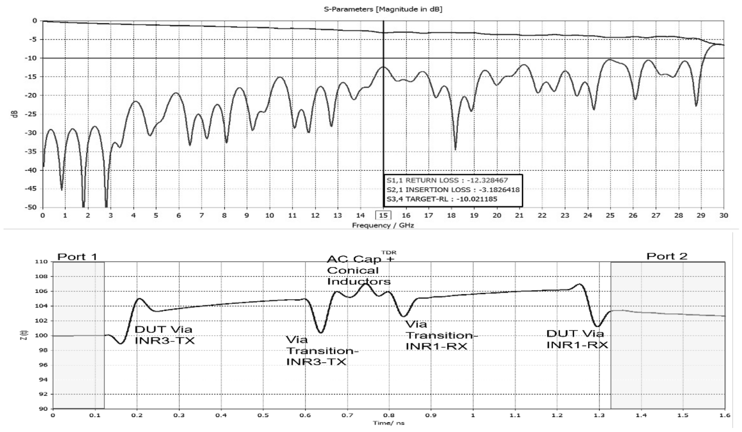
Critical to circuit optimization

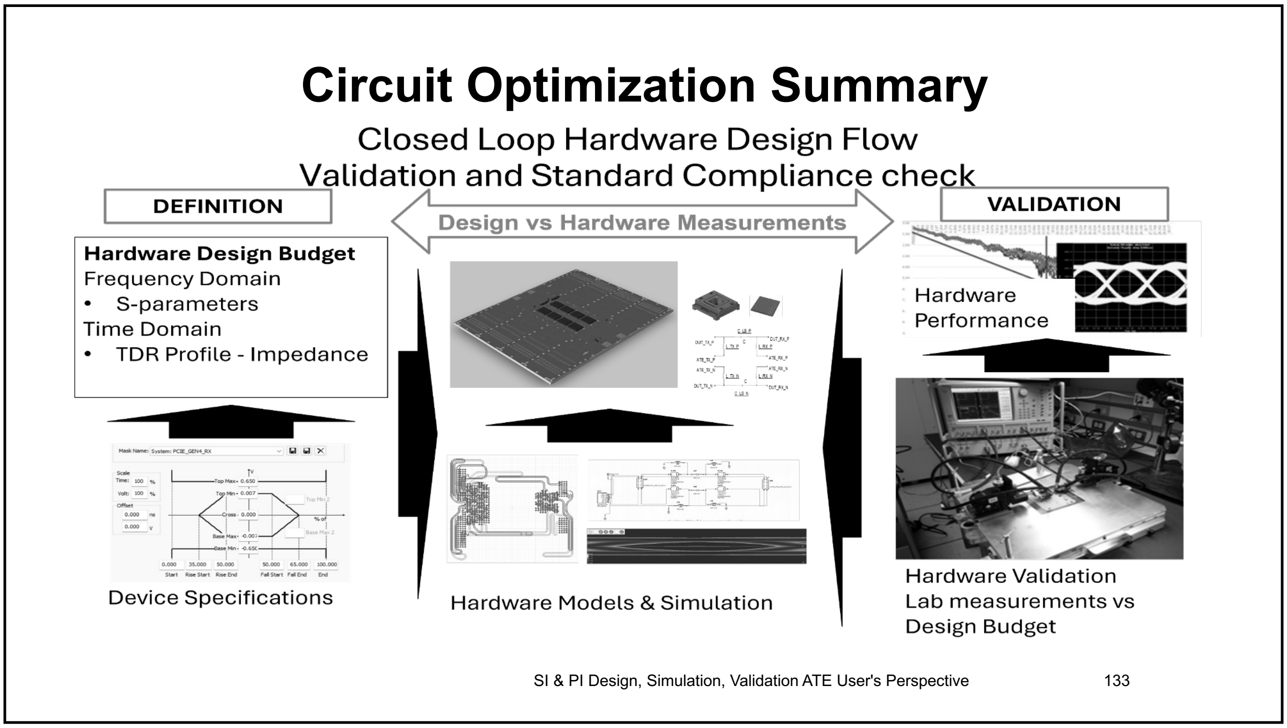
- IP 3D and or frequency models of HW providers (PCB).

S-Parameters & TDR



Design File Signal Routing





Circuit Optimization Summary

Closed Loop Hardware Design Flow
Validation and Standard Compliance check

DEFINITION

Hardware Design Budget
Frequency Domain
- S-parameters

Time Domain
- TDR Profile - Impedance

Device Specifications

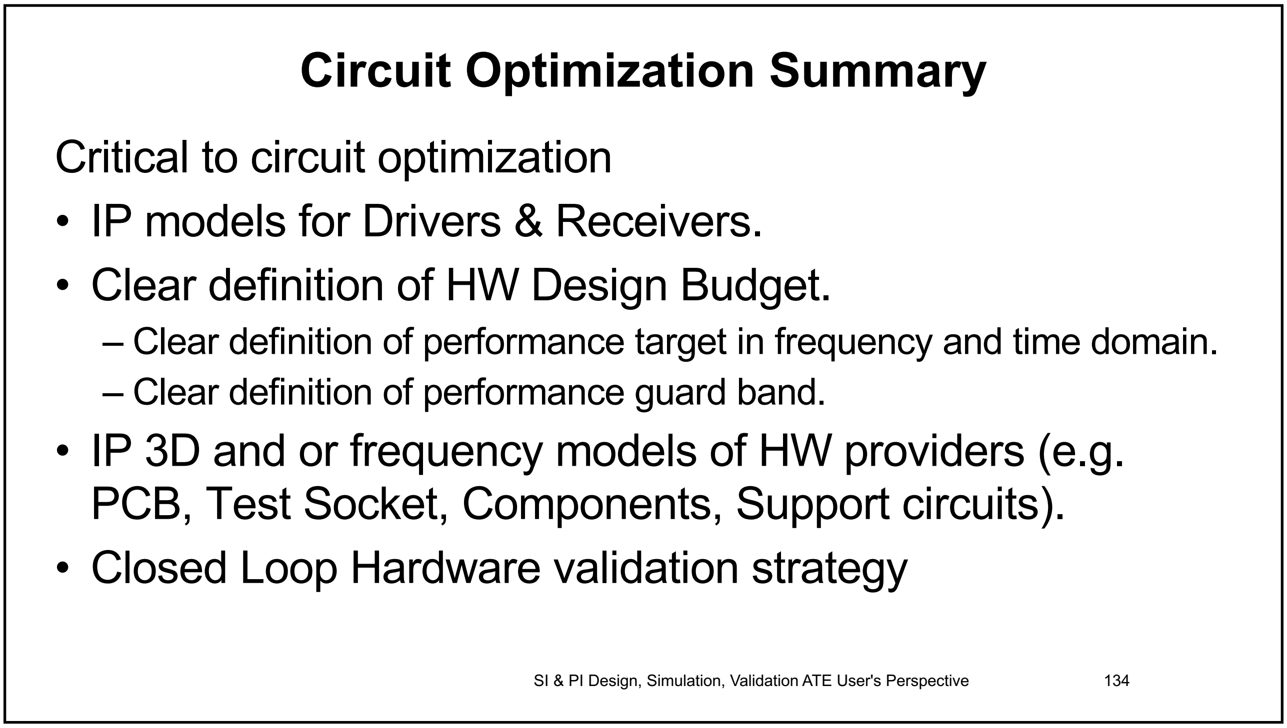
Design vs Hardware Measurements

Hardware Models & Simulation

VALIDATION

Hardware Performance

Hardware Validation
Lab measurements vs
Design Budget



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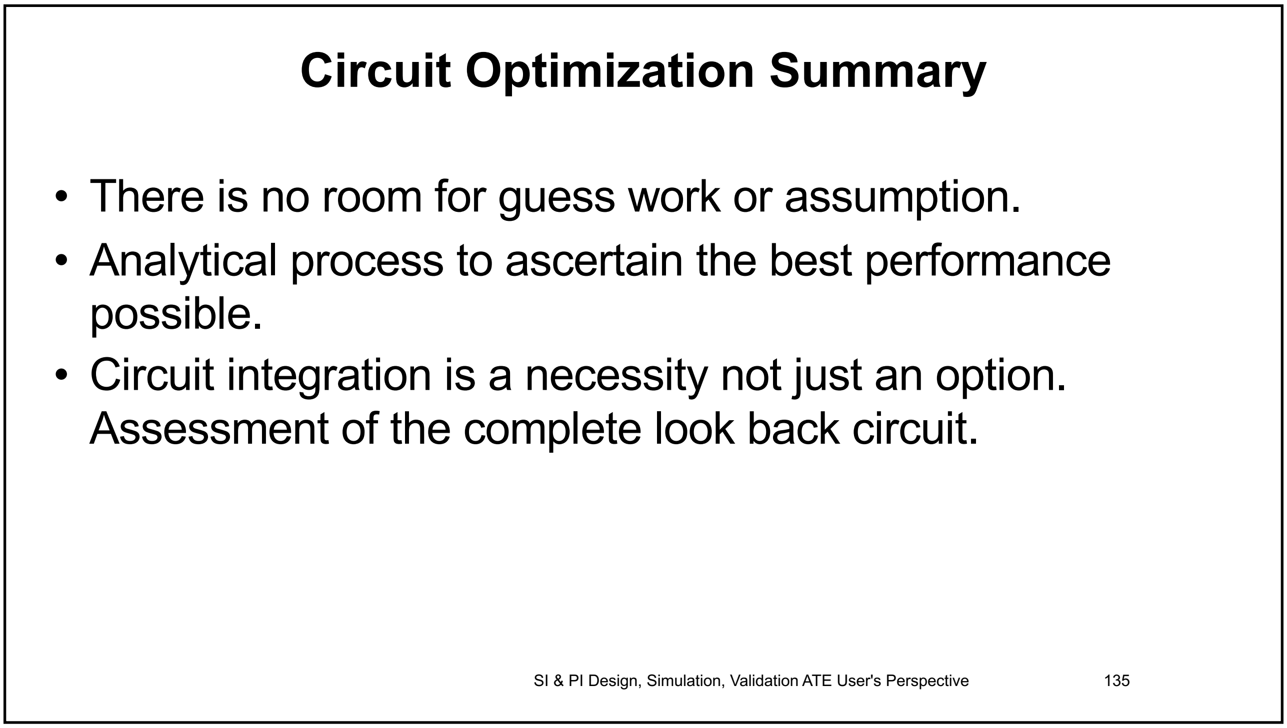
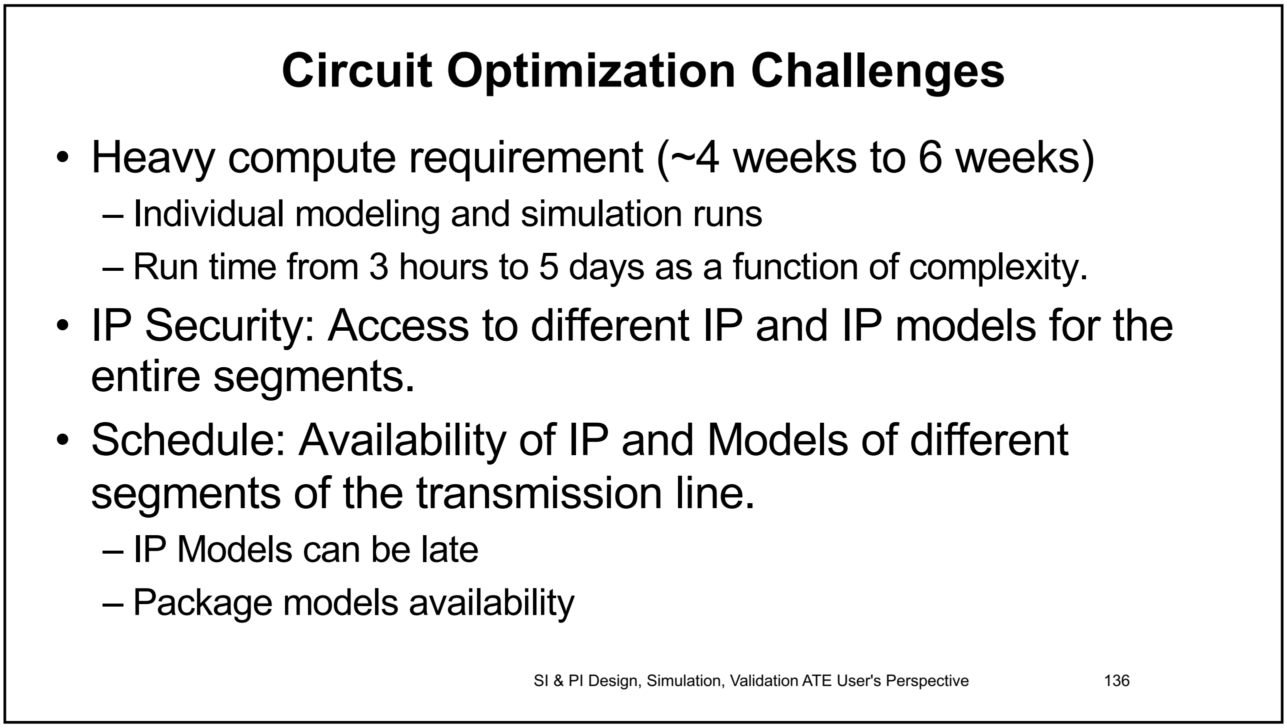


Circuit Optimization Summary

- There is no room for guess work or assumption.
- Analytical process to ascertain the best performance possible.
- Circuit integration is a necessity not just an option. Assessment of the complete look back circuit.



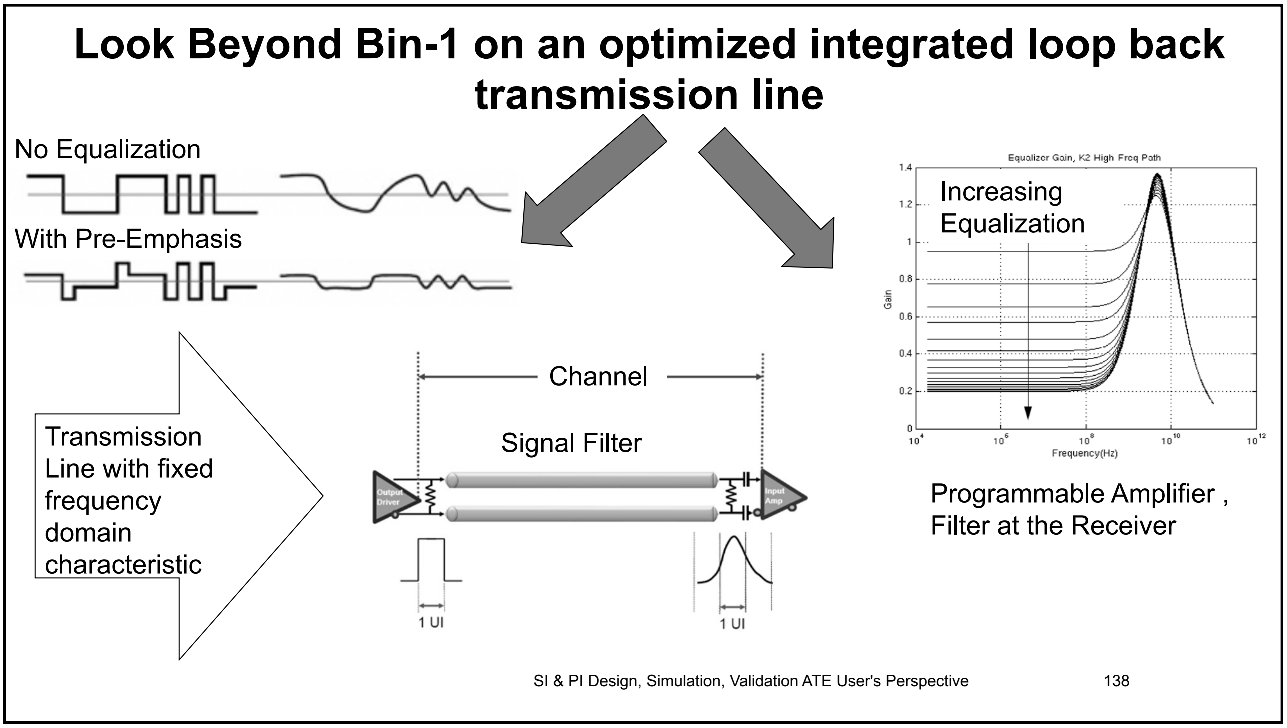
Circuit Optimization Challenges

- Heavy compute requirement (~4 weeks to 6 weeks)
  - Individual modeling and simulation runs
  - Run time from 3 hours to 5 days as a function of complexity.
- IP Security: Access to different IP and IP models for the entire segments.
- Schedule: Availability of IP and Models of different segments of the transmission line.
  - IP Models can be late
  - Package models availability

Circuit Optimization Summary

Decisions can’t be made based on a single segment model and simulation results. That is integration is completed with positive results.

- PCB models and simulation results is just one piece of the puzzle.
- Test Socket models and simulation results are 90% to 95% incompatible during integration process and needs to be updated.



Look Beyond Bin-1 on an optimized integrated loop back transmission line

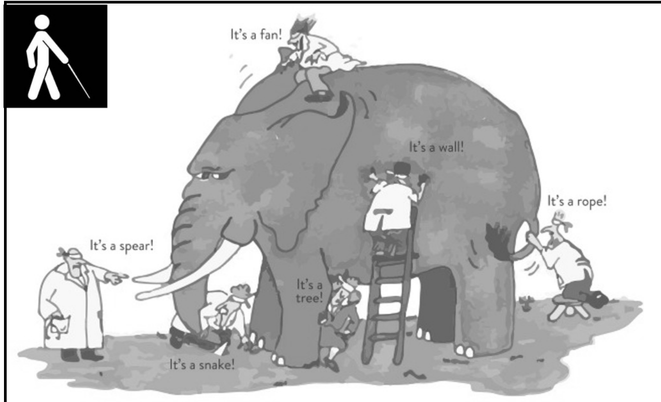
No Equalization

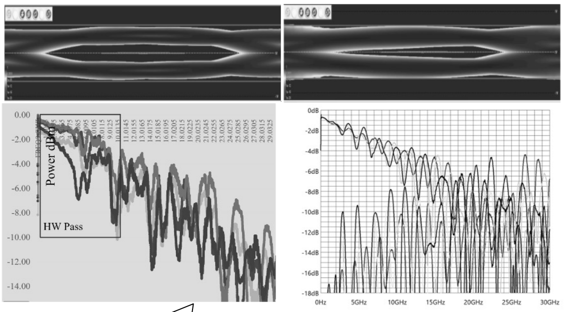
With Pre-Emphasis

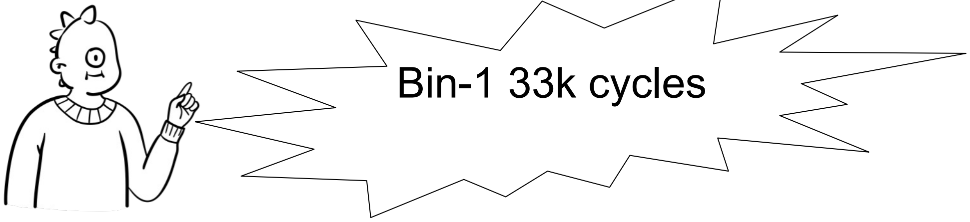
Transmission Line with fixed frequency domain characteristic

Programmable Amplifier , Filter at the Receiver

Blinded by Bin-1

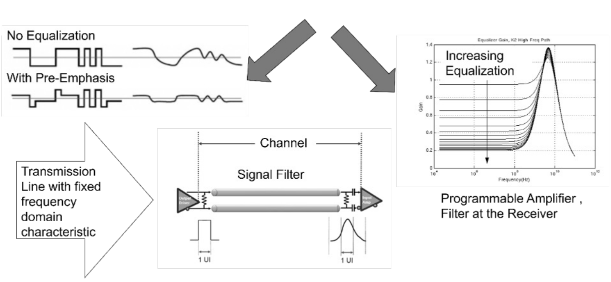






Know, Quantify the transmission line (filter), no room for guess work or assumption

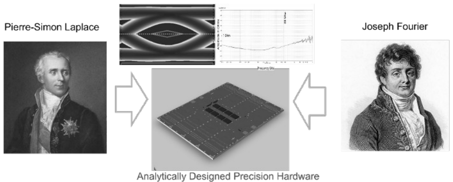
Transmission Line Objective Assessment



Programmable Amplifier , Filter at the Receiver

Define Good

Equalization
DFE: Decision Feed Back Equalization
CTE: Continuous Time Equalization

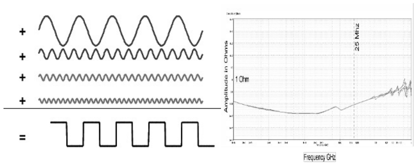


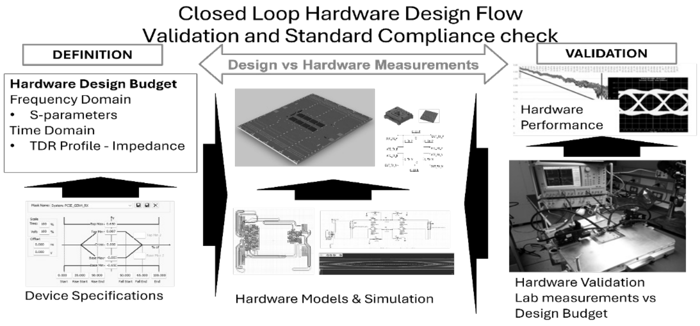
DUT at speed functional test don't involve the ATE.
Dut Signaling(SI) and Power(PI) delivery in FREQUENCY DOMAIN

Questions ?

Validation
Translation of Models, Simulation Results to Physical World

Mesa, Arizona ● March 1–4, 2026





Closed Loop Hardware Design Flow
Validation and Standard Compliance check

TEST HARDWARE VALIDATION

Models to Real World Hardware

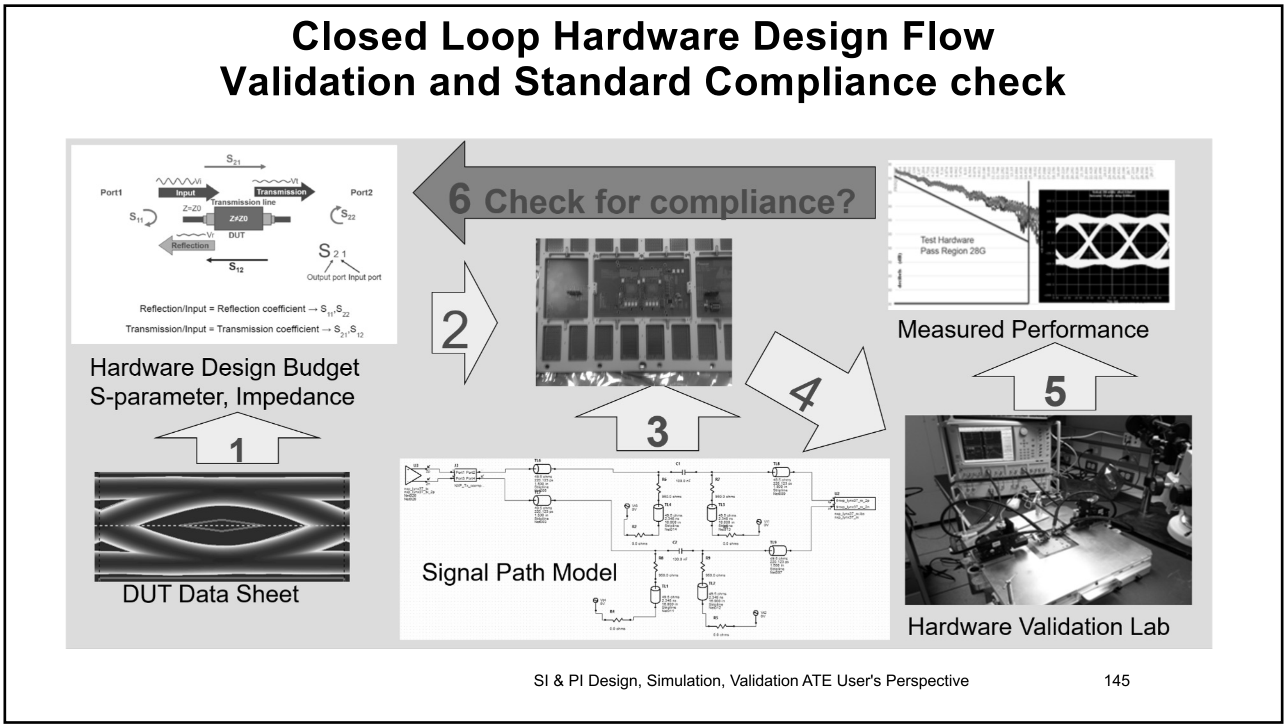
Models and Simulation results are of very little value unless it translate to real work integrated hardware.

PCB and support circuits dominate the transmission line of the loop back circuit.

  Non-compliance is common on any existing PCB providers today as a function of requirements, design budget.

  Test Sockets and interposers are the common source of discontinuity specifically during integration with the package and pcb structures.

Measure and validate. No room for guess work and assumption.



Closed Loop Hardware Design Flow
Validation and Standard Compliance check

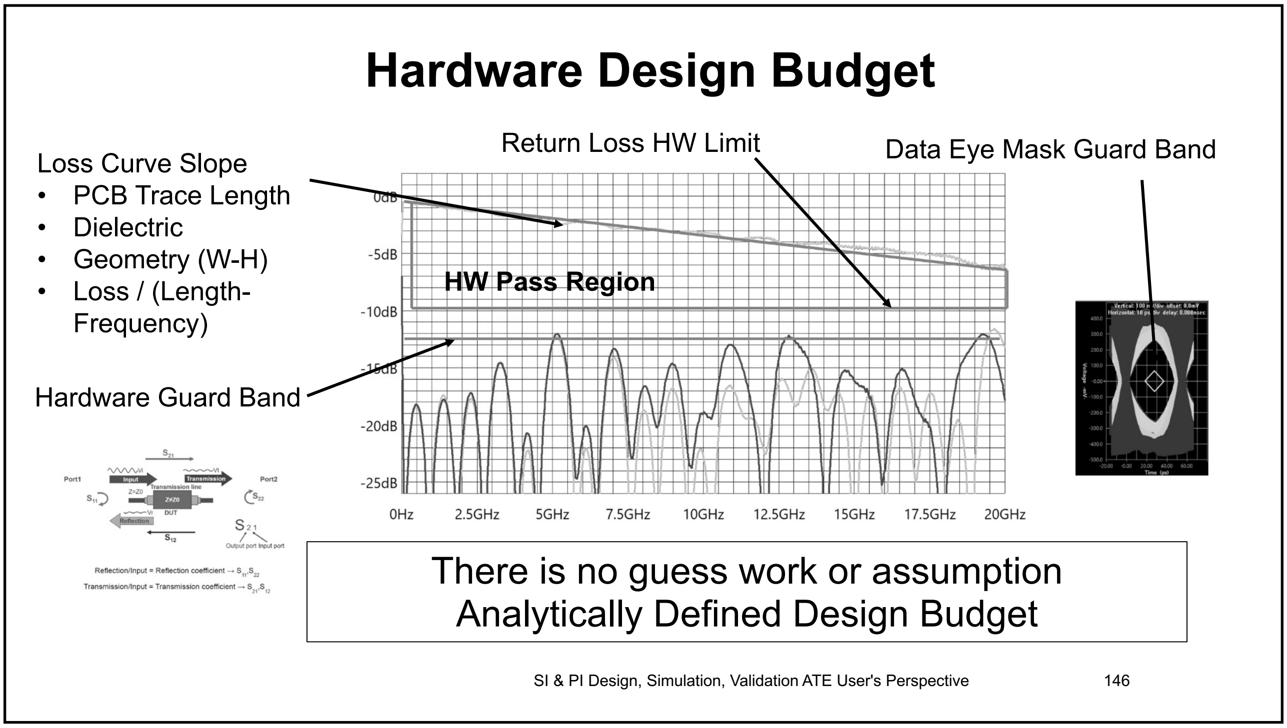
Hardware Design Budget
S-parameter, Impedance

DUT Data Sheet

Signal Path Model

Measured Performance

Hardware Validation Lab



Hardware Design Budget

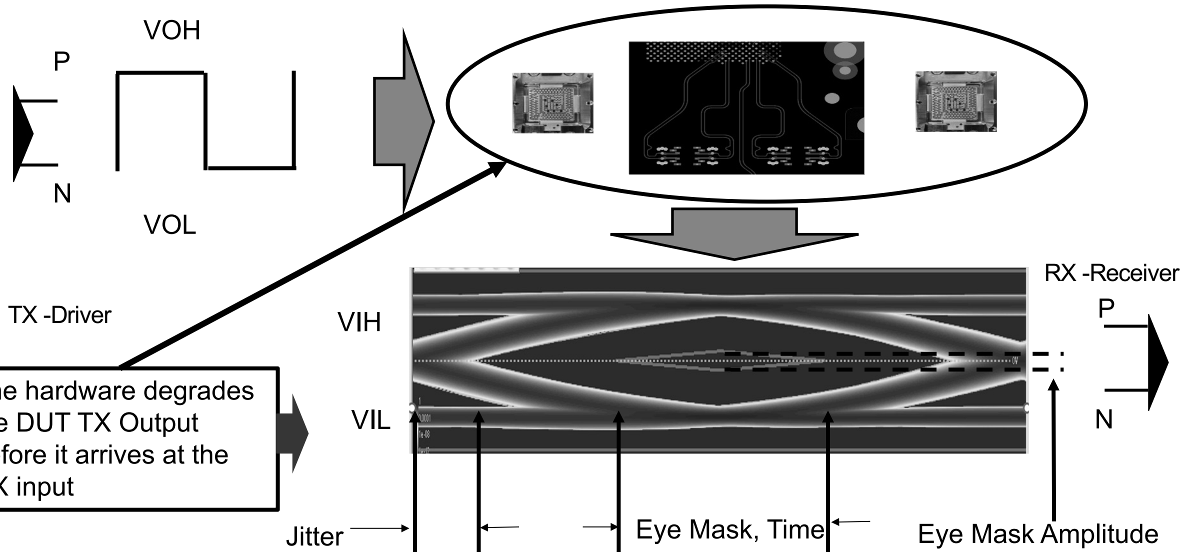
Loss Curve Slope
- PCB Trace Length
- Dielectric
- Geometry (W-H)
- Loss / (Length-Frequency)

Hardware Guard Band

Return Loss HW Limit

Data Eye Mask Guard Band

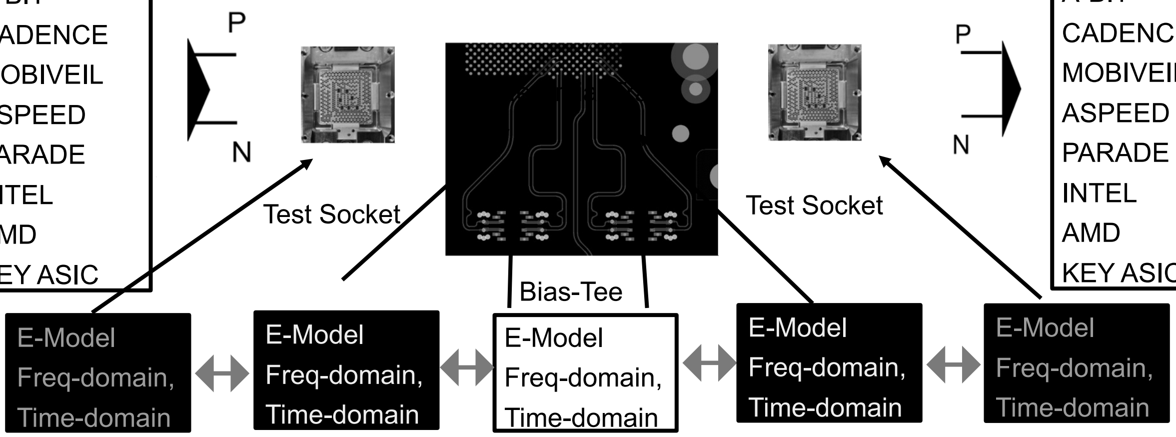
There is no guess work or assumption
Analytically Defined Design Budget



The hardware degrades the DUT TX Output before it arrives at the RX input

Loop Back Testing Transmission Line Segments

- SYNOPSIS
- A-BIT
- CADENCE
- MOBIVEIL
- ASPEED
- PARADE
- INTEL
- AMD
- KEY ASIC



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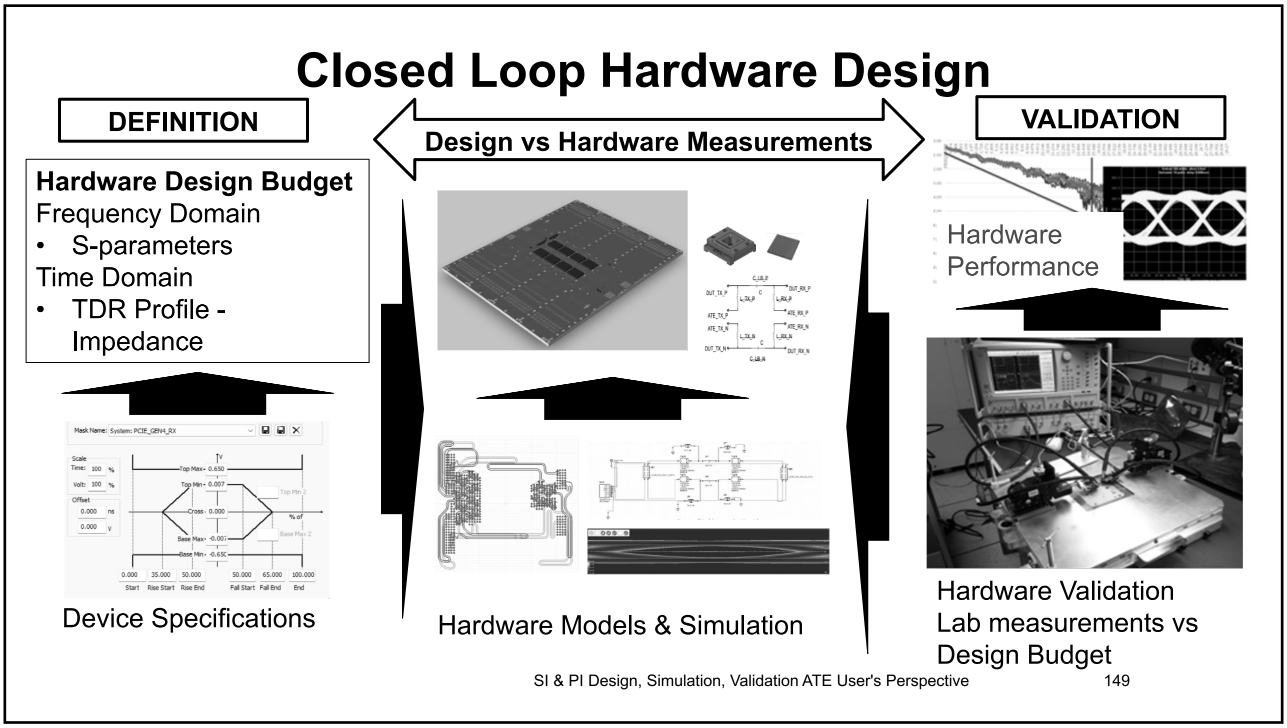


Closed Loop Hardware Design

DEFINITION

Design vs Hardware Measurements

VALIDATION

Hardware Design Budget
Frequency Domain
- S-parameters

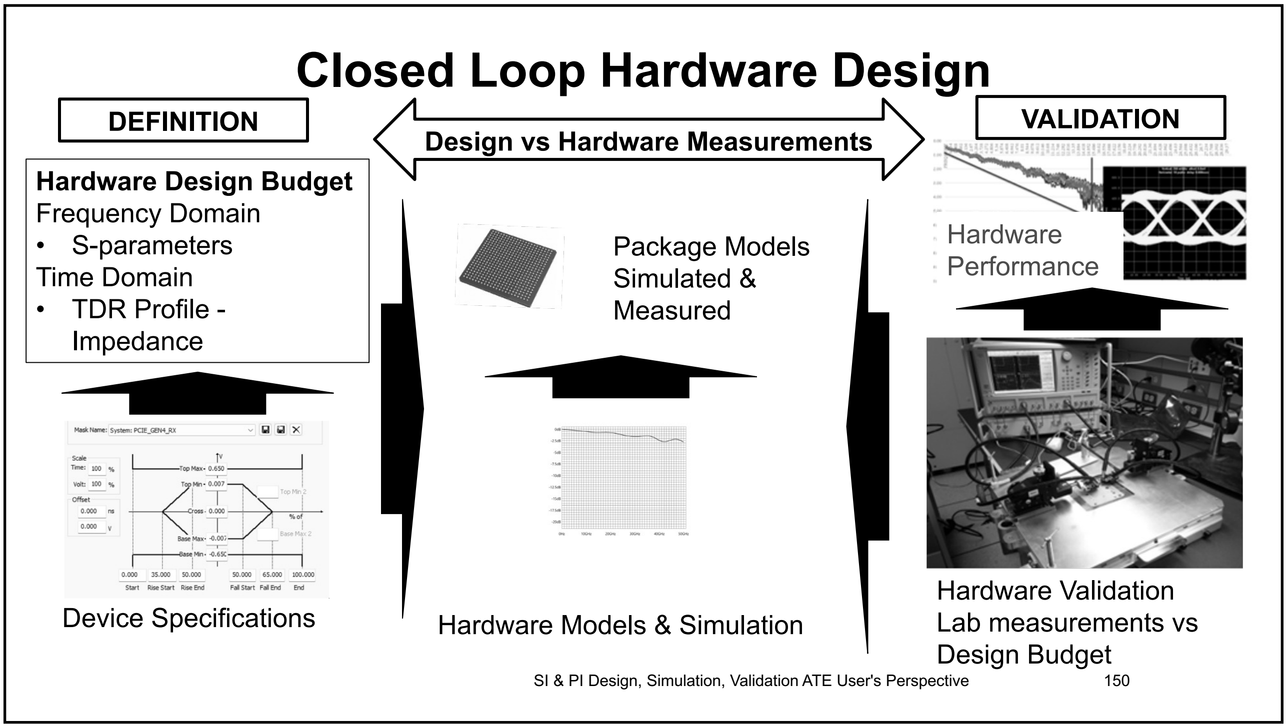
Time Domain
- TDR Profile - Impedance

Hardware Performance

Device Specifications

Hardware Models & Simulation

Hardware Validation
Lab measurements vs Design Budget



Closed Loop Hardware Design

DEFINITION

Design vs Hardware Measurements

VALIDATION

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Frequency Domain
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- TDR Profile - Impedance

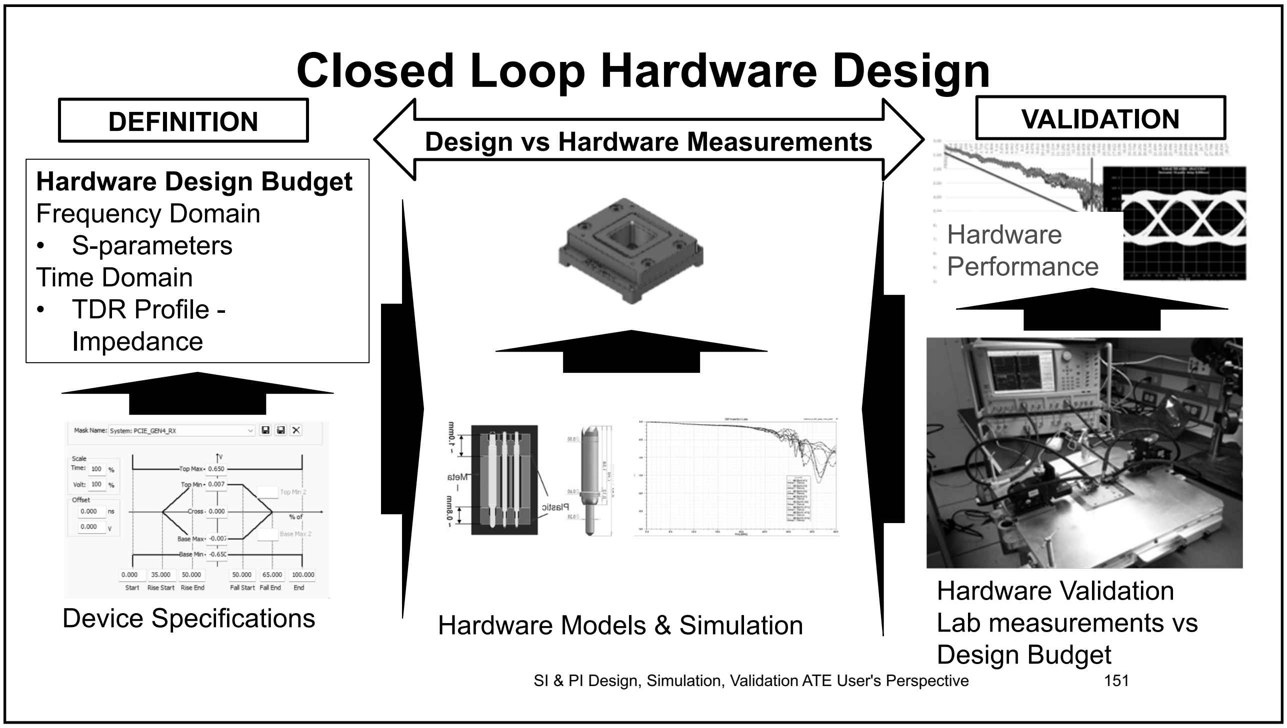
Package Models
Simulated &
Measured

Hardware Performance

Device Specifications

Hardware Models & Simulation

Hardware Validation
Lab measurements vs Design Budget



Closed Loop Hardware Design

DEFINITION

Design vs Hardware Measurements

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Device Specifications

Hardware Models & Simulation

Hardware Performance

Hardware Validation
Lab measurements vs
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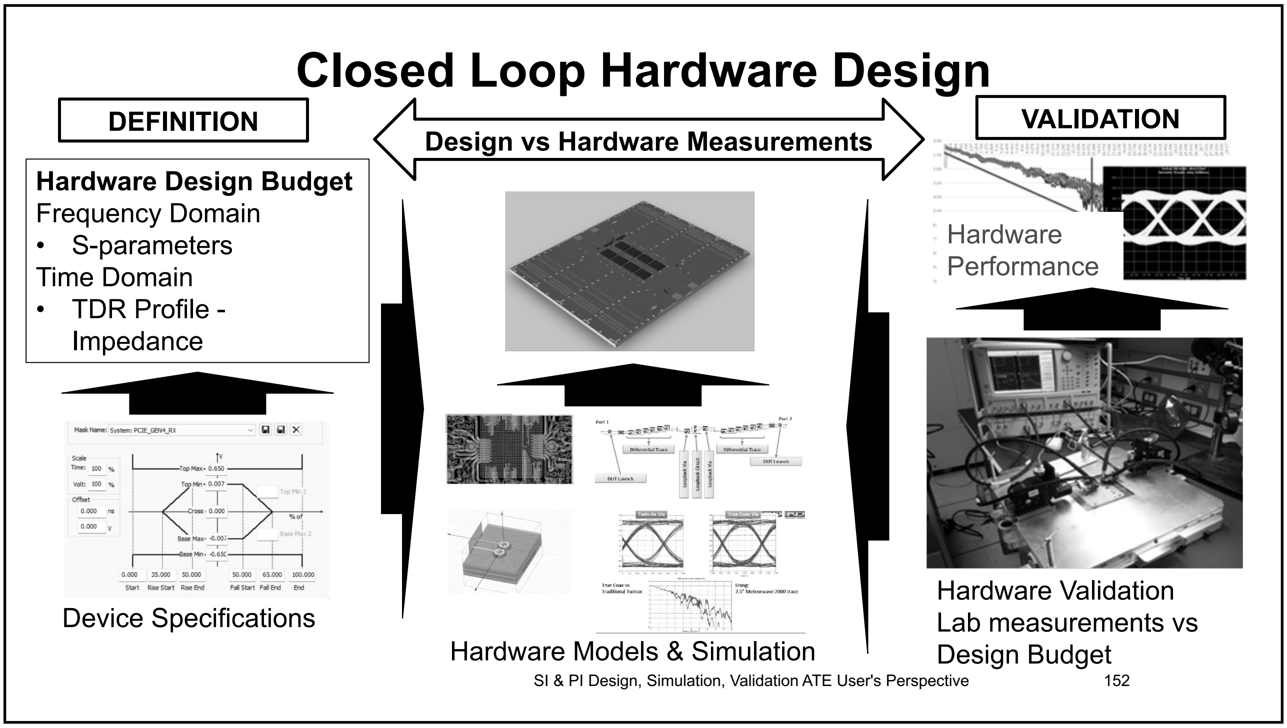

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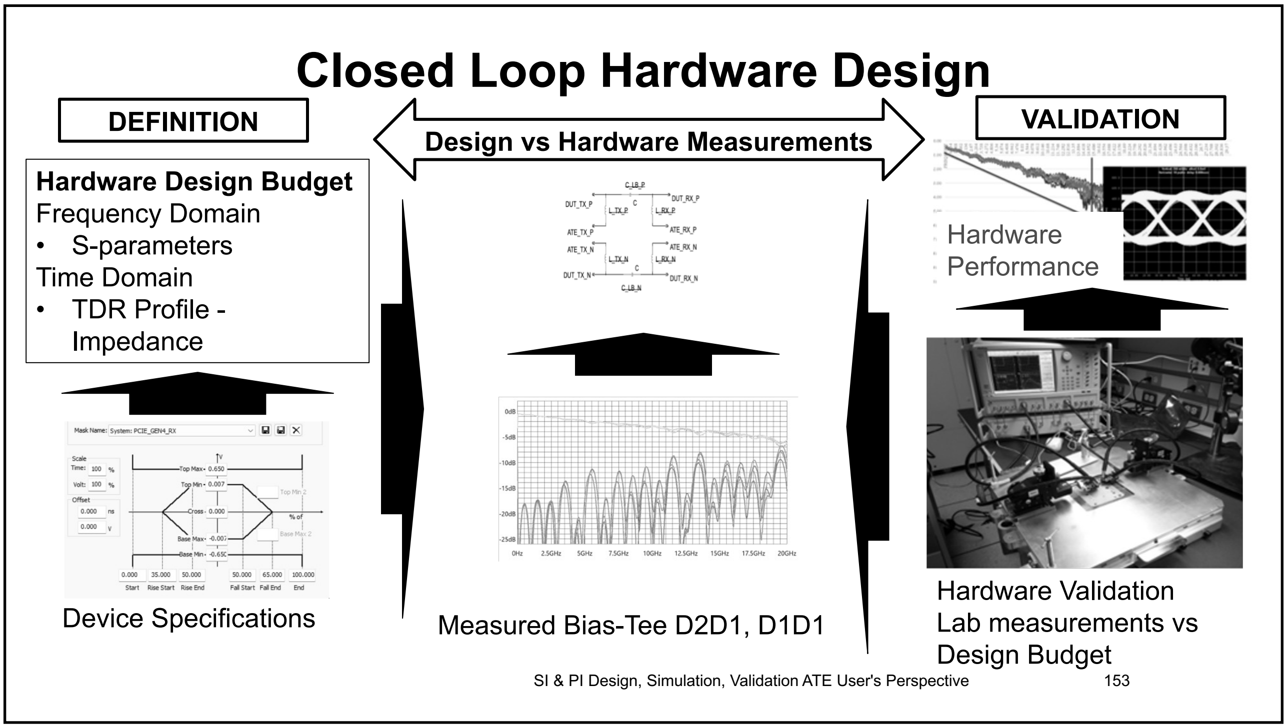


Closed Loop Hardware Design

DEFINITION

Design vs Hardware Measurements

VALIDATION

Hardware Design Budget
Frequency Domain
- S-parameters

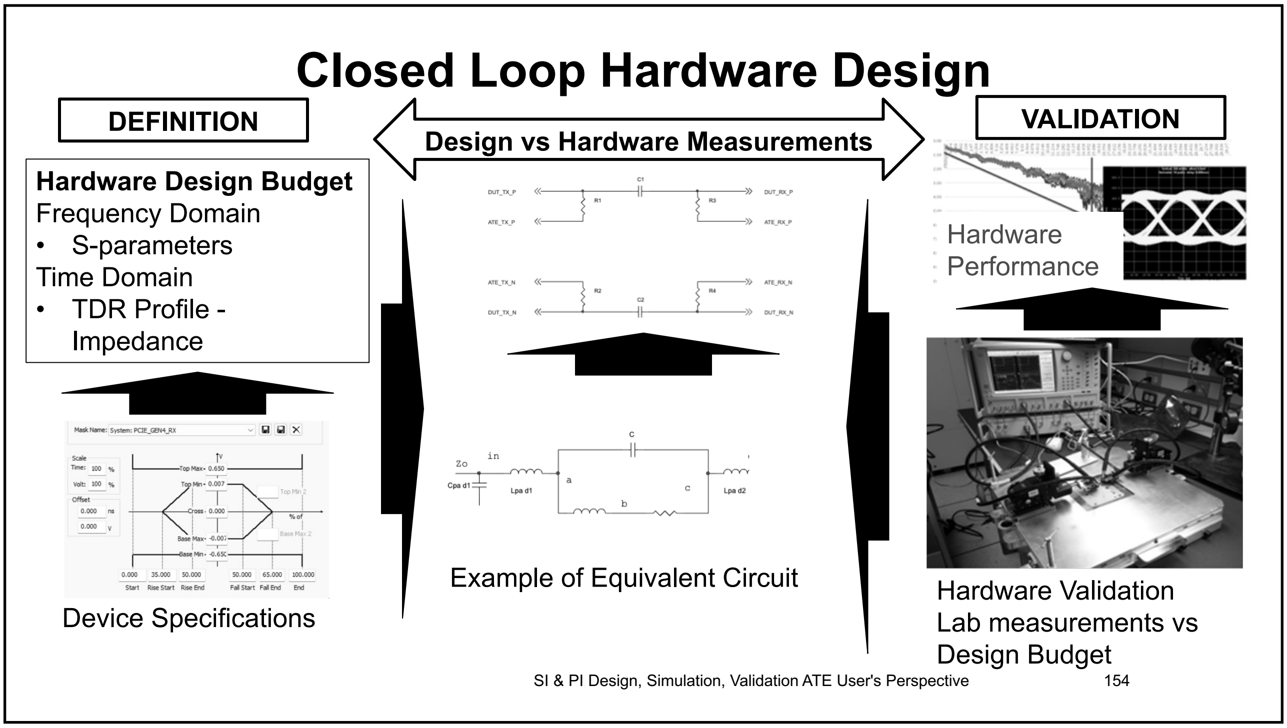
Time Domain
- TDR Profile - Impedance

Hardware Performance

Device Specifications

Measured Bias-Tee D2D1, D1D1

Hardware Validation
Lab measurements vs
Design Budget



Closed Loop Hardware Design

DEFINITION

Design vs Hardware Measurements

VALIDATION

Hardware Design Budget
Frequency Domain
- S-parameters

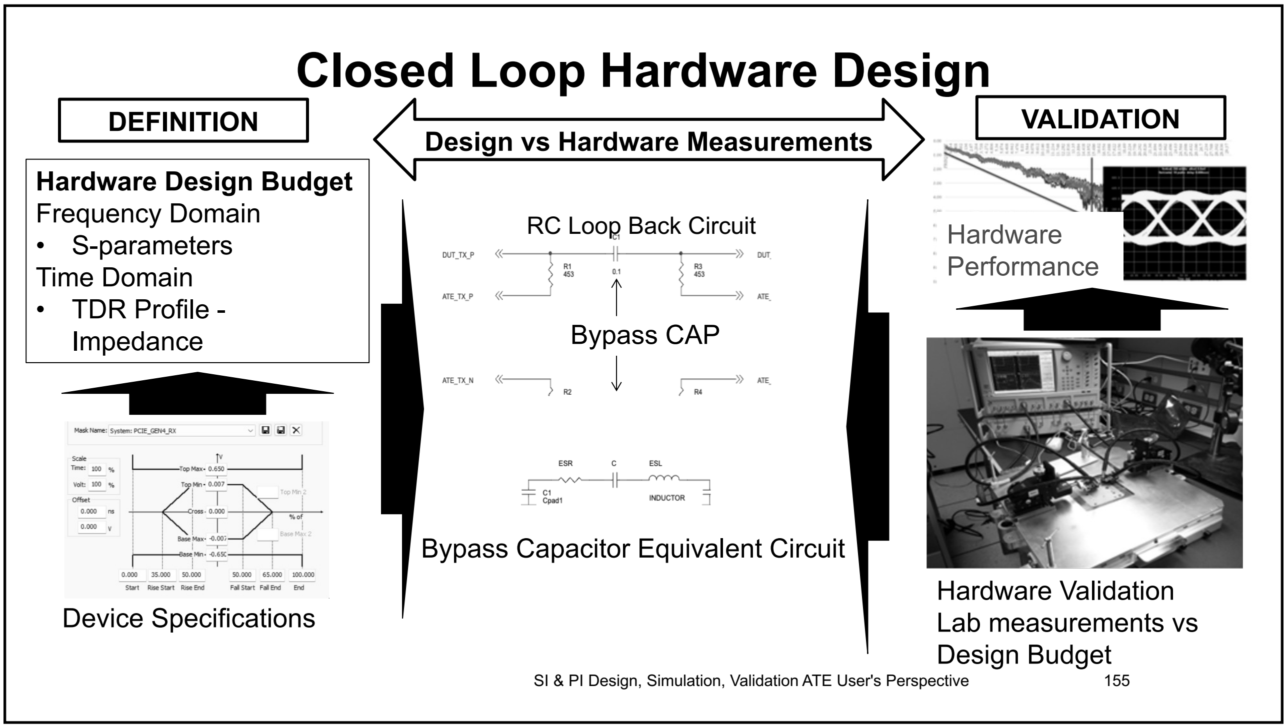
Time Domain
- TDR Profile - Impedance

Hardware Performance

Device Specifications

Example of Equivalent Circuit

Hardware Validation
Lab measurements vs
Design Budget



Closed Loop Hardware Design

DEFINITION

Design vs Hardware Measurements

VALIDATION

Hardware Design Budget
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Device Specifications

RC Loop Back Circuit

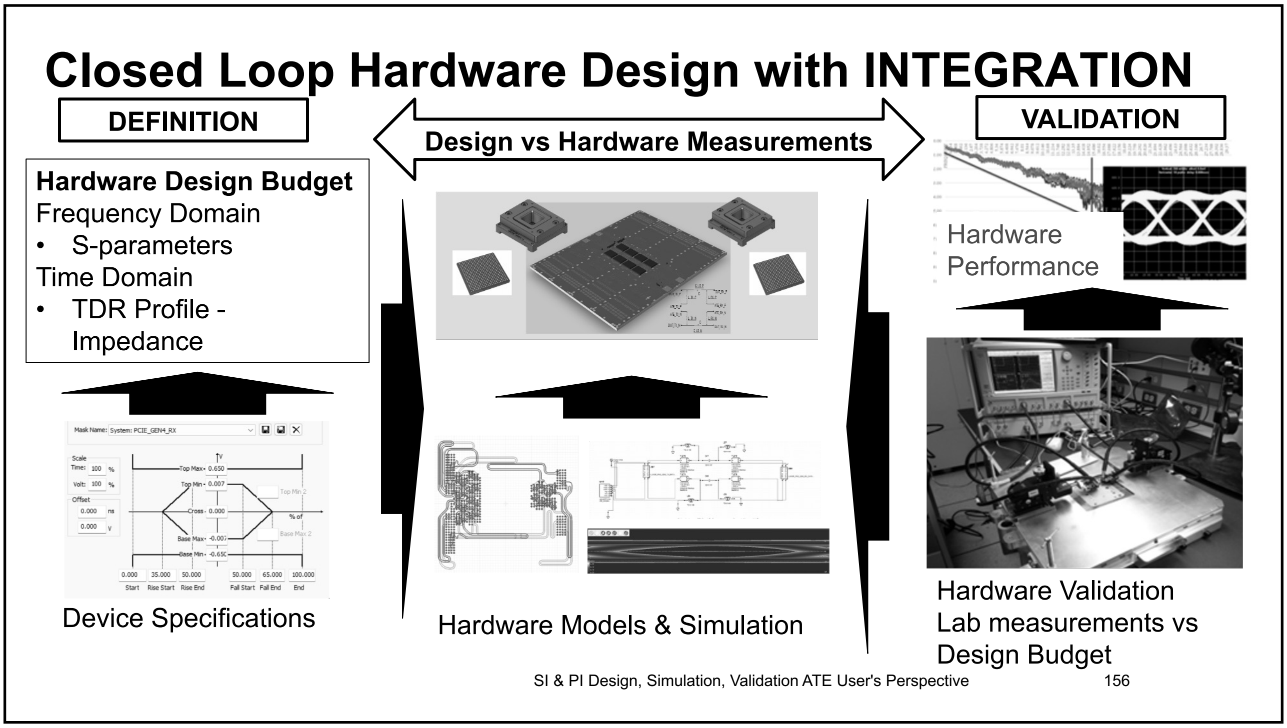
Bypass CAP

Bypass Capacitor Equivalent Circuit

Hardware Performance

Hardware Validation
Lab measurements vs
Design Budget

SI & PI Design, Simulation, Validation ATE User's Perspective



Closed Loop Hardware Design with INTEGRATION

DEFINITION

Design vs Hardware Measurements

VALIDATION

Hardware Design Budget
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- S-parameters

Time Domain
- TDR Profile - Impedance

Device Specifications

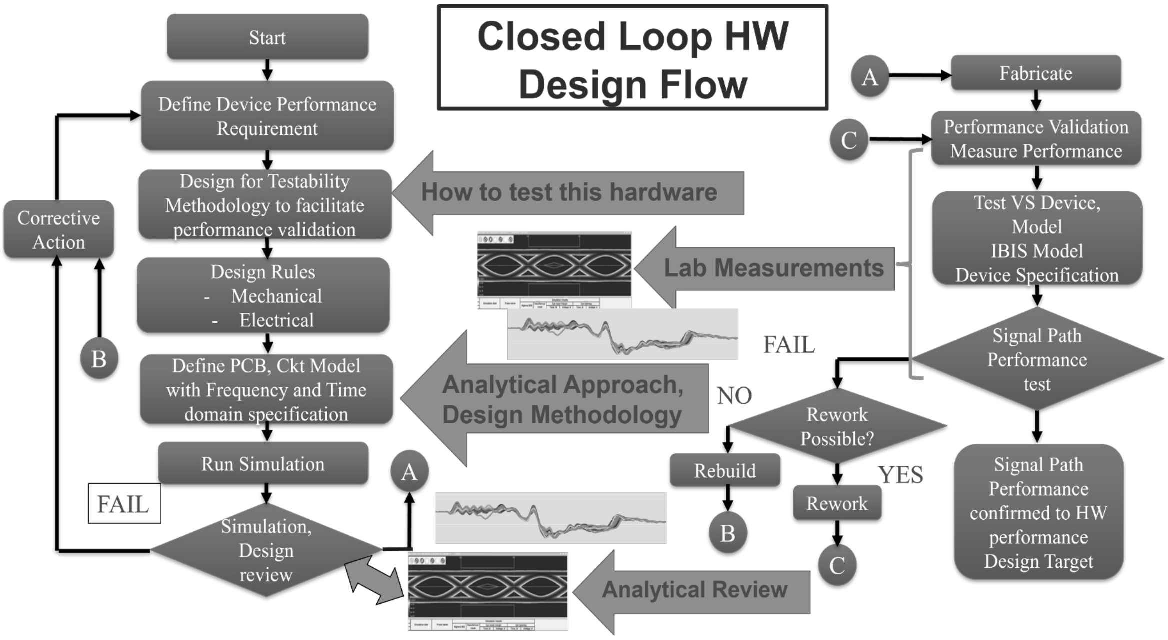
Hardware Models & Simulation

Hardware Performance

Hardware Validation
Lab measurements vs
Design Budget

SI & PI Design, Simulation, Validation ATE User's Perspective

Closed Loop HW Design Flow



Start

Define Device Performance Requirement

Design for Testability Methodology to facilitate performance validation

Design Rules
- Mechanical
- Electrical

Define PCB, Ckt Model with Frequency and Time domain specification

Run Simulation

Simulation, Design review

FAIL

Corrective Action

B

A

How to test this hardware

Lab Measurements

Analytical Approach, Design Methodology

Analytical Review

A → Fabricate

C → Performance Validation Measure Performance

Test VS Device, Model IBIS Model Device Specification

Signal Path Performance test

FAIL

Rework Possible?

NO

Rebuild

B

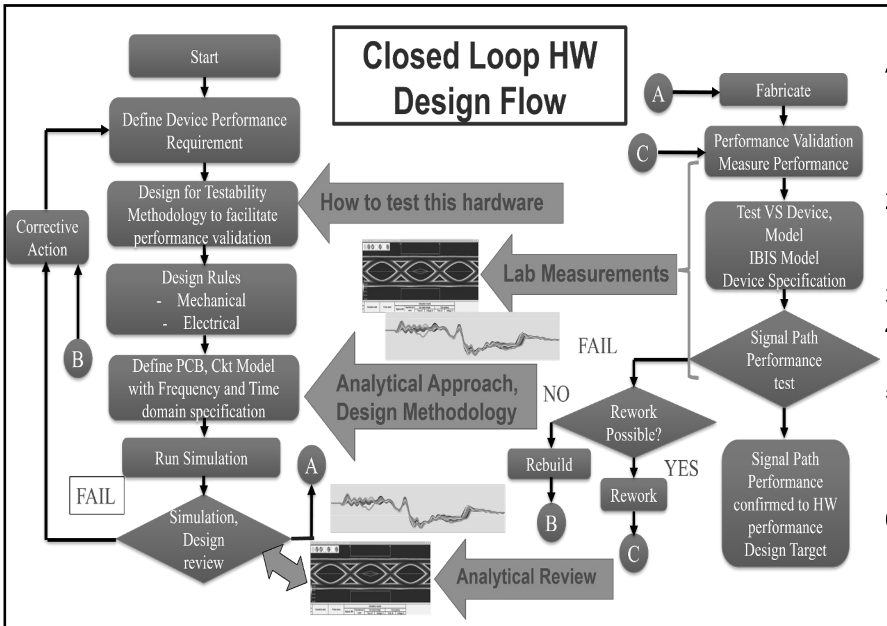
YES

Rework

C

Signal Path Performance confirmed to HW performance Design Target

Closed Loop HW Design Flow



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NO

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B

YES

Rework

C

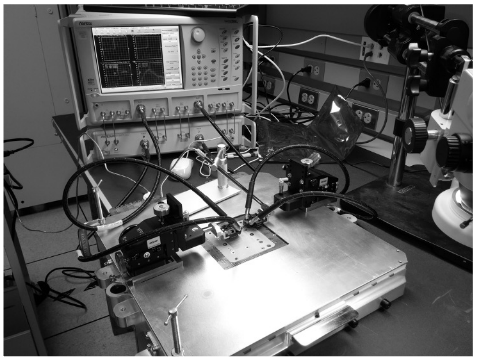
Signal Path Performance confirmed to HW performance Design Target

Analytical Approach to HW Design

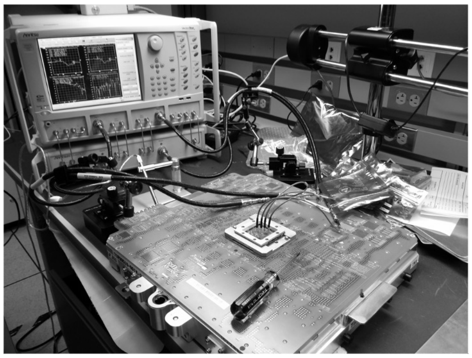
1. **We don't need the device to guarantee BIN-1**
2. Quantified performance target with transmission line parameters
3. Structures are modeled
4. HW DFT, with the capability for performance verification
5. There is no confusion between HW-capability and device performance requirements
6. It requires a strong SI Team to ensure Models, Simulation Results hold true in real world (validated)

VALIDATION WITH VECTOR NETWORK ANALYZER

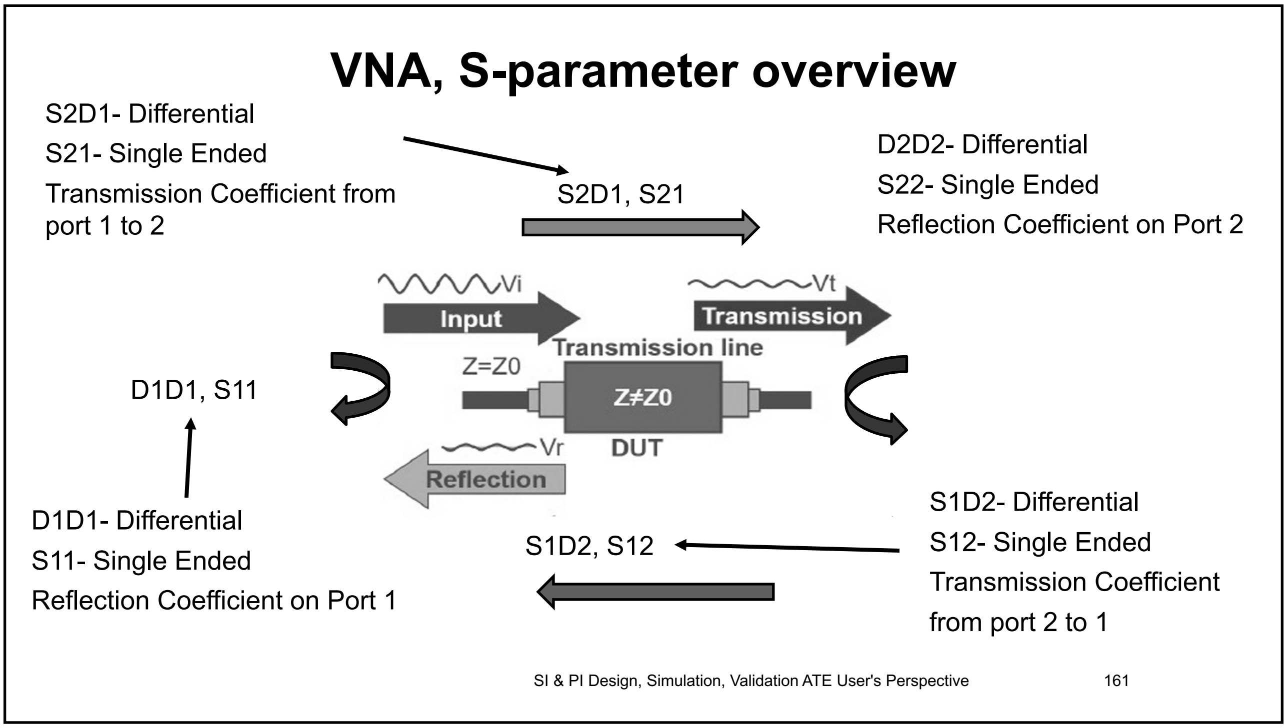
Vector Network Analyzer(VNA) for hardware transmission line validation



Vector Network Analyzer
Board Probe



Vector Network Analyzer
Cabled



VNA, S-parameter overview

S2D1- Differential
S21- Single Ended
Transmission Coefficient from port 1 to 2

S2D1, S21

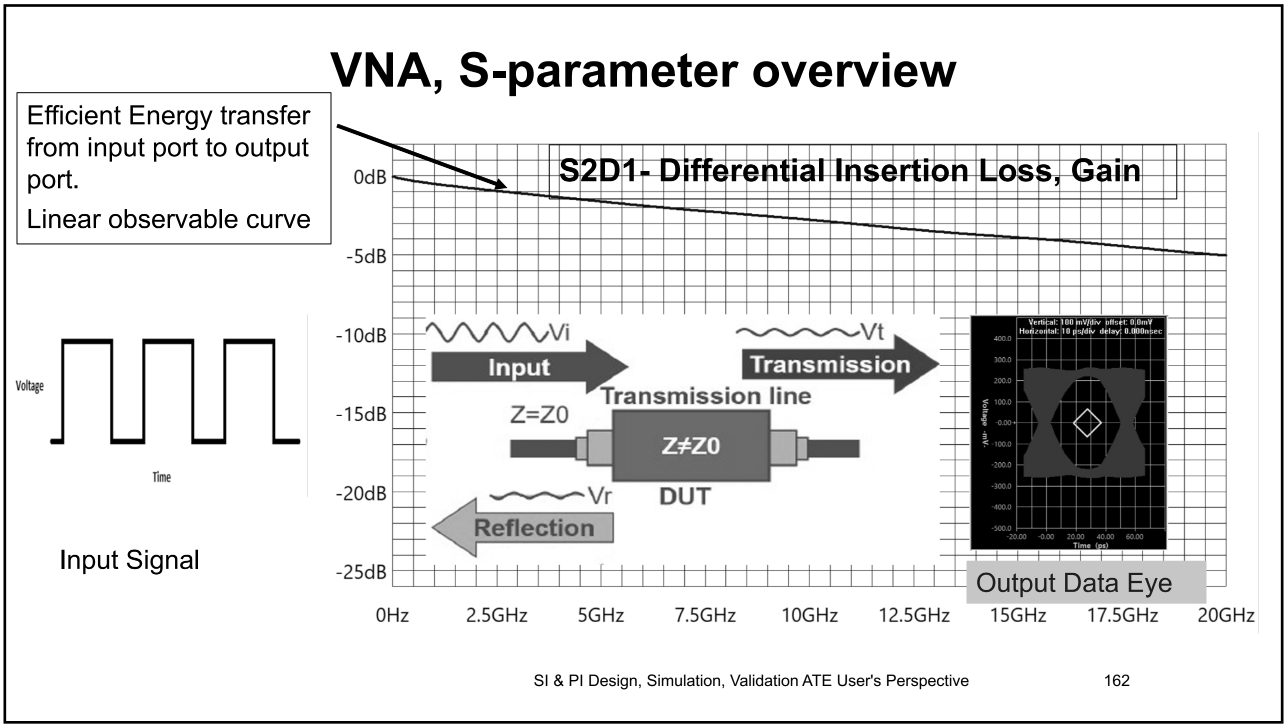
D2D2- Differential
S22- Single Ended
Reflection Coefficient on Port 2

D1D1, S11

D1D1- Differential
S11- Single Ended
Reflection Coefficient on Port 1

S1D2, S12

S1D2- Differential
S12- Single Ended
Transmission Coefficient from port 2 to 1



VNA, S-parameter overview

Efficient Energy transfer from input port to output port.
Linear observable curve

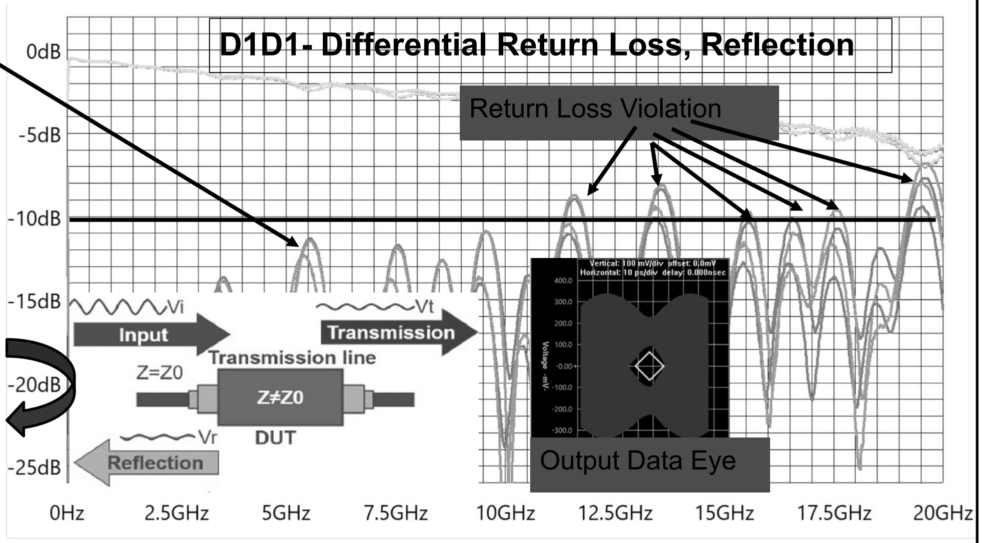
S2D1- Differential Insertion Loss, Gain

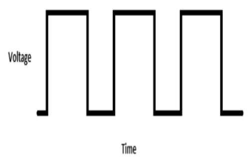
Input Signal

Output Data Eye

VNA, S-parameter overview, Cross check with other VNA Lab

High Reflection rate
Poor Energy transfer
from input port to
output port.

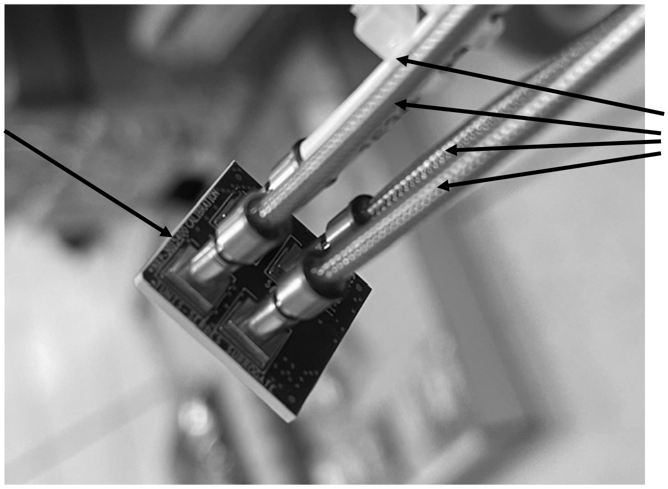




Input Signal

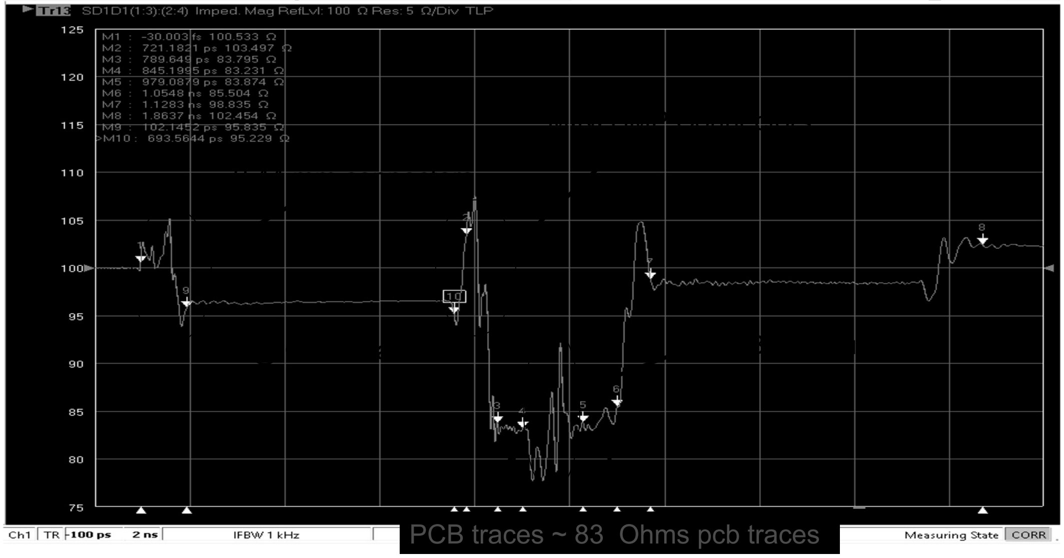
VNA D-embedding methods

Measuring fixture
(e.g. probe-package-pcb)
Differential 4-port



4-Port Cable
2.4mm to Mini SMP
6 Inch Cable

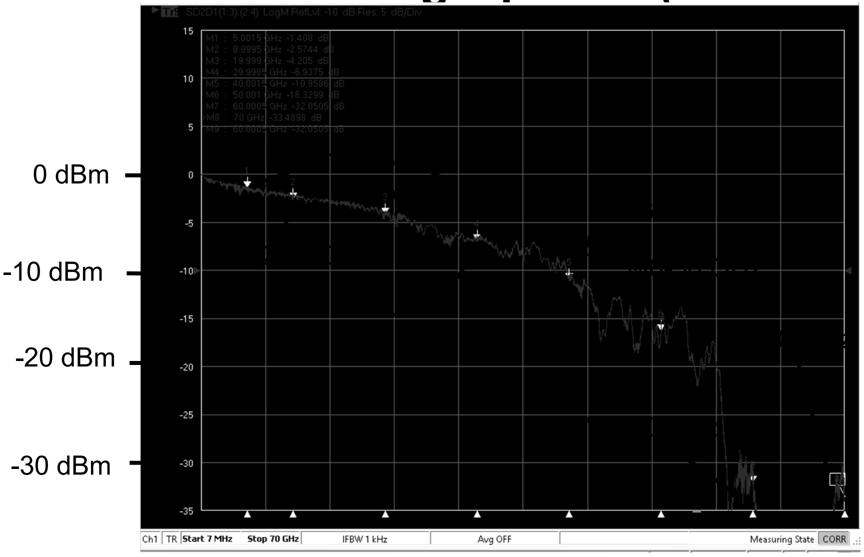
VNA, Time Domain Reflectometry



```
Tr13 SD1D1(1:3):(2:4) Imped. Mag RefLvl: 100 Ω Res: 5 Ω/Div TLP
M1 :  -30.003 fs 100.533 Ω
M2 :  721.1821 ps 103.497 Ω
M3 :  789.649 ps 83.795 Ω
M4 :  845.1995 ps 83.231 Ω
M5 :  979.0879 ps 83.874 Ω
M6 :  1.0548 ns 85.504 Ω
M7 :  1.1283 ns 98.835 Ω
M8 :  1.8637 ns 102.454 Ω
M9 :  102.1452 ps 95.835 Ω
>M10 :  693.5644 ps 95.229 Ω
```

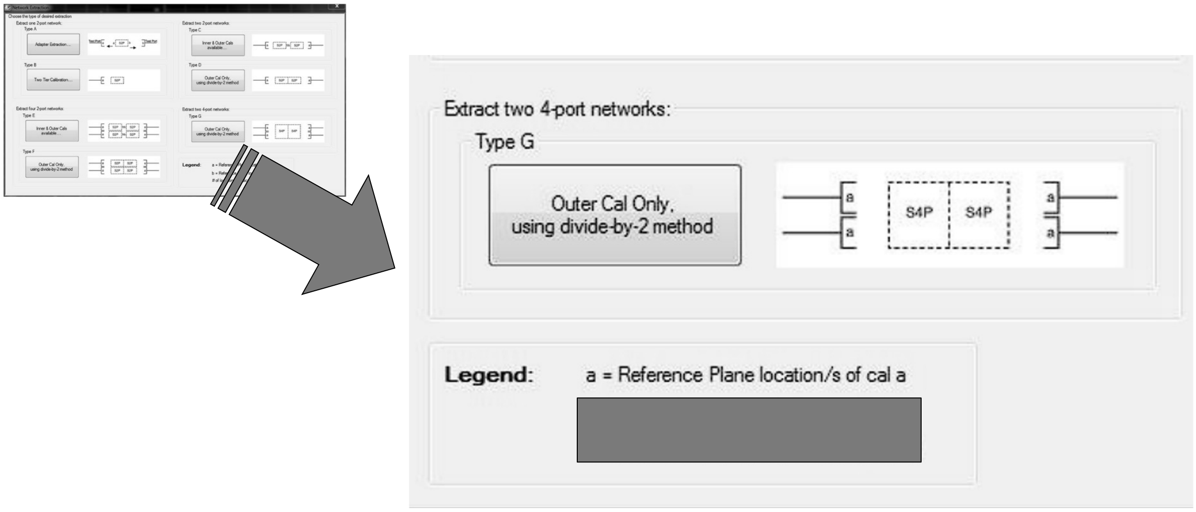
PCB traces ~ 83 Ohms pcb traces

VNA De-embedding Options (Insertion Loss)



```
Tr9 SD2D1(1:3):(2:4) LogM RefLvl: -10 dB Res: 5 dB/Div
M1 :  5.0015 GHz -1.408 dB
M2 :  9.9995 GHz -2.5744 dB
M3 :  19.999 GHz -4.205 dB
M4 :  29.9985 GHz -6.9375 dB
M5 :  40.0015 GHz -10.9586 dB
M6 :  50.001 GHz -16.3299 dB
M7 :  60.0005 GHz -32.0505 dB
>M8 :  70 GHz -33.4896 dB
M9 :  60.0005 GHz -32.0505 dB
```

VNA De-embedding Options



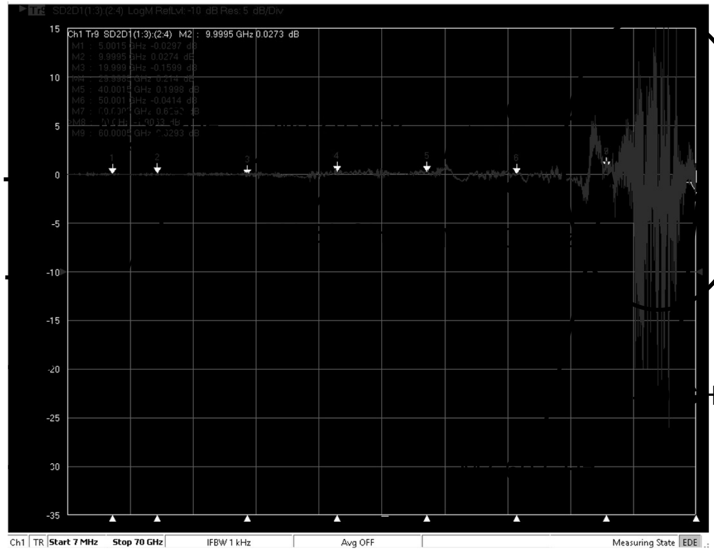
Extract two 4-port networks:

Type G

Legend: a = Reference Plane location/s of cal a

[redacted]

VNA De-embedding Options (Insertion Loss)



```
Tr9 SD2D1(1:3):(2:4) LogM RefLvl: -10 dB Res: 5 dB/Div
Ch1 Tr9 SD2D1(1:3):(2:4)  M2 :  9.9995 GHz 0.0273 dB
M1 :  5.0015 GHz  -0.0297 dB
M2 :  9.9995 GHz  0.0274 dB
M3 :  19.999 GHz  -0.1599 dB
M4 :  29.9985 GHz  0.214 dB
M5 :  40.0015 GHz  0.1998 dB
M6 :  50.001 GHz  -0.0414 dB
M7 :  [illegible] GHz  [illegible] dB
>M8 :  70 GHz  [illegible] dB
M9 :  60.0005 GHz  [illegible] dB
```

0 dBm

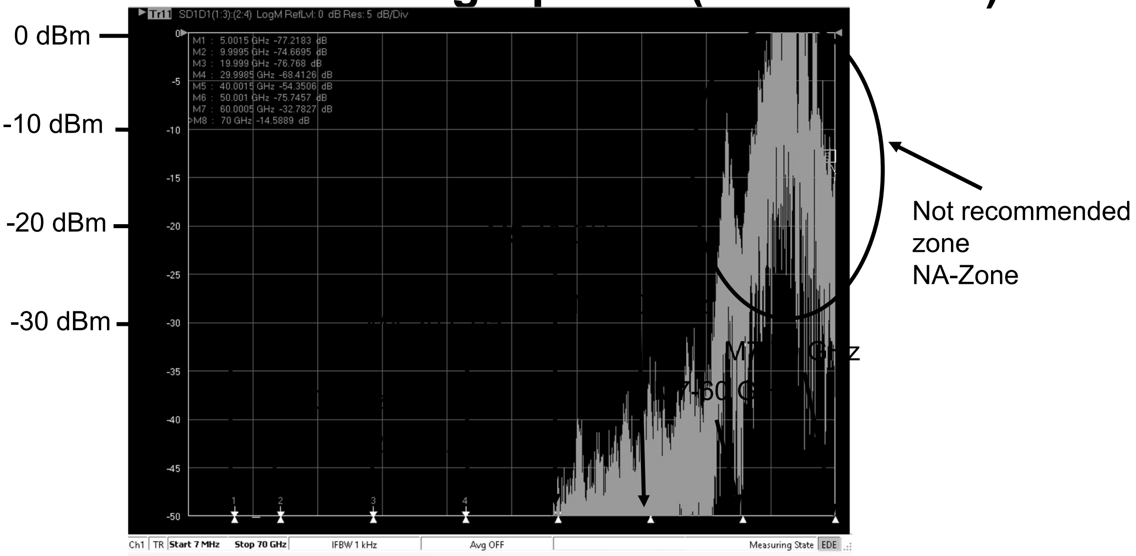
-10 dBm

-20 dBm

-30 dBm

Not recommended zone
NA-Zone

VNA De-embedding Options (Return Loss)



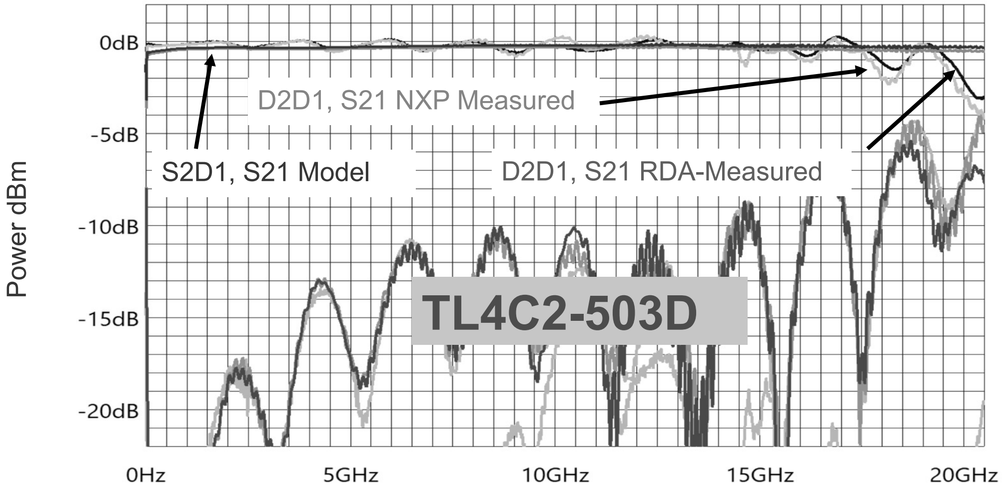
Tr11 SD1D1(1:3):(2:4) LogM RefLvl: 0 dB Res: 5 dB/Div

M1 : 5.0015 GHz -77.2183 dB
M2 : 9.9995 GHz -74.6695 dB
M3 : 19.999 GHz -76.768 dB
M4 : 29.9985 GHz -68.4126 dB
M5 : 40.0015 GHz -54.3506 dB
M6 : 50.001 GHz -75.7457 dB
M7 : 60.0005 GHz -32.7827 dB
>M8 : 70 GHz -14.5889 dB

Ch1 | TR | Start 7 MHz | Stop 70 GHz | IFBW 1 kHz | Avg OFF | Measuring State | EDE

Not recommended zone
NA-Zone

VNA, 85 Ohms Bias-Tee Model vs Two labs Measurement (w/ RDA in Allentown)



Measurement Strategy & Planning two VNA labs

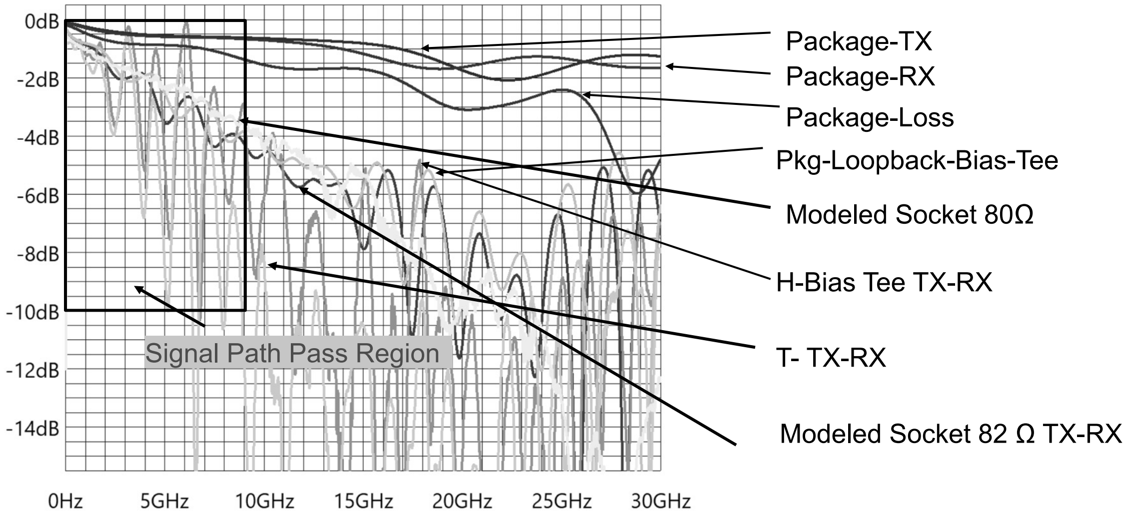
- Correlation of measurement methodology and techniques is key
  - Resolution Steps
  - Range as function of real-world application of the hardware to be measured (e.g. 3rd , 5th harmonic, standards compliance)
  - Fixturing such as connectors, cables, probes, prototype boards
- Hardware Design for Testability
  - How to facilitate Signal Integrity Validation on the hardware
  - Design fixtures, probe for SI measurement of the transmission line
  - Transmission line segment design, analysis, and integration

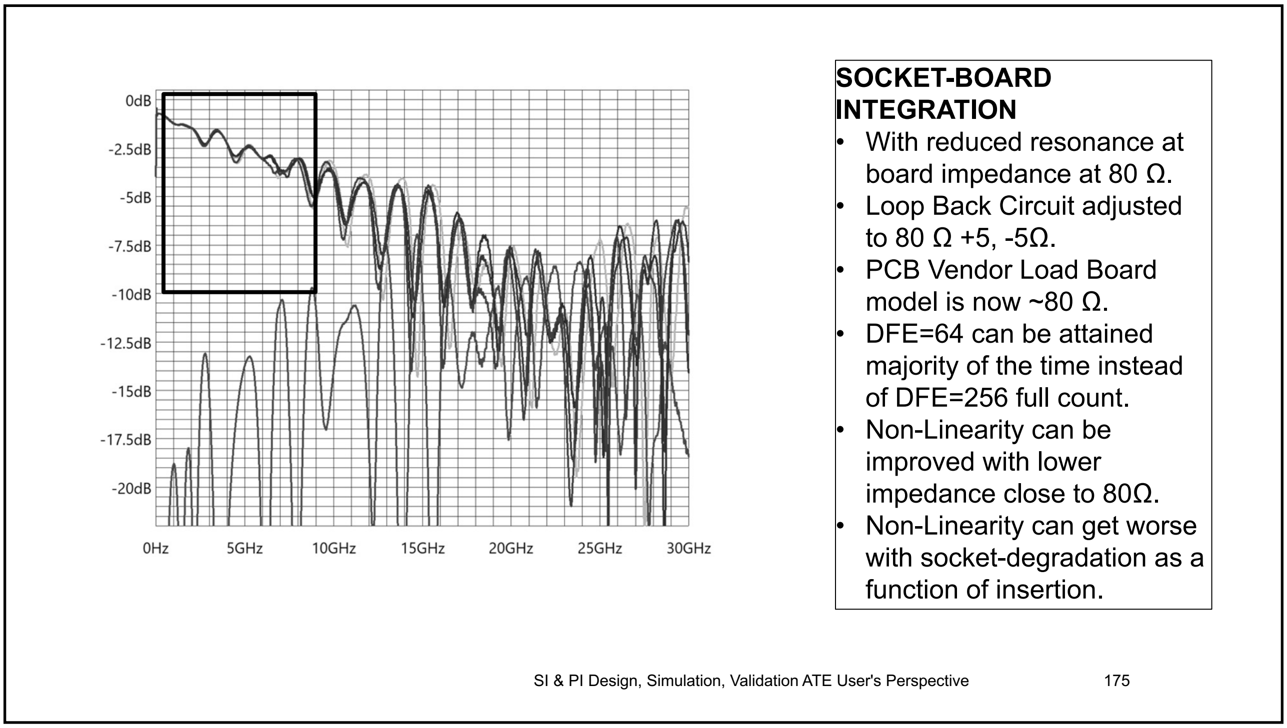
Validation with Vector Network Analyzer

- Cross check or correlate with other VNA Laboratory.
- Always check for compliance and or up to date calibration standards.

VALIDATION EXAMPLES

High failure rate on socket integration

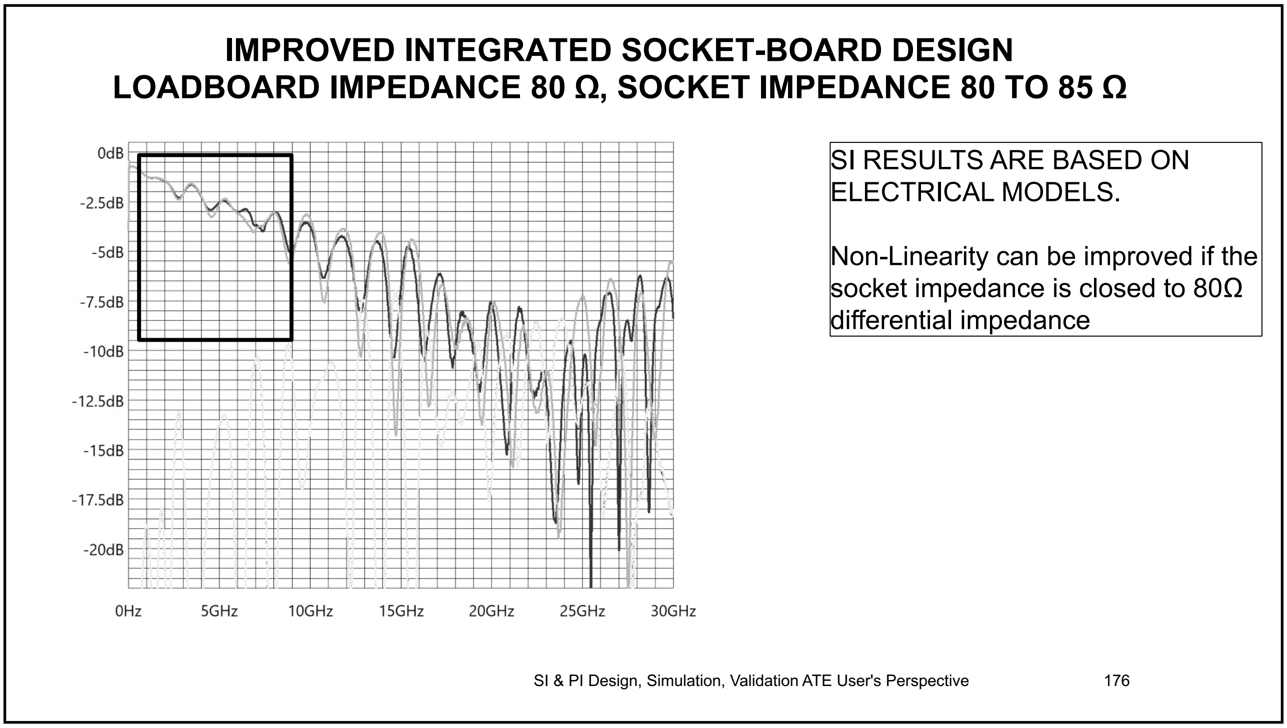




SOCKET-BOARD INTEGRATION

- With reduced resonance at board impedance at 80 Ω.
- Loop Back Circuit adjusted to 80 Ω +5, -5Ω.
- PCB Vendor Load Board model is now ~80 Ω.
- DFE=64 can be attained majority of the time instead of DFE=256 full count.
- Non-Linearity can be improved with lower impedance close to 80Ω.
- Non-Linearity can get worse with socket-degradation as a function of insertion.

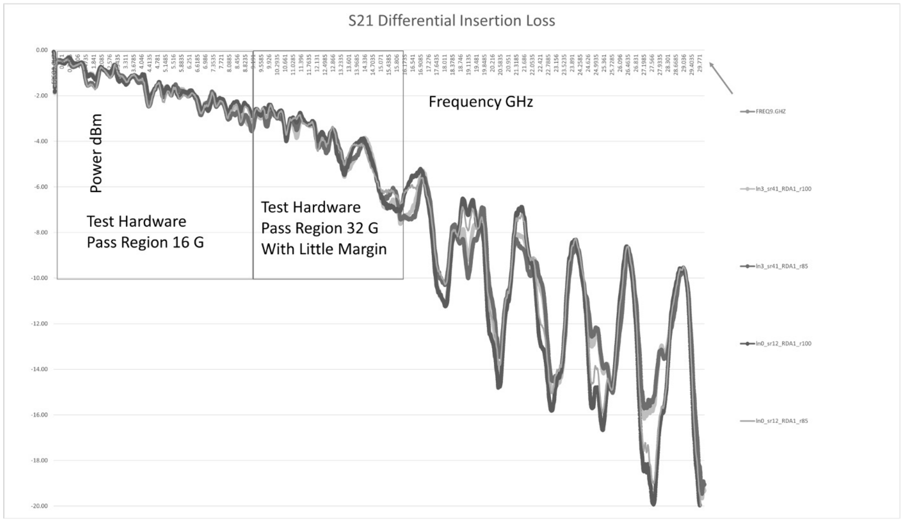
IMPROVED INTEGRATED SOCKET-BOARD DESIGN
LOADBOARD IMPEDANCE 80 Ω, SOCKET IMPEDANCE 80 TO 85 Ω



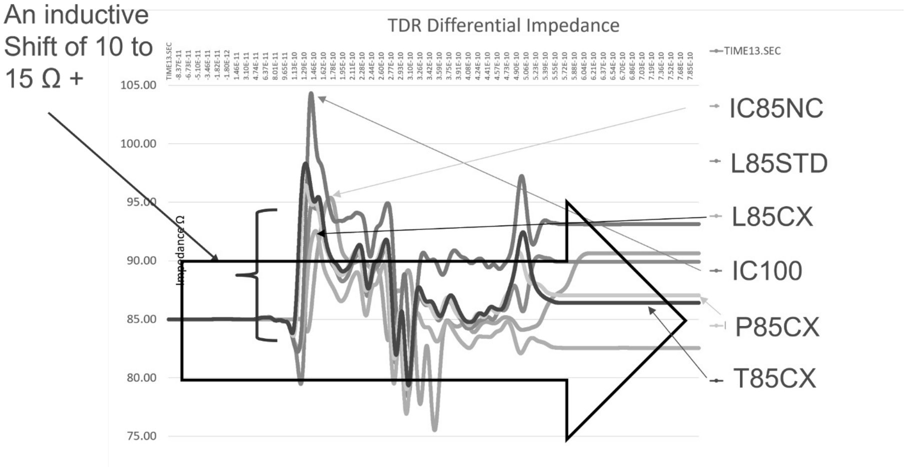
SI RESULTS ARE BASED ON ELECTRICAL MODELS.

Non-Linearity can be improved if the socket impedance is closed to 80Ω differential impedance

Tunis Test Signal Integrity (SI) Socket Validation Insertion Loss reference at 100 Ω, 85 Ω Sockets : RDA1, Lane 0 & 3, Surrogates 41,12

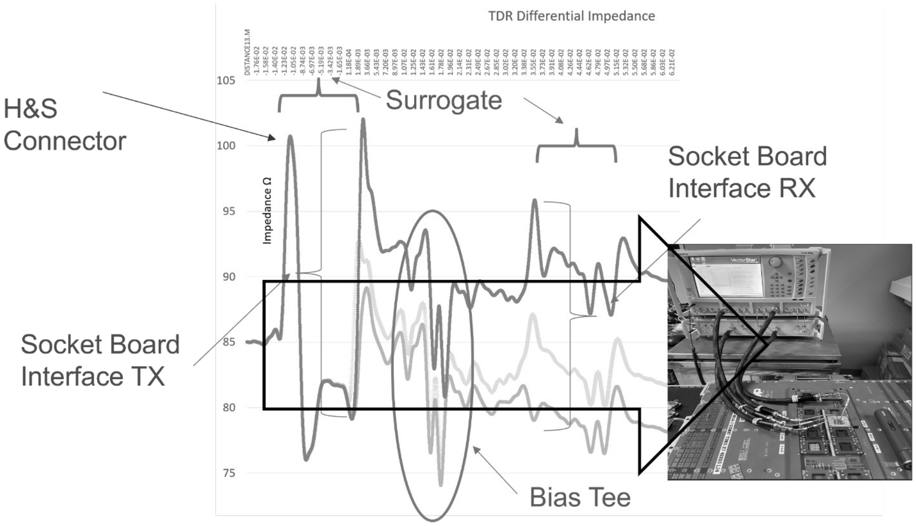


TDR Differential Impedance; Surrogate not included to de-embedding. Time-Gated before Test Socket-TX, and after Socket-RX; 30 GHz; Ref=85 Ω



Observations:
- The profile is normalized to the circuit.
- Partial Capacitive reactance at ball-Pogo interface.
- Inductive reactance at socket-board interface.
- Impedance anomalies at the bias-tee routing.

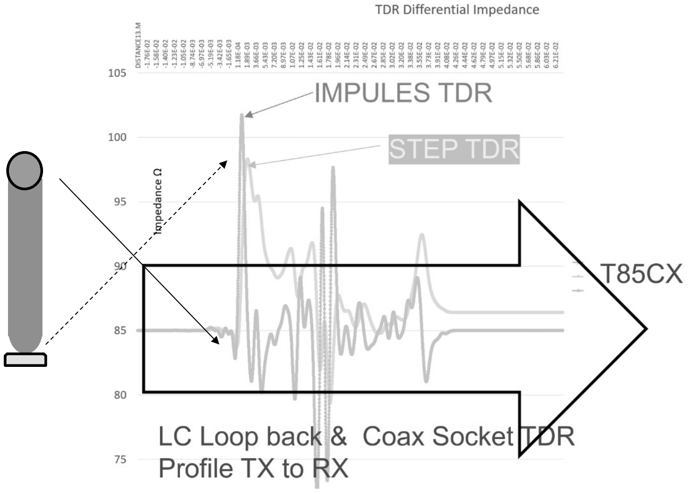
TDR Differential Impedance; Surrogate not included to de-embedding. No time gate before Test Socket-TX, and after Socket-RX; 30 GHz



Observations:

- The profile is normalized to the circuit.
- Partial Capacitive reactance at ball-Pogo interface.
- There is no massive shift of impedances over 120 Ω or magnitude shift 20 Ω or even higher.
- Cohu STD socket remains highly inductive.

TDR Differential Impedance; Surrogate not included to de-embedding. Time-Gated before Test Socket-TX, and after Socket-RX; 30 GHz

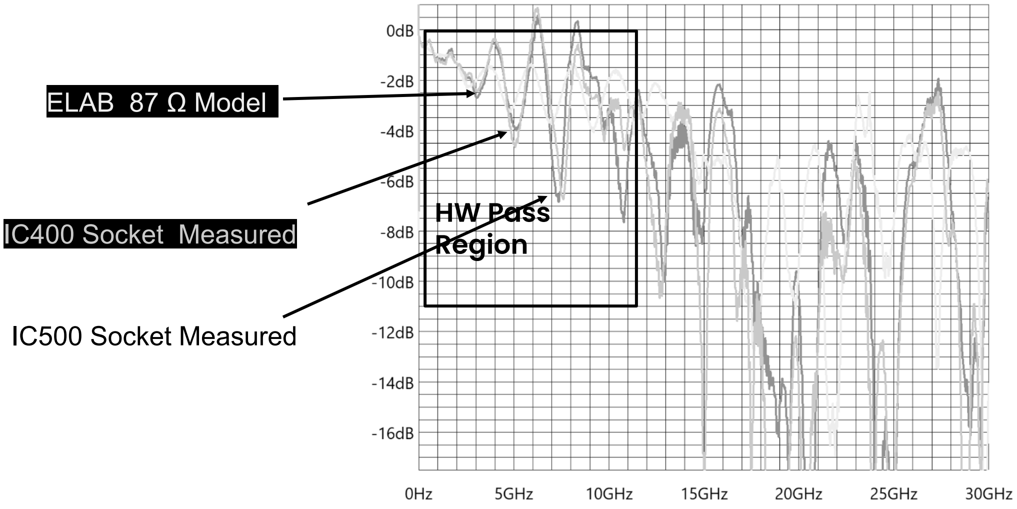


Observations:

- IMPULES TDR: Are the discrete events or occurrences of discontinuities along the transmission line.
- STEP TDR: Is the integral effect of the discontinuities along the signal path.
- Take note that IMPULSE are ahead of the STEP plots as it should be.

FOUR SOCKET MODELS ON A SINGLE IP
ELAB87 (87Ω),
ES90,IC400, IC500 (90Ω)

SYP IP , Package, Socket, Board Integration with 220nf bypass Lane-0 Zero Cyle PCB=90Ω

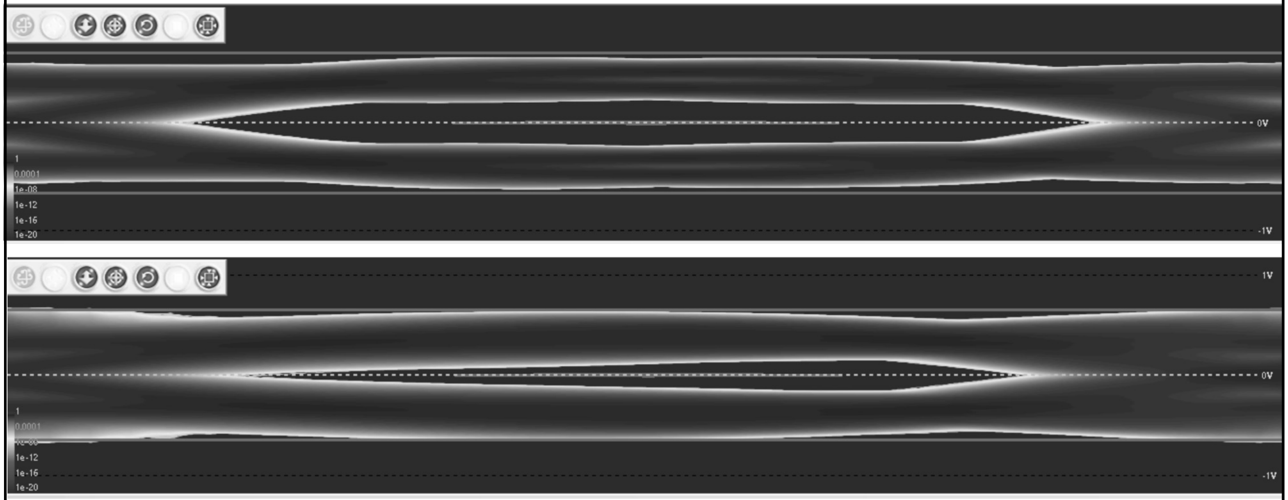


ELAB 87 Ω Model

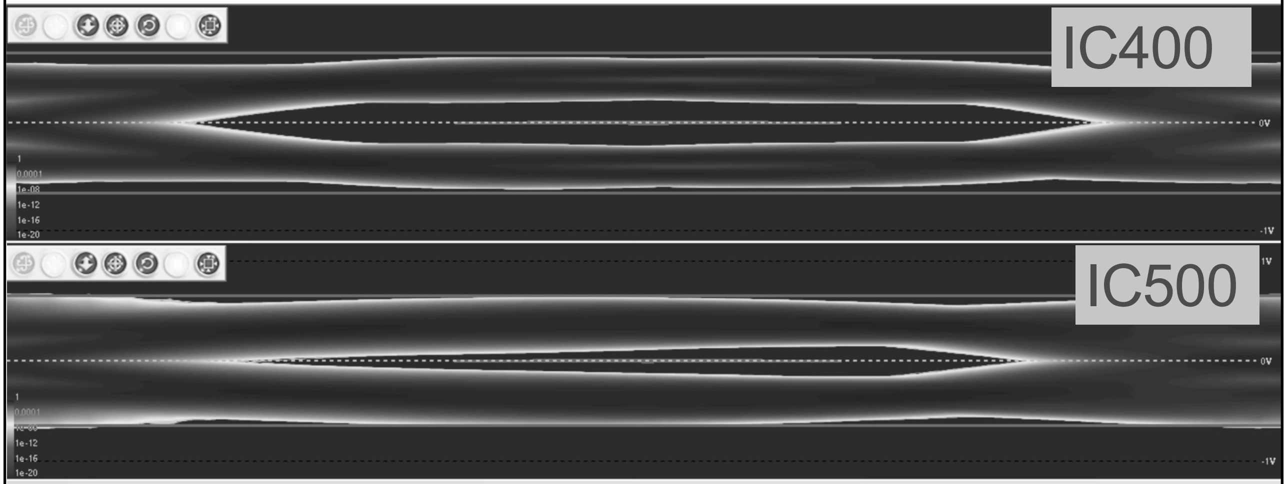
IC400 Socket Measured

IC500 Socket Measured

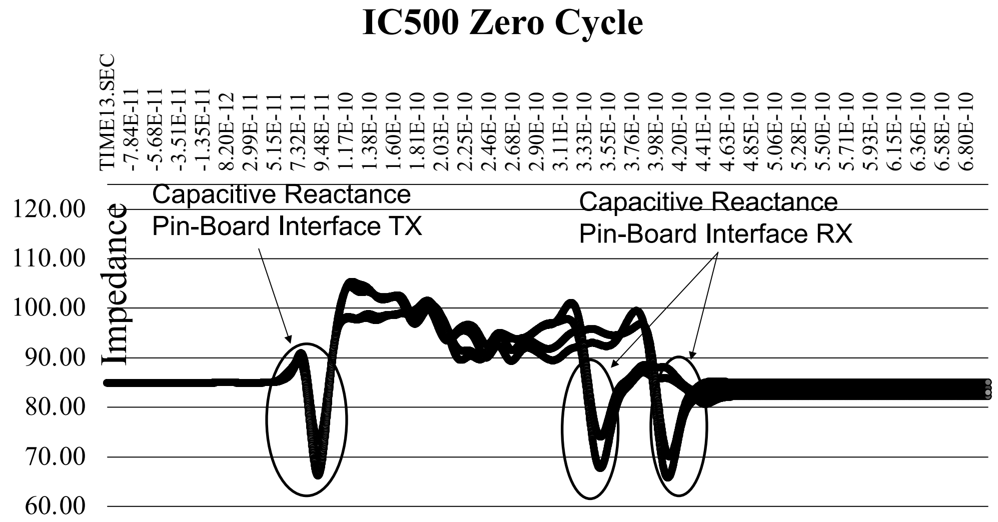
Complete Circuit Integration: IC400 and IC500 both Zero-Cycle. PRBS31, 18G, EQUAL=Disabled, DFE=8, CTLE=Enabled



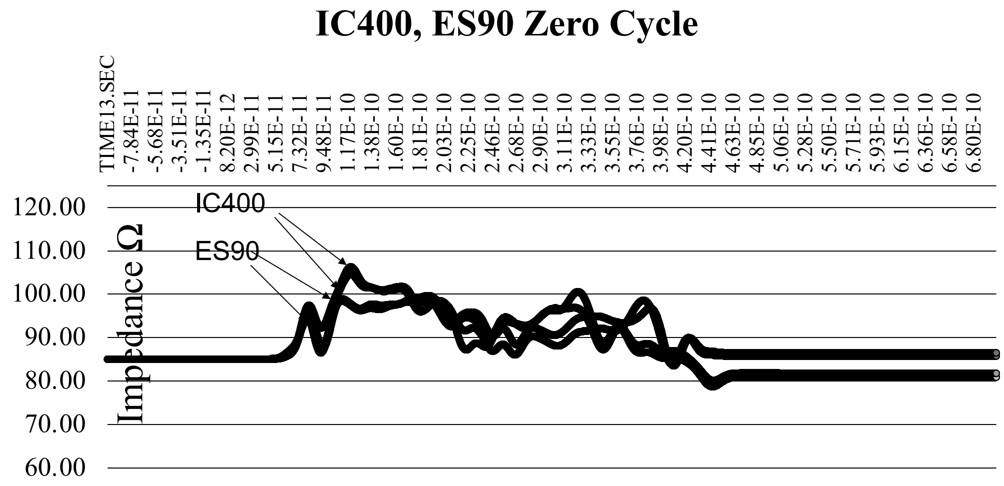
Both test socket results to Bin1 up to 33K cycles + Measured Transmission Line



IC500 Zero Cycle Measured



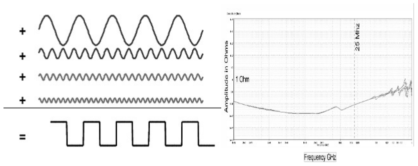
IC400, ES90 Socket Zero Cycle Measured



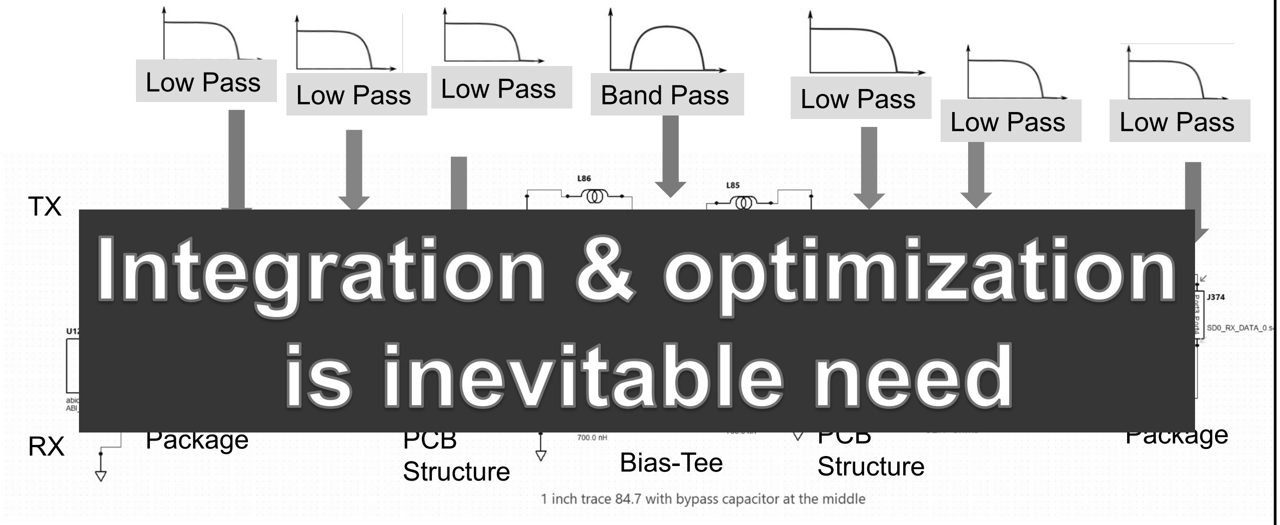
SI Summary

TestConX™

Mesa, Arizona ● March 1–4, 2026



Integrated Filters; Merge of transmission line segments



Integration & optimization is inevitable need

ANALYTICAL APPROACH TO HARDWARE INTEGRATION

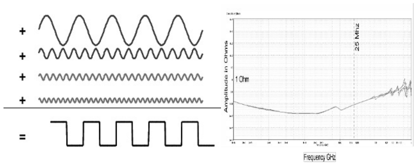
- **ANALYTICALLY MODELED-SIMULATED CIRCUIT CONFIGURATION IS THE PREFERRED METHOD. INTEGRATED MODELED TRANSMISSION LINE SEGMENTS.**
- **HARDWARE PROVIDERS IS SHORT OF INFORMATION TO BEST OR OPTIMIZE CIRCUIT FOR PRODUCTION TESTING.**
  - SOCKET VENDORS DO NOT KNOW
  - PCB VENDORS DO NOT KNOW
  - COMPONENT VENDORS DO NOT KNOW
- **THE CURRENT PROCEDURE OF RELYING ON VENDOR MODELING AND SIMULATION IS INSUFFICIENT AT BEST.**
  - FRAGMENTED RESULTS DON'T ADD UP IT CREATE RESONANT CIRCUITS.
- **PACKAGE ELECTRICAL DESIGN RULES IS NOT ALWAYS THE BEST OPTIMIZE PERFORMANCE FOR PRODUCTION TEST**
  - UFS RECOMMENDED IMPEDANCE 100 Ω. TEST ENGINEERING MODELING AND SIMULATION RESULTED LOWER IMPEDANCE IS BETTER (80 TO 85 Ω)
  - PCIE RECOMMENDED IMPEDANCE IS 85 Ω. CIRCUIT MODELING AND SIMULATION INDICATED 80 Ω BELOW 85 AND ABOVE 75.

The Need to Develop Hardware Provider (Socket, Board, Components)

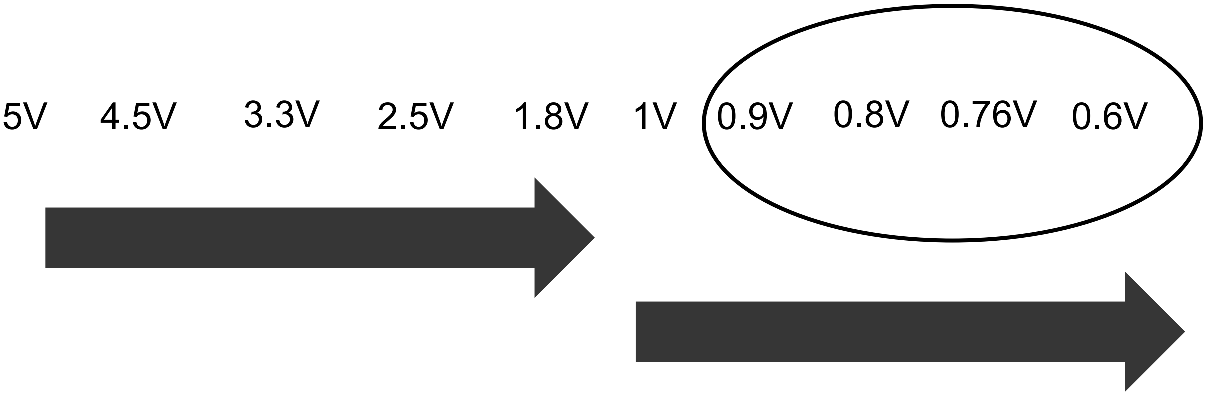
- Need an INTEGRATED HARDWARE PROVIDER
  - Socket, Board, Components
  - Signal Integrity
  - Power Integrity
- Need for alternative HW Design and Fabrication
  - Exposure to cost
  - Capacity
  - Mistakes
    - Inductive Spikes Loop Back Circuit, Via-manufacturing excursion Discovered in VNA Lab early January, & June 2025
- Need new HW Design and strong SI, PI, and Validation capability(Total Ownership)

Power Integrity

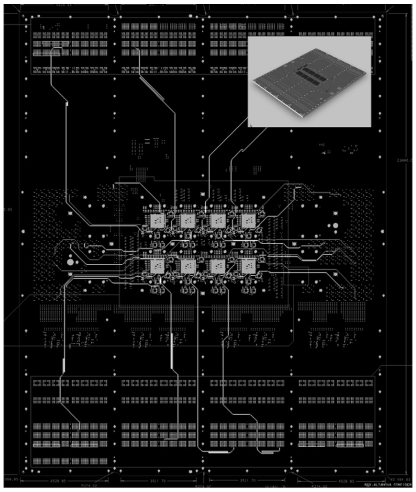
Mesa, Arizona ● March 1–4, 2026



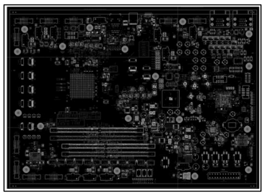
Power Integrity



5V 4.5V 3.3V 2.5V 1.8V 1V 0.9V 0.8V 0.76V 0.6V

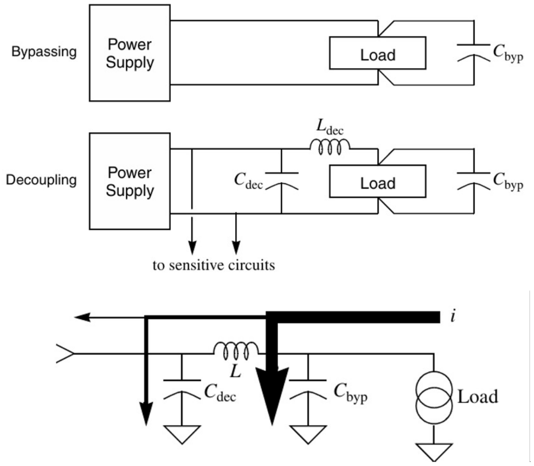


8 Site ATE Load Board
- $250K Dev Cost
- 80 Layers
- $40K to $60K/Unit
- 300 mils thick
- Low Dielectric Material
- At speed test for high speed I/O
- Advance ATE Instrumentation
- Advance ATE DPS



Application Board
- Single Site
- $10K/Unit
- 10 to 12 layers
- Manuel Test
- Connector to instrument interface
- PC or LAB PSU

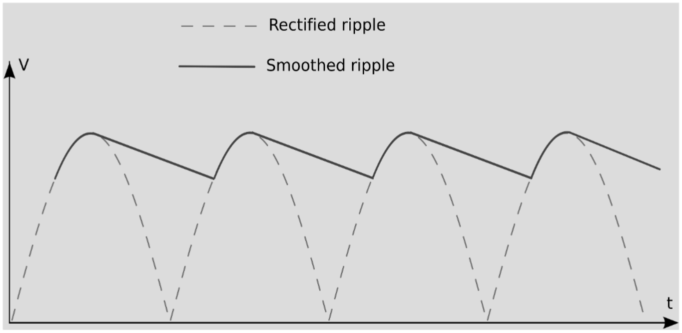
Power Filter Concepts for PLLs and IP Isolation



Bypassing is the reduction of high frequency current flow in a high impedance path by shunting that path with a bypass, usually a capacitor (in this case, Cbyp). Bypassing is used to reduce the noise current on power supply lines.

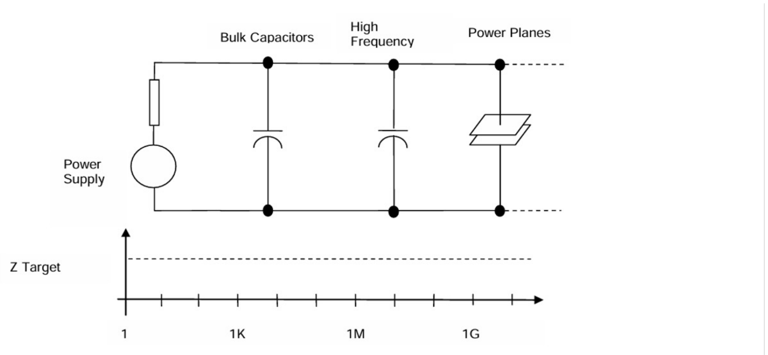
Decoupling is the isolation of two circuits on a common line. The decoupling network is usually a low pass filter and the isolation is rarely equal in both directions. Decoupling is used to prevent transmission of noise from one circuit to another. In the figure a bypass capacitor, Cbyp, is shown along with the decoupling circuit, Ldec and Cdec. This is because in practice bypassing is always used when decoupling.

What is the ripple voltage requirement for DUT



A typical case: ripple of 2.5%, VDD = 1.2 V, and current = 500 mA:
Target Impedance = V DD (I MIN DD ( ) * Ripple MAX) = 1 . 2 * 0 .
0 . 025 500 = 60 m Ω

$$\text{Target Impedance} = \frac{V_{DD}(MIN) * Ripple}{I_{DD}(MAX)} = \frac{1.2 * 0.025}{0.500} = 60m\Omega$$



Flat target impedance vs. frequency, and decoupling elements frequency range

Calculating the Total Required Bulk Capacitance (VDDINT)

Allow a drop of no more than 2.5% in VDD (for example, 82.5 mV for a 3.3V supply, or 30 mV for a 1.2V supply

To find the required, total supply bypass capacitance, treat the processor as a “noise generator” of a known source impedance. Then determine the capacitive reactance necessary to bypass this source impedance, keeping the terminal noise voltage within the data sheet limits. This is sometimes referred to as “target impedance”. The difficulty with this approach is the ill-defined nature of the internal core load impedance, represented by the processor; a conservative approximation assumes that the minimum impedance can not be less than the minimum supply voltage divided by the maximum load current stated in the data sheet.

VDD = 1.2 V and current = 500 mA

$$\left|Z_{DSP}\right| \geq \frac{V_{DD}(MIN)}{I_{DD}(MAX)} = \frac{1.2}{500mA} = 2.4\Omega$$

If we know the processor’s supply tolerance (typically ±5%) and the voltage regulator accuracy and frequency response (typically ±2.5% and 100 kHz, respectively), we can determine the minimum total bypass capacitance within the limits for the processor, as follows:

$$C_{BPTOT} = \frac{I_{DD}(MAX)}{2f \times ripple \times V_{DD}(MIN)} F$$

Example: processor core voltage (VDDINT) = 1.2 V, IDDINT = 500 mA. Hence, ZDSP ≥ 2.4 Ω and ZTARGET < 60 mΩ.)

$$C_{BPTOT} \geq \frac{500(mA)}{2 \times 100(kHz) \times 0.025 \times 1.2(V)} \mu F$$

$$C_{BPTOT} \geq 83.3\mu F$$

If the maximum change in IDD is known, we can determine the minimum total bypass capacitance. For example, if the change in processor load current from IDD(MIN) to IDD(MAX) is determined to be 250 mA, the minimum capacitance can be found, as follows

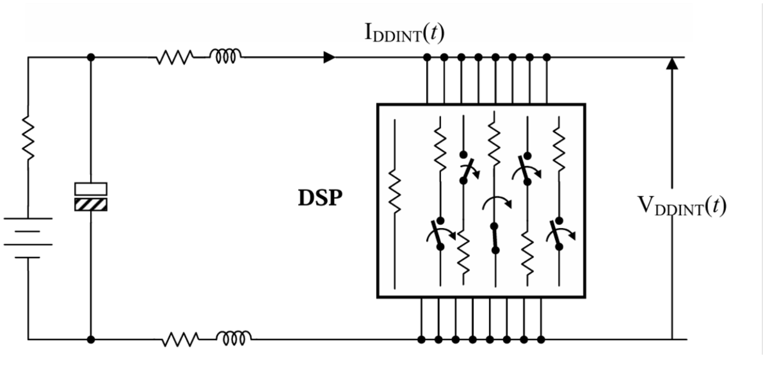
$$C_{BP(MIN)} = \Delta I_{DD} \times \frac{\Delta t}{\Delta V_{DD}} \quad F$$

$$\Delta I_{DD} = I_{DD}(MAX) - I_{DD}(MIN)$$
$$\Delta t = Power\ Supply\ Response\ Time$$
$$\Delta V_{DD} = Max\ Permitted\ Voltage\ Sag$$

$$C_{BP(MIN)} = 250\,(mA) \times \frac{10\,(\mu s)}{82.5\,(mV)}\ \mu F$$

$$\therefore C_{BP} \geq 30.3\mu F$$

(BOARD PARASITIC): Another consideration in determining an effective bypassing strategy is the effect of the parasitic inductance and resistance associated with component packages and mounting methods.



Switched resistor approximation of noise model
High Frequency VDDINT Bypassing – Noise Generator and Equivalent Circuit

$$\left(\frac{X_C}{Z_{DSP}(MIN)}\right) \le \left(\frac{\delta V_{DD}}{V_{DDINT}}\right)$$

$$\frac{1}{2\pi f_{MIN}\, C_{BP} \times Z_{DSP}(MIN)} \le \left(\frac{\delta V_{DD}}{V_{DDINT}}\right)$$

$$\frac{I_{DDINT}(MAX)}{2\pi f_{MIN}\, C_{BP} \times Z_{DSP}(MIN)} \le \left(\frac{\delta V_{DD}}{V_{DDINT}}\right)$$

$$C_{BP} \ge \frac{I_{DDINT}(MAX) \times V_{DDINT}}{(2\pi f_{MIN} \times V_{DDINT} \times \delta V_{DD})}$$

$$C_{BP} \ge \frac{I_{DDINT}(MAX)}{(2\pi f_{MIN} \times \delta V_{DD})} \quad F$$

Processor with typical operating conditions so that VDDINT = 1.2 V and IDD(MAX) = 1.1 A, at a minimum core clock frequency of 100 MHz. This device is available in a 136-ball BGA package with 13 balls allocated to VDDINT. Let the required ripple factor (RF) be 2.5%; therefore, δVDD = 30 mV.

Distribute 16 capacitors on device package-pins.

$$C_{BP} = \frac{1.1}{\left(2 \times \pi \times 100 \times 10^{6} \times 30 \times 10^{-3}\right)}$$

$$\therefore C_{BP} = 58.4 \quad nF$$

$$C_{BP}' = \frac{C_{BP}(nF)}{n} \quad nF$$

$$C_{BP}' = \frac{58.4}{16}$$

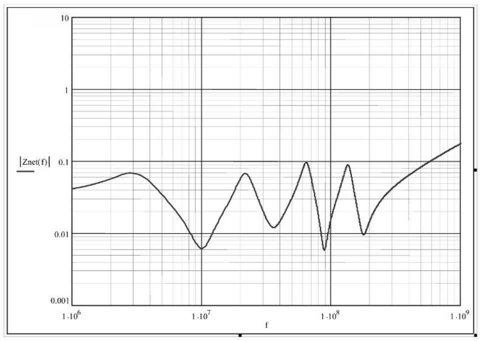
$$\therefore C_{BP}' = 3.65 \quad nF$$

Use multiple copies of standard capacitors 3.9nf

Bypassing and impedance

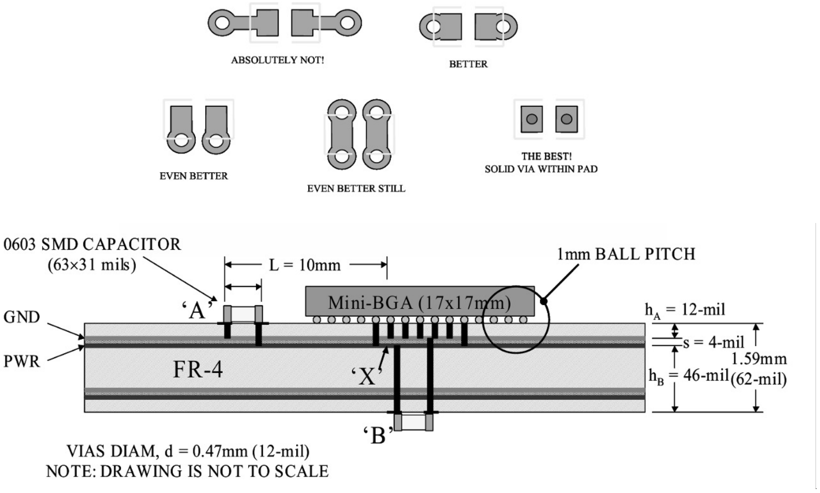
$$|Z_C(f)| = \sqrt{(ESR)^2 + \left(\omega(ESL) - \frac{1}{(\omega C)}\right)^2}$$

C_0	20 × 680 pF, NP0 ceramic, assume ESL ≅1.2 nH, ESR ≅ 200 mΩ
C_1	10 × 2.7 nF, NP0 ceramic, assume ESL ≅1.2 nH, ESR ≅ 60 mΩ
C_2	12 × 10 nF, X7R ceramic, assume ESL ≅ 2 nH, ESR ≅ 150 mΩ
C_3	8 × 100 nF, X7R ceramic, assume ESL ≅ 2.5 nH, ESR ≅ 50 mΩ
C_4	4 × 2.2 µF, tantalum, assume ESL ≅ 10 nH, ESR ≅ 150 mΩ



Example: capacitor net impedance magnitude vs. frequency

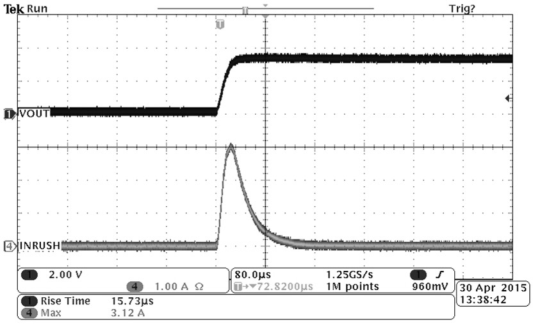
PCB Layout and Capacitor Mounting

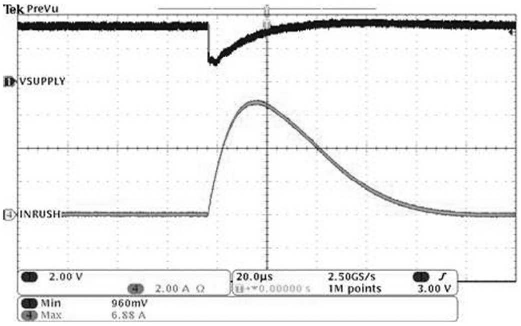


ATE Power Integrity Intricacies

- DUT supply at .8V to .5V with currents 30A, 100A, 500A+
- Low impedance from DSP(Device Power Supplies) to the DUT(Device under test) power pins
  - Compliance to ripple factor is a huge challenge for power delivery
- Site to Site correlation is an absolute necessity
  - Avoid False Failures
  - All sites Power delivery profiles are similar

In rush current and voltage droop





Site to site correlation is absolute necessity

DUT1 Power Supply Impedance Table

21.08mΩ

S.No.	Supply Name	Current (A)_30%-GB	Voltage (V)	V-5% (V)	Imp-5% @DC Ω	Impedance (mΩ) At 25MHz							Site-Site Deviation
						Site 0	Site 1	Site 2	Site 3	Site 4	Site 5	Site 6	
1	VDD_SOC	21.00072	0.9	0.045	0.002	21.56	20.89	20.76	20.87	21.08	20.78	21.09	0.26
2	NVCC_AON	0.033384	3.3	0.165		246.76	246.70	250.47	244.57	249.86	245.63	246.78	1.99
3	NVCC_BBSM_1P8	0.029172	1.8	0.090		297.61	277.04	291.49	283.02	291.08	282.59	286.46	6.37
4	NVCC_CCM_DAP	0.090324	3.3	0.165		275.95	275.91	278.79	266.56	282.31	267.06	273.31	5.39
5	NVCC_ENET	0.200772	3.3	0.165		171.31	170.43	171.46	169.33	172.98	169.42	172.85	1.37
6	NVCC_ENET1	0.200772	3.3	0.165		193.47	177.92	184.35	179.35	196.13	180.51	182.59	6.59
7	NVCC_GPIO	0.256308	3.3	0.165		[illegible]	[illegible]	[illegible]	100.94	101.70	101.71	102.53	0.69
8	NVCC_SD2	0.104988	3.3	0.165		[illegible]	[illegible]	[illegible]	235.44	242.79	234.78	235.95	4.17
9	NVCC_WAKEUP	0.128544	3.3	0.165		202.62	202.83	204.05	202.16	203.16	203.01	203.52	0.57
10	VDD2H_DDR	0.65	1.1	0.055		317.31	321.48	332.55	314.09	334.73	316.51	326.48	7.53
11	VDDQ_DDR	4.55	0.6	0.030	0.007	99.01	93.77	103.10	97.94	98.21	93.44	96.02	3.09
12	VDD_ANA_0P8	0.104864565	0.8	0.040		124.84	125.06	126.10	124.45	125.99	124.66	124.58	0.63
13	VDD_ANA_1P8	0.052503477	1.8	0.090		140.21	134.69	144.69	137.19	146.94	135.50	140.62	4.26
14	VDD_ANAVDET_1P8	0.000205218	1.8	0.090		206.50	193.01	212.72	190.45	208.41	198.87	199.36	7.60
15	VDD_BBSM_0P8_CAP	0.018719688	0.8	0.040		178.63	177.78	179.00	177.02	178.71	177.84	177.93	0.64
16	VDD_DDR_0P8	2.6	0.8	0.040	0.015	102.92	99.50	111.78	108.78	112.91	99.39	106.37	5.13
17	VDD_LVDS_1P8	0.395928	1.8	0.090		257.20	247.91	266.07	246.60	266.14	252.95	273.47	9.46
18	VDD_ETH_0P8	0.23712	0.8	0.040		[illegible]	[illegible]	[illegible]	135.31	148.59	138.46	141.17	4.33
19	VDD_ETH_1P8	0.105768	1.8	0.090		[illegible]	[illegible]	[illegible]	191.07	193.17	189.73	191.15	1.00
20	VDD_PCI_0P8	0.089811353	0.8	0.040		252.81	249.19	253.17	253.31	251.49	246.10	252.40	2.46
21	VDD_PCI_1P8	0.076145316	1.8	0.090		185.31	183.07	189.40	183.24	185.23	184.20	188.25	2.25
22	VDD_USB_0P8	0.07883492	0.8	0.040		172.55	167.19	170.28	169.79	167.61	173.86	167.75	2.39
23	VDD_USB_1P8	0.030409408	1.8	0.090		296.11	303.30	286.86	294.95	293.98	296.03	305.24	5.66
24	VDD_USB_3P3	0.203144347	3.3	0.165		285.42	284.29	288.33	286.25	291.70	284.18	288.51	2.52
25	VREFH_1P8_ADC	0.003588	1.8	0.090		398.12	396.66	414.26	396.25	407.71	398.79	398.58	6.32

99.01m Ω

102.92 mΩ

DUT 2 Supply DC Resistance Table

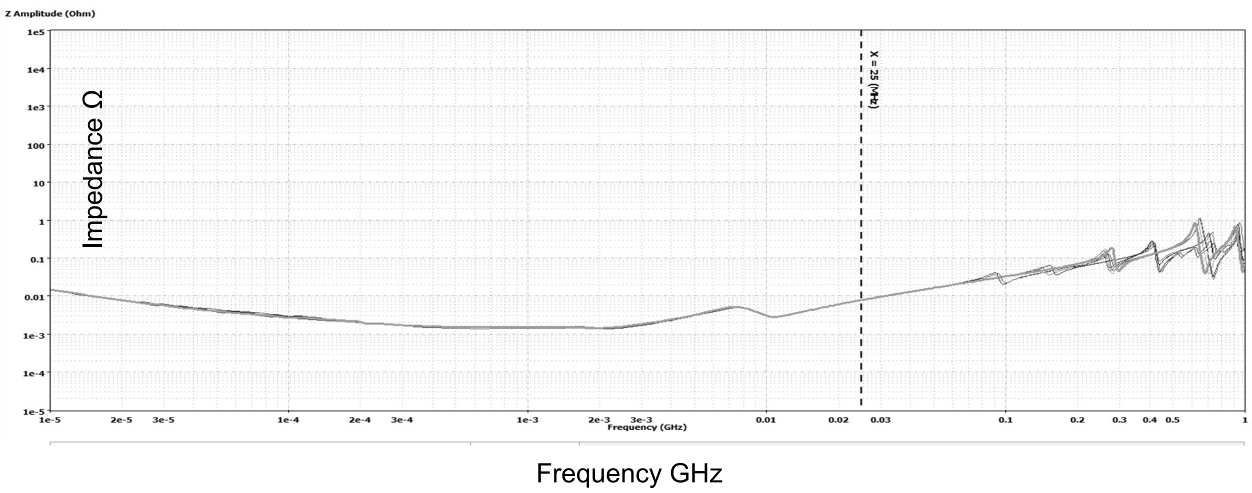
2.143 mΩ

6.593 mΩ

15.385 mΩ

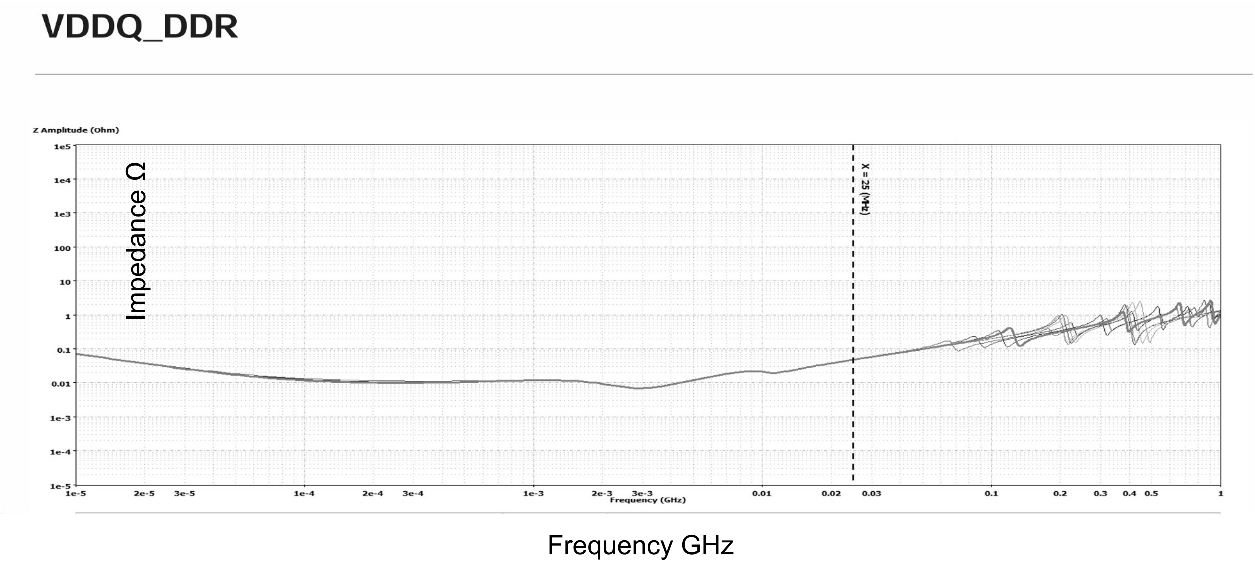
S.No.	Supply Name	Current (A)_30%	Voltage (V)	V-5% V	R-5% Ω	DCR (mΩ)							STD	3STD	Min	Max
						Site 01	Site 02	Site 03	Site 04	Site 05	Site 06	Site 07				
1	VDD_SOC	21.001	0.9	0.045	2.143	1.74	1.24	1.93	1.22	2.04	1.06	1.09	0.417	1.251	1.055	2.043
2	NVCC_AON	0.033	3.3	0.165		20.16	16.63	25.39	16.01	26.98	14.26	14.52	5.211	15.632	14.256	26.979
3	NVCC_BBSM_1P8	0.029	1.8	0.09		31.94	20.41	47.52	19.24	38.19	19.65	21.37	11.162	33.487	19.242	47.516
4	NVCC_CCM_DAP	0.090	3.3	0.165		26.68	19.67	30.81	15.84	34.44	18.68	15.78	7.511	22.532	15.782	34.437
5	NVCC_ENET	0.201	3.3	0.165		[illegible]	18.76	39.06	14.23	30.44	16.73	28.25	8.998	26.995	14.231	39.061
6	NVCC_ENET1	0.201	3.3	0.165		[illegible]	[illegible]	41.94	16.54	42.57	17.26	22.98	12.111	36.333	16.540	42.572
7	NVCC_GPIO	0.256	3.3	0.165		[illegible]	[illegible]	31.86	12.98	31.48	14.17	17.40	8.501	25.502	12.984	31.856
8	NVCC_SD2	0.105	3.3	0.165		[illegible]	[illegible]	59.48	21.37	45.64	17.51	15.84	17.205	51.614	15.838	59.482
9	NVCC_WAKEUP	0.129	3.3	0.165		39.38	23.07	48.95	22.05	34.67	21.86	22.75	10.784	32.353	21.861	48.952
10	VDD2H_DDR	0.650	1.1	0.055		20.57	17.36	44.10	21.36	35.08	21.15	27.79	9.647	28.942	17.355	44.104
11	VDDQ_DDR	4.550	0.6	0.03	6.593	5.52	4.49	7.98	4.69	7.49	4.54	6.10	1.432	4.295	4.492	7.979
12	VDD_ANA_0P8	0.105	0.8	0.04		13.63	11.52	25.73	12.03	20.98	10.85	17.36	5.617	16.850	10.851	25.730
13	VDD_ANA_1P8	0.053	1.8	0.09		13.39	11.13	23.80	10.62	21.94	13.89	18.80	5.284	15.853	10.623	23.804
14	VDD_ANAVDET_1P8	0.000	1.8	0.09		35.12	15.60	32.76	14.15	35.01	16.44	14.14	10.329	30.988	14.137	35.117
15	VDD_BBSM_0P8_CAP	0.019	0.8	0.04		26.89	28.68	42.14	21.78	34.94	23.57	20.73	7.746	23.239	20.735	42.142
16	VDD_DDR_0P8	2.600	0.8	0.04	15.385	5.21	4.31	8.63	4.31	7.88	4.20	4.94	1.836	5.509	4.201	8.631
17	VDD_LVDS_1P8	0.396	1.8	0.09		22.78	19.92	33.73	18.61	26.97	18.89	32.08	6.307	18.922	18.607	33.731
18	VDD_ETH_0P8	0.237	0.8	0.04		[illegible]	[illegible]	20.28	16.66	20.71	14.82	18.80	2.784	8.352	14.238	20.710
19	VDD_ETH_1P8	0.106	1.8	0.09		[illegible]	[illegible]	28.32	20.59	31.56	17.23	16.49	5.637	16.912	16.493	31.557
20	VDD_PCI_0P8	0.090	0.8	0.04		[illegible]	[illegible]	38.07	24.15	37.64	18.14	22.23	7.799	23.398	18.142	38.071
21	VDD_PCI_1P8	0.076	1.8	0.09		27.48	19.98	45.06	23.47	33.14	20.55	32.31	8.864	26.593	19.985	45.062
22	VDD_USB_0P8	0.079	0.8	0.04		21.48	18.15	44.53	24.83	43.57	18.78	26.19	11.203	33.609	18.153	44.527
23	VDD_USB_1P8	0.030	1.8	0.09		8.29	7.67	9.21	7.84	10.26	6.56	8.25	1.176	3.529	6.562	10.261
24	VDD_USB_3P3	0.203	3.3	0.165		15.47	19.94	30.17	22.55	26.79	17.24	28.27	5.670	17.010	15.473	30.169
25	VREFH_1P8_ADC	0.004	1.8	0.09		26.25	19.16	27.18	17.60	26.82	17.86	17.66	4.675	14.025	17.605	27.180

Multi-Site SOC VDD PDN

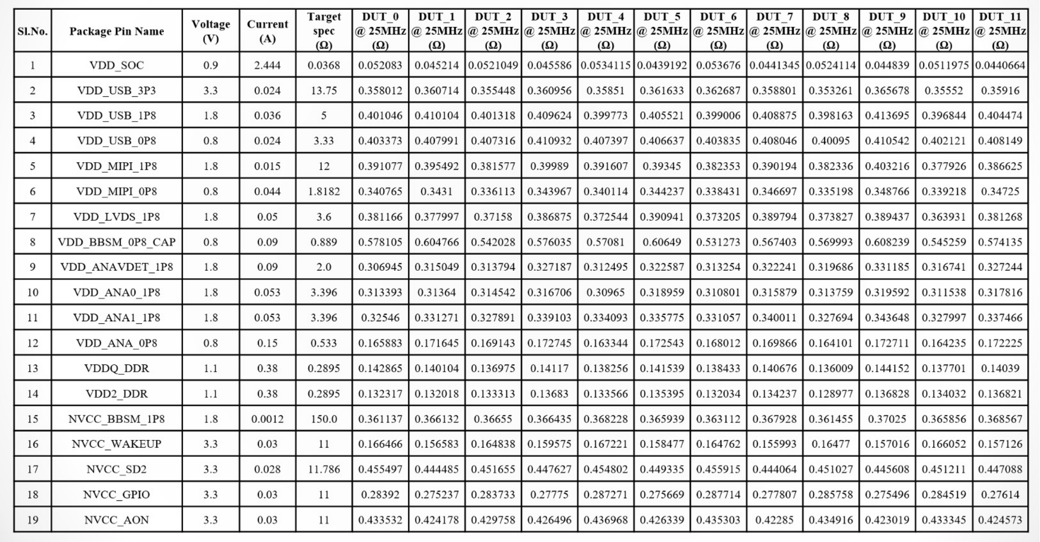


Multi-Site SOC VDD_DDR PDN

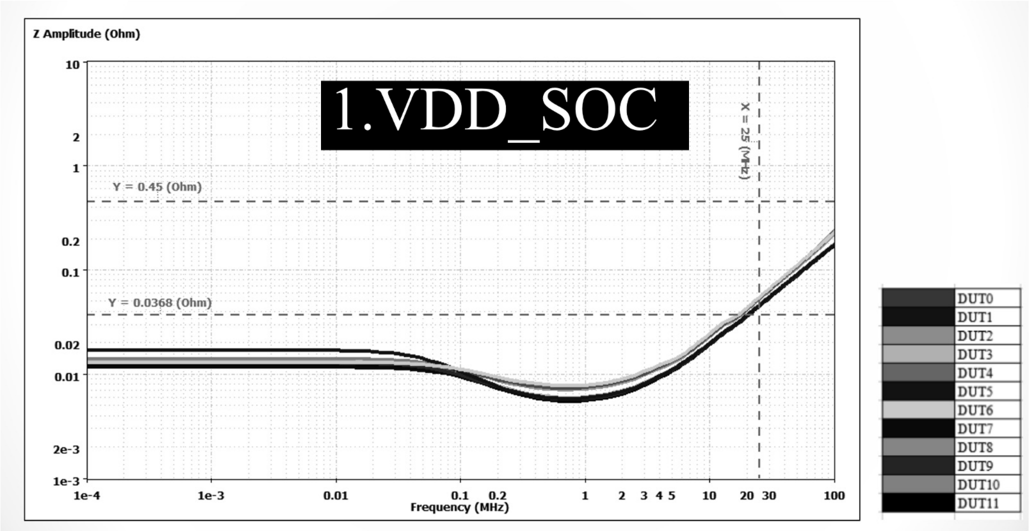
VDDQ_DDR



PDN Table per site @ 25MHz

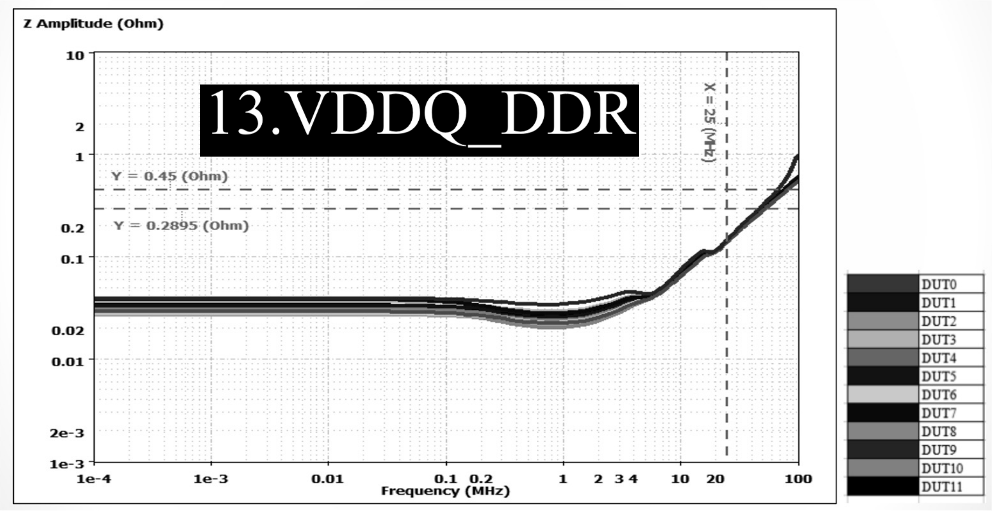


Sl.No.	Package Pin Name	Voltage (V)	Current (A)	Target spec (Ω)	DUT_0 @ 25MHz (Ω)	DUT_1 @ 25MHz (Ω)	DUT_2 @ 25MHz (Ω)	DUT_3 @ 25MHz (Ω)	DUT_4 @ 25MHz (Ω)	DUT_5 @ 25MHz (Ω)	DUT_6 @ 25MHz (Ω)	DUT_7 @ 25MHz (Ω)	DUT_8 @ 25MHz (Ω)	DUT_9 @ 25MHz (Ω)	DUT_10 @ 25MHz (Ω)	DUT_11 @ 25MHz (Ω)
1	VDD_SOC	0.9	2.444	0.0368	0.052083	0.045214	0.0521049	0.045586	0.0534115	0.0439192	0.053676	0.0441345	0.0524114	0.044839	0.0511975	0.0440664
2	VDD_USB_3P3	3.3	0.024	13.75	0.358012	0.360714	0.355448	0.360956	0.35851	0.361633	0.362687	0.358801	0.353261	0.365678	0.35552	0.35916
3	VDD_USB_1P8	1.8	0.036	5	0.401046	0.410104	0.401318	0.409624	0.399773	0.405521	0.399006	0.408875	0.398163	0.413695	0.396844	0.404474
4	VDD_USB_0P8	0.8	0.024	3.33	0.403373	0.407991	0.407316	0.410932	0.407397	0.406637	0.403835	0.408046	0.40095	0.410542	0.402121	0.408149
5	VDD_MIPI_1P8	1.8	0.015	12	0.391077	0.395492	0.381577	0.39989	0.391607	0.39345	0.382353	0.390194	0.382336	0.403216	0.377926	0.386625
6	VDD_MIPI_0P8	0.8	0.044	1.8182	0.340765	0.3431	0.336113	0.343967	0.340114	0.344237	0.338431	0.346697	0.335198	0.348766	0.339218	0.34725
7	VDD_LVDS_1P8	1.8	0.05	3.6	0.381166	0.377997	0.37158	0.386875	0.372544	0.390941	0.373205	0.389794	0.373827	0.389437	0.363931	0.381268
8	VDD_BBSM_0P8_CAP	0.8	0.09	0.889	0.578105	0.604766	0.542028	0.576035	0.57081	0.60649	0.531273	0.567403	0.569993	0.608239	0.545259	0.574135
9	VDD_ANAVDET_1P8	1.8	0.09	2.0	0.306945	0.315049	0.313794	0.327187	0.312495	0.322587	0.313254	0.322241	0.319686	0.331185	0.316741	0.327244
10	VDD_ANA0_1P8	1.8	0.053	3.396	0.313393	0.31364	0.314542	0.316706	0.30965	0.318959	0.310801	0.315879	0.313759	0.319592	0.311538	0.317816
11	VDD_ANA1_1P8	1.8	0.053	3.396	0.32546	0.331271	0.327891	0.339103	0.334093	0.335775	0.331057	0.340011	0.327694	0.343648	0.327997	0.337466
12	VDD_ANA_0P8	0.8	0.15	0.533	0.165883	0.171645	0.169143	0.172745	0.163344	0.172543	0.168012	0.169866	0.164101	0.172711	0.164235	0.172225
13	VDDQ_DDR	1.1	0.38	0.2895	0.142865	0.140104	0.136975	0.14117	0.138256	0.141539	0.138433	0.140676	0.136009	0.144152	0.137701	0.14039
14	VDD2_DDR	1.1	0.38	0.2895	0.132317	0.132018	0.133313	0.13683	0.133566	0.135395	0.132034	0.134237	0.128977	0.136828	0.134032	0.136821
15	NVCC_BBSM_1P8	1.8	0.0012	150.0	0.361137	0.366132	0.36655	0.366435	0.368228	0.365939	0.363112	0.367928	0.361455	0.37025	0.365856	0.368567
16	NVCC_WAKEUP	3.3	0.03	11	0.166466	0.156583	0.164838	0.159575	0.167221	0.158477	0.164762	0.155993	0.16477	0.157016	0.166052	0.157126
17	NVCC_SD2	3.3	0.028	11.786	0.455497	0.444485	0.451655	0.447627	0.454802	0.449335	0.455915	0.444064	0.451027	0.445608	0.451211	0.447088
18	NVCC_GPIO	3.3	0.03	11	0.28392	0.275237	0.283733	0.27775	0.287271	0.275669	0.287714	0.277807	0.285758	0.275496	0.284519	0.27614
19	NVCC_AON	3.3	0.03	11	0.433532	0.424178	0.429758	0.426496	0.436968	0.426339	0.435303	0.42285	0.434916	0.423019	0.433345	0.424573



Impedance Ω

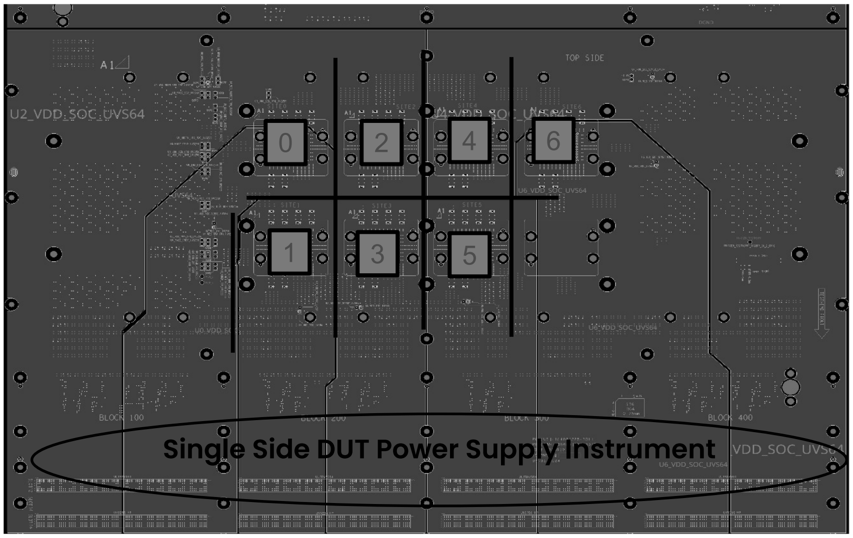
Frequency GHz



Impedance Ω

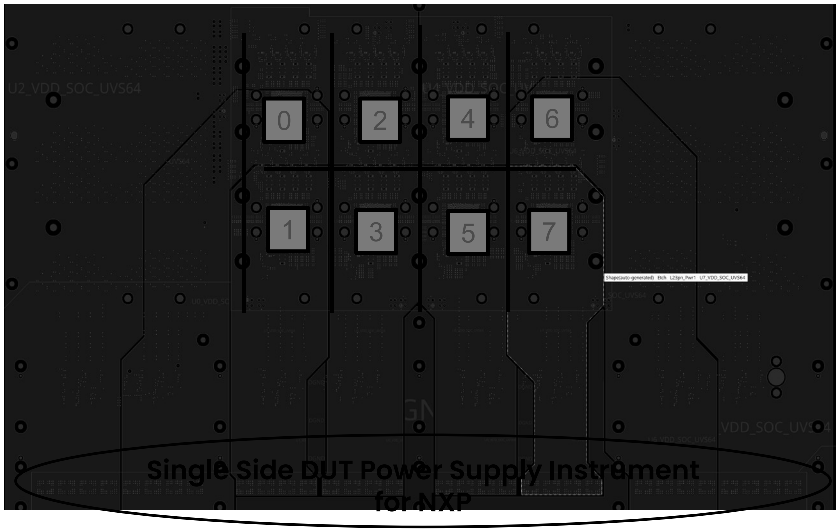
Frequency GHz

Power Plane design for multi-site(7) load board



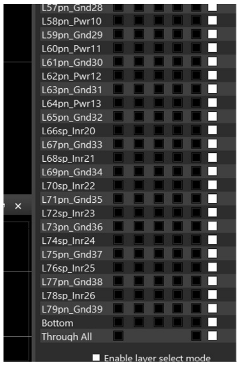
- Critical Geometries to ensure correlation between sites.
- ATE Symmetric instruments layout per associated sites.
- The entire power plane is used for a single DUT power, VDD.
- Additional layers for power distribution.

Power Plane design for multi-site(8) load board



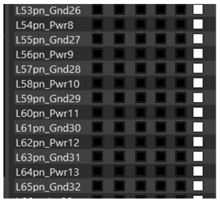
- Critical Geometries to ensure correlation between sites.
- ATE Symmetric instruments layout per associated sites.
- The entire power plane is used for a single DUT power, VDD.
- Additional layers for power distribution.

Additional power layers for low voltage SOC



L57pn_Gnd28
L58pn_Pwr10
L59pn_Gnd29
L60pn_Pwr11
L61pn_Gnd30
L62pn_Pwr12
L63pn_Gnd31
L64pn_Pwr13
L65pn_Gnd32
L66sp_Inr20
L67pn_Gnd33
L68sp_Inr21
L69pn_Gnd34
L70sp_Inr22
L71pn_Gnd35
L72sp_Inr23
L73pn_Gnd36
L74sp_Inr24
L75pn_Gnd37
L76sp_Inr25
L77pn_Gnd38
L78sp_Inr26
L79pn_Gnd39
Bottom
Through All
☐ Enable layer select mode

L22pn_Gnd11
L23pn_Pwr1 ☑
L24pn_Gnd12
L25pn_Pwr2
L26pn_Gnd13
L27pn_Pwr3
L28pn_Gnd14
L29pn_Pwr4
L30pn_Gnd15
L31pn_Pwr5
L32pn_Gnd16
L33pn_Pwr6
L34pn_Gnd17
L35sp_Inr11
L36pn_Gnd18



L53pn_Gnd26
L54pn_Pwr8
L55pn_Gnd27
L56pn_Pwr9
L57pn_Gnd28
L58pn_Pwr10
L59pn_Gnd29
L60pn_Pwr11
L61pn_Gnd30
L62pn_Pwr12
L63pn_Gnd31
L64pn_Pwr13
L65pn_Gnd32

The need for more power plane layers

- Power delivery requires precise power plane design.
- Additional layer count is inevitable.
- Electrical, mechanical complexities associated with thick boards.

70, 80+ layer PCB

Sound Engineering on PCB Stack Up

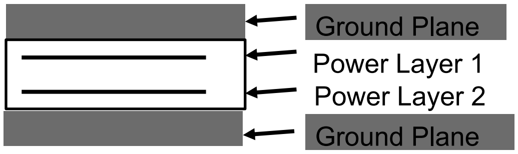
L18pn_Gnd9
L19sp_Inr9
L20pn_Gnd10
L21sp_Inr10
L22pn_Gnd11
L23pn_Pwr1 ☑
L24pn_Gnd12
L25pn_Pwr2
L26pn_Gnd13
L27pn_Pwr3
L28pn_Gnd14

Signal Planes In between Ground plane

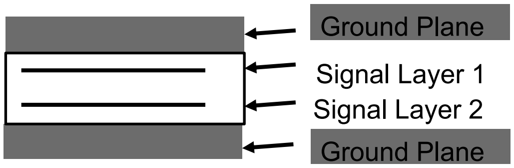
Power Planes In between Ground plane

- **Eliminate all sources of cross talk or undesired coupling.**
- **IP to IP crosstalk**
- **IP-Power to IP-power crosstalk**

No Double Stacking of Power Layer

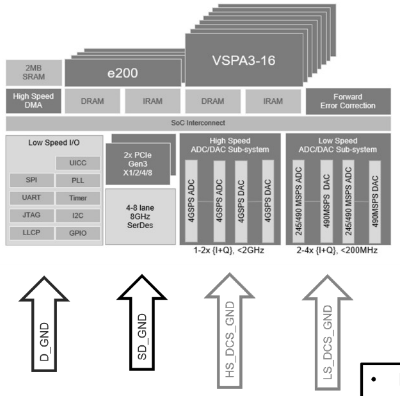


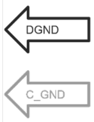
No Double Stacking of Signal Layer



300 mils,70, 80+ layer PCB

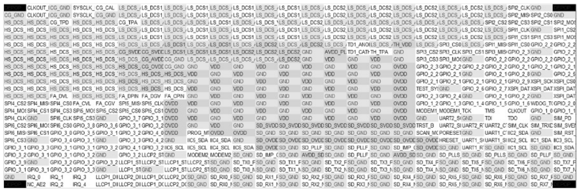
Noise Floor : Typical Mixed Signal Device





- Different power, ground domain as function of IP

1) DGND for Digital Core, and I/Os
2) SD_GND for high speed serdes
3) DCS_GND(LS_DCS_GND, HS_DCS_GND) for ADC/DAC IPS, and I/Os
4) CG_GND for Low Jitter reference clock



- Noise Floor sensitivity as a function of IP

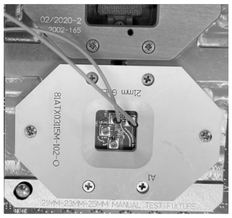
1) DGND for Digital Core, and I/Os < (-20dBm)
2) SD_GND for high speed serdes < (-30dBm)
3) DCS_GND(LS_DCS_GND, HS_DCS_GND) < (-90dB) or better
4) CG_GND for Low Jitter reference clock < (-140dBc), Phase Noise ~ 80femto seconds

Challenges

Common Challenges on mixed signal testing that are least understood

- **Noise floor and specific sensitivity as a function of IP (CORE, ADC, DAC, Serdes)**
- **Misconception of grounding rules on ATE**
- **How to manage device with different power, ground domains(Digital, Analog, reference clock) on the aspect of noise and noise floor.**
- **On Test load board design: There is an absence or lack of application of design, simulation tools to understand noise, noise propagation on Test Load board. Focus and resources are on existing accepted practice**

Dut Signal, Clock, Noise Floor Measurement Setup at the test site

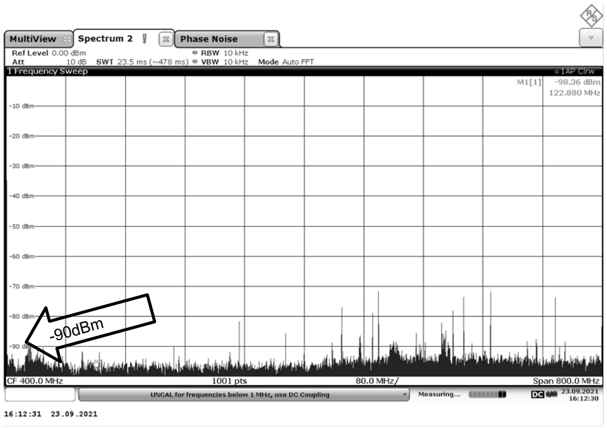


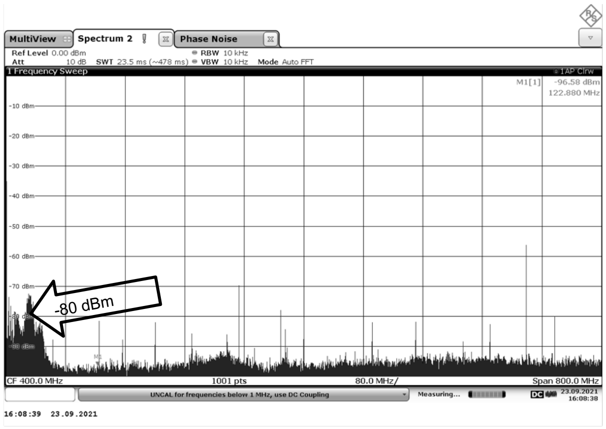
Measurements with Active Program, Patterns, Power Supplies

At the test site package balls

Noise, Noise Floor, Clock, ATE Signal, DUT Outputs

Analog Ground Noise Floor Measurement at the Test Site

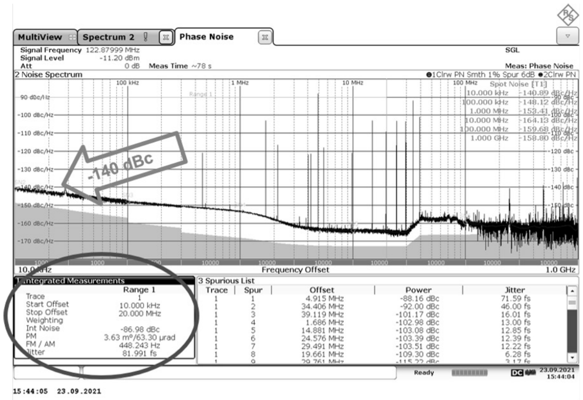




LS AGND Test program running , Pattern, Power Supplies **HS AGND**

ATE INSTRUMENT NOISE FLOOR

DUT clock and phase noise measurements 122.88Mhz



Signal Frequency 122.87999 MHz
Signal Level -11.20 dBm
Att 0 dB Meas Time ~78 s
SGL
Meas: Phase Noise

Spot Noise [T1]

10.000 kHz	-140.89 dBc/Hz
100.000 kHz	-148.12 dBc/Hz
1.000 MHz	-153.41 dBc/Hz
10.000 MHz	-164.13 dBc/Hz
100.000 MHz	-159.68 dBc/Hz
1.000 GHz	-158.80 dBc/Hz

1 Integrated Measurements

	Range 1
Trace	1
Start Offset	10.000 kHz
Stop Offset	20.000 MHz
Weighting	
Int Noise	-86.98 dBc
PM	3.63 m°/63.30 µrad
FM / AM	448.243 Hz
Jitter	81.991 fs

3 Spurious List

Trace	Spur	Offset	Power	Jitter
1	1	4.915 MHz	-88.16 dBc	71.59 fs
1	2	34.406 MHz	-92.00 dBc	46.00 fs
1	3	39.119 MHz	-101.17 dBc	16.01 fs
1	4	1.686 MHz	-102.98 dBc	13.00 fs
1	5	14.881 MHz	-103.08 dBc	12.85 fs
1	6	24.576 MHz	-103.39 dBc	12.39 fs
1	7	29.491 MHz	-103.51 dBc	12.22 fs
1	8	19.661 MHz	-109.30 dBc	6.28 fs
1	9	29.761 MHz	-115.22 dBc	3.17 fs

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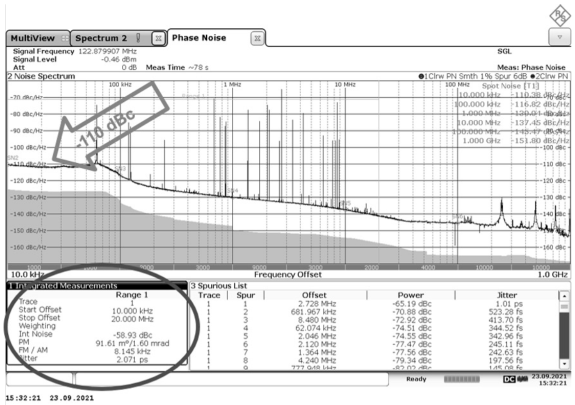
External PLL Low Jitter GENERATED CLOCK

1. 122.88 Mhz
2. Format Differential
3. **Phase Noise = 81.991 femto seconds**
4. Integration Range = 10 KHz to 20 MHz



Signal Frequency 122.879907 MHz
Signal Level -0.46 dBm
Att 0 dB Meas Time ~78 s
SGL
Meas: Phase Noise

Spot Noise [T1]

10.000 kHz	-110.38 dBc/Hz
100.000 kHz	-116.82 dBc/Hz
1.000 MHz	-130.01 dBc/Hz
10.000 MHz	-137.45 dBc/Hz
100.000 MHz	-145.47 dBc/Hz
1.000 GHz	-151.80 dBc/Hz

1 Integrated Measurements

	Range 1
Trace	1
Start Offset	10.000 kHz
Stop Offset	20.000 MHz
Weighting	
Int Noise	-58.93 dBc
PM	91.61 m°/1.60 mrad
FM / AM	8.145 kHz
Jitter	2.071 ps

3 Spurious List

Trace	Spur	Offset	Power	Jitter
1	1	2.728 MHz	-65.19 dBc	1.01 ps
1	2	681.967 kHz	-70.88 dBc	523.28 fs
1	3	8.480 MHz	-72.92 dBc	413.70 fs
1	4	62.074 kHz	-74.51 dBc	344.52 fs
1	5	2.046 MHz	-74.55 dBc	342.96 fs
1	6	2.120 MHz	-77.47 dBc	245.11 fs
1	7	1.364 MHz	-77.56 dBc	242.63 fs
1	8	4.240 MHz	-79.34 dBc	197.56 fs
1	9	777.948 kHz	-82.02 dBc	145.08 fs

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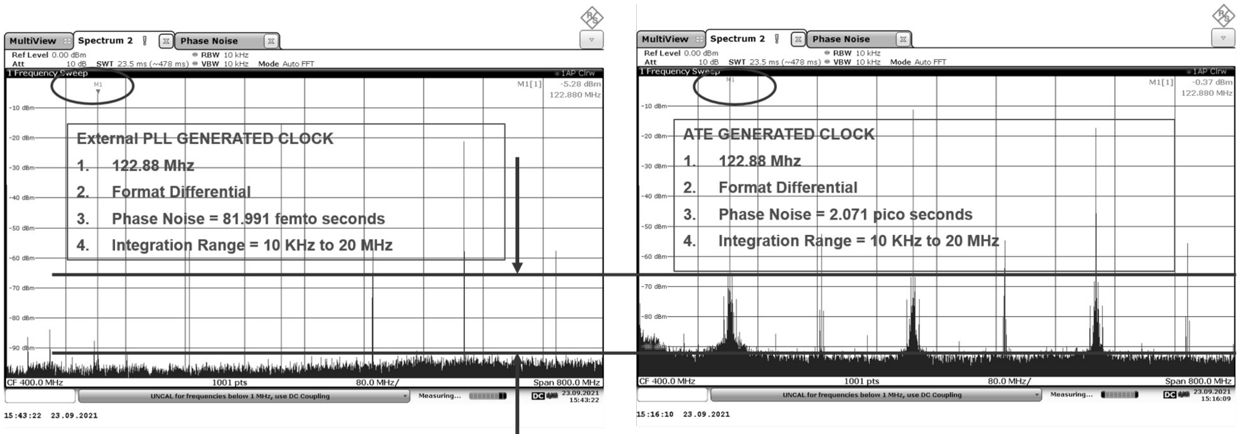
15:32:21 23.09.2021

ATE GENERATED CLOCK (Teradyne UP1600)

1. 122.88 Mhz
2. Format Differential
3. **Phase Noise = 2.071 pico seconds**
4. Integration Range = 10 KHz to 20 MHz

Clock spectrum, external PLL vs ate upc-1600 differential clock 122.88Mhz



External PLL GENERATED CLOCK

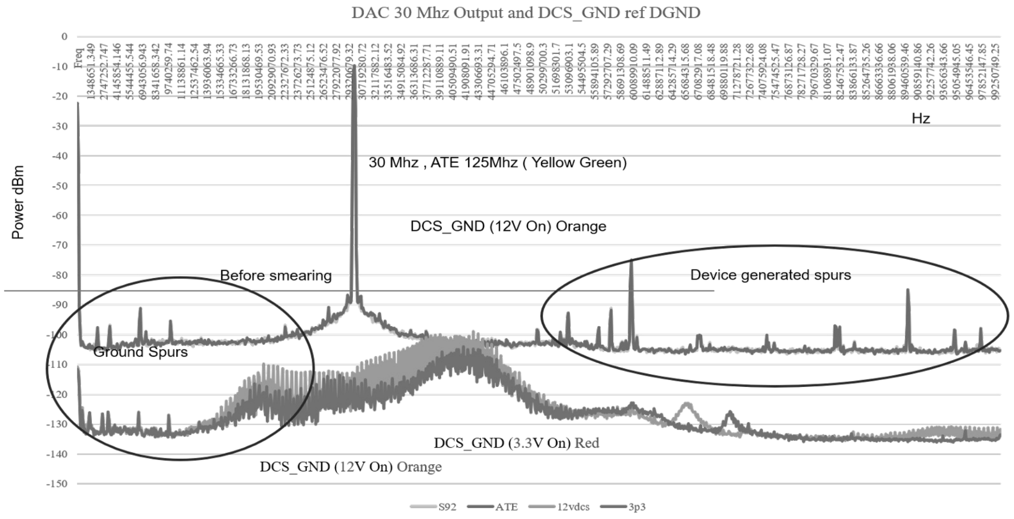
1. 122.88 Mhz
2. Format Differential
3. Phase Noise = 81.991 femto seconds
4. Integration Range = 10 KHz to 20 MHz

ATE GENERATED CLOCK

1. 122.88 Mhz
2. Format Differential
3. Phase Noise = 2.071 pico seconds
4. Integration Range = 10 KHz to 20 MHz

~ 20dBm

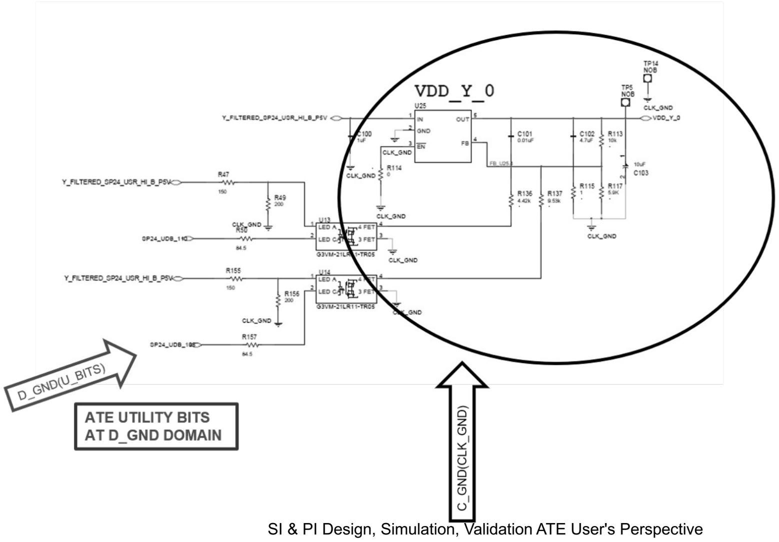
DAC Output 30 MHz, ATE 125Mhz, DCS_GND Noise, Utility supplies 12V on and 3.3V on



Power & Ground Domain management (CIRCUIT IMPLEMENTATION)

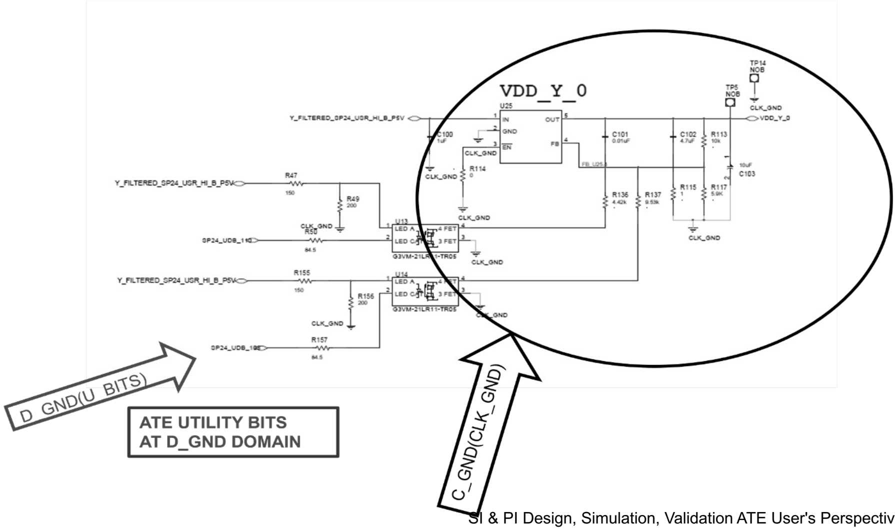
Power ground Isolation techniques

Opto-Isolators(U13, U14) to separate two (2) ground domains, digital DGND (ATE utility supply and unitality bits) and DUT CLK_GND



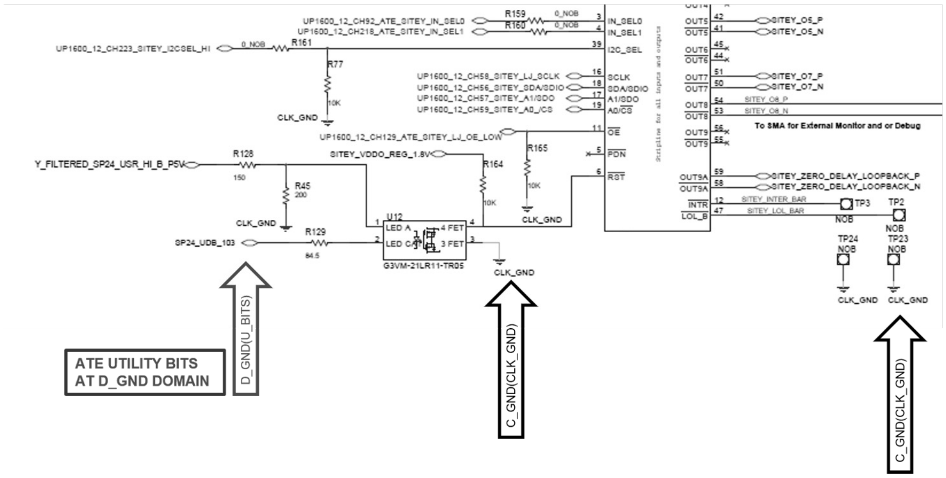
Power ground Isolation techniques

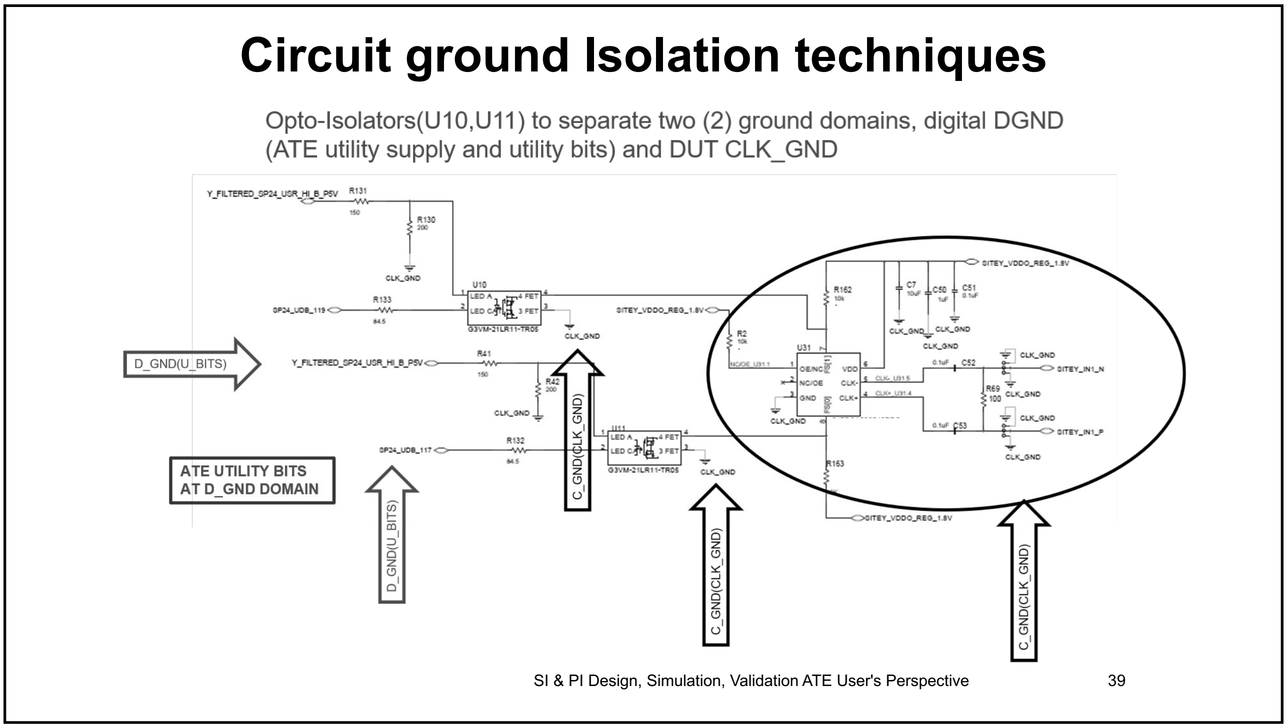
Opto-Isolators(U13, U14) to separate two (2) ground domains, digital DGND (ATE utility supply and utility bits) and DUT CLK_GND



Circuit ground Isolation techniques

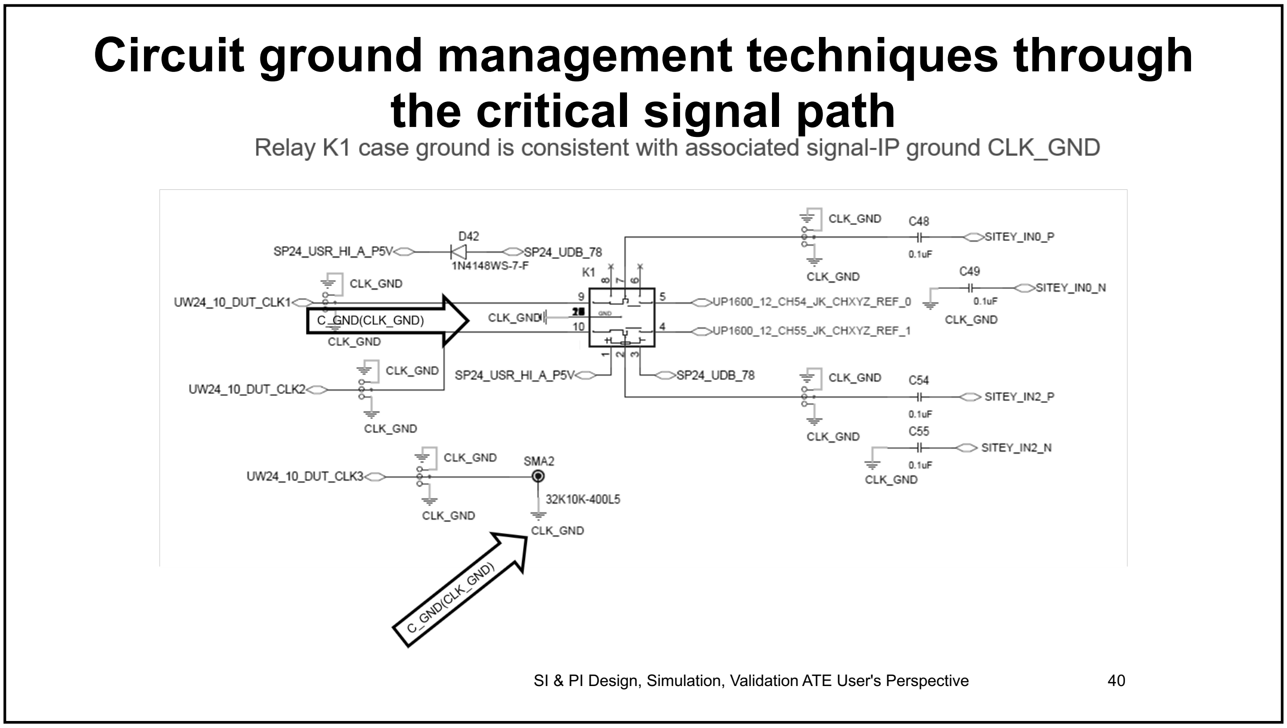
Opto-Isolators(U12) to separate two (2) ground domains, digital DGND (ATE utility supply and utility bits) and DUT CLK_GND





Circuit ground Isolation techniques

Opto-Isolators(U10,U11) to separate two (2) ground domains, digital DGND (ATE utility supply and utility bits) and DUT CLK_GND

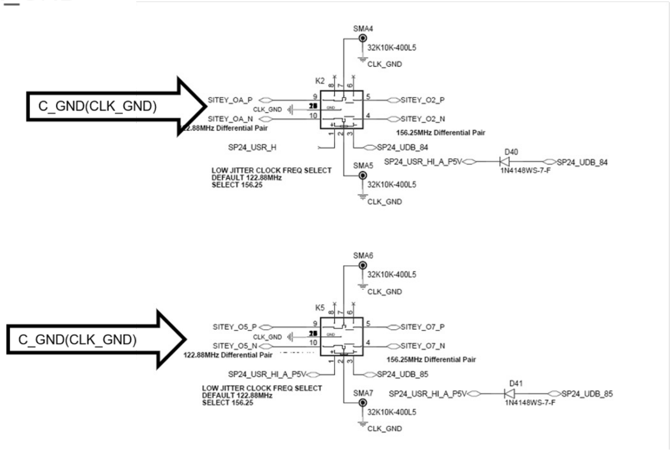


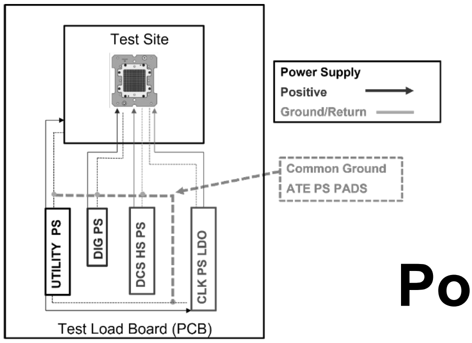
Circuit ground management techniques through the critical signal path

Relay K1 case ground is consistent with associated signal-IP ground CLK_GND

Circuit ground management techniques through the critical signal path

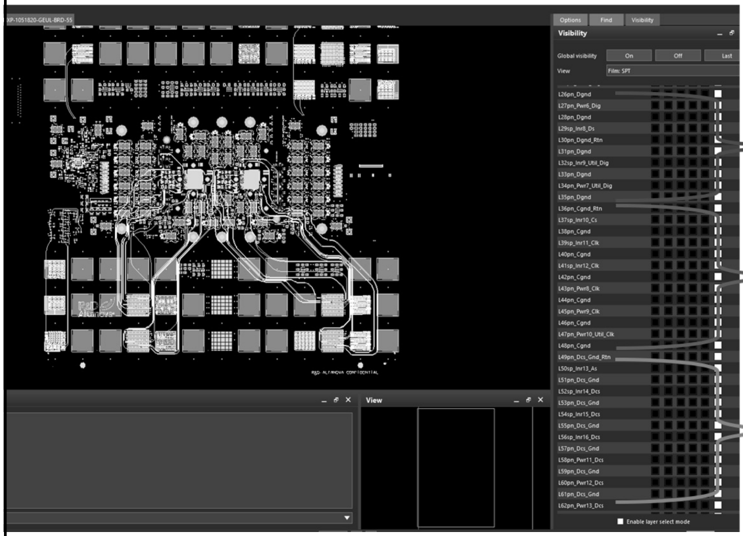
Relay K2, K5, SMAs 4,5,6,7 case ground consistent with associated signal-IP ground CLK_GND





Power & Ground Domain management (PCB , LAYOUT, LAYERS)

Ground & Layer Management and Isolation



Visibility

View: Film: SPT

L26pn_Dgnd
L27pn_Pwr6_Dig
L28pn_Dgnd
L29sp_Inr8_Ds
L30pn_Dgnd_Rtn
L31pn_Dgnd
L32sp_Inr9_Util_Dig
L33pn_Dgnd
L34pn_Pwr7_Util_Dig
L35pn_Dgnd
L36pn_Cgnd_Rtn
L37sp_Inr10_Cs
L38pn_Cgnd
L39sp_Inr11_Clk
L40pn_Cgnd
L41sp_Inr12_Clk
L42pn_Cgnd
L43pn_Pwr8_Clk
L44pn_Cgnd
L45pn_Pwr9_Clk
L46pn_Cgnd
L47pn_Pwr10_Util_Clk
L48pn_Cgnd
L49pn_Dcs_Gnd_Rtn
L50sp_Inr13_As
L51pn_Dcs_Gnd
L52sp_Inr14_Dcs
L53pn_Dcs_Gnd
L54sp_Inr15_Dcs
L55pn_Dcs_Gnd
L56sp_Inr16_Dcs
L57pn_Dcs_Gnd
L58pn_Pwr11_Dcs
L59pn_Dcs_Gnd
L60pn_Pwr12_Dcs
L61pn_Dcs_Gnd
L62pn_Pwr13_Dcs

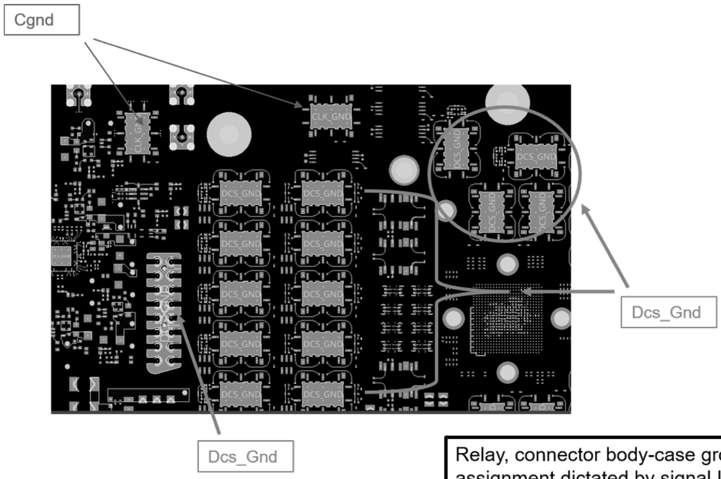
☐ Enable layer select mode

- Different power, ground domain as function of IP
- Consistency in ground domain implementation for power and signal delivery.

- No mixed-ground

1) Dgnd for Digital Core, and I/Os
2) DCS_GnD for ADC/DAC IPS, and I/Os
3) Cgnd for Low Jitter reference clock

Ground & Layer Management and Isolation



- Different power, ground domain as function of IP
- Consistency in ground-type domain routing, connection for power and signal delivery.

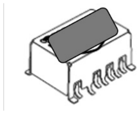
- No mixed-ground

1) Dgnd for Digital Core, and I/Os
2) DCS_GnD for ADC/DAC IPS, and I/Os
3) Cgnd for Low Jitter reference clock

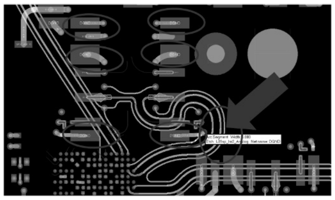
Relay, connector body-case ground assignment dictated by signal IPs (i.e. Dcs_Gnd)

Signal Relay (-20dB, -40dB isolation), Signal Shield & Relay Case Ground

GROUND SHIELD Relay Case, Signal Shield are wired to associated IP ground DCS_GND (Analog Ground)

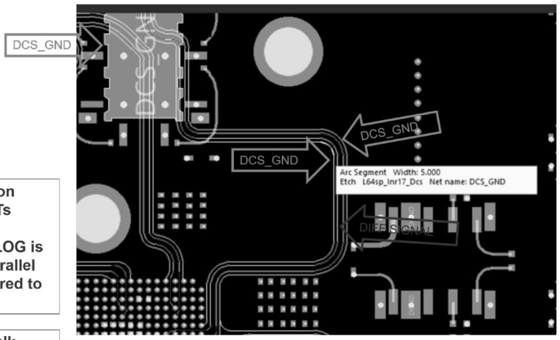


-20dB Isolation rated
- Crosstalk issues
- EMI issues

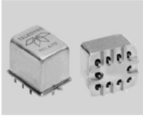


DGND connection on relay body and NETs where DGND and L09SP_INR2_ANALOG is connected. The parallel ground shield is wired to DGND.

- We have cross talk between relay poles
- Cross talk of digital IP noise(D_GND) getting into Analog I/O



Panasonic ARJ20A4H DPDT



Teledyne GRF180 DPDT

Power and Ground Management

Summary

1. **Key strategy for Power and Ground Management**
    1. **Power Return path is forced by design to the immediate (top/bottom layer ground)**
    2. **Signal Return path is forced by design to the immediate (top/bottom layer ground)**
    3. **There is no Power or Signal with different type of ground (top/bottom).**
        1. **Digital Block layer DGND top and bottom layer**
        2. **CLK Support layer CGND top and bottom layer**
        3. **DAC/ADC Analog block LS_DCS_GND, HS_DC_GND (top/bottom)**
    4. **Careful, focus layout planning maximized the use of board layers that are IP specific**
2. **Ground Isolation eliminated key issues for device testing**
    1. **Improve the noise floor to improve SINAD, SNR test parameters for ADC and DAC**
    2. **Eliminate Digital IP Noise from getting into the Analog I/O for single site testing and multi-site testing**
3. **Consistency on ground routing to associated IP is key. No mixing of ground along the signal path especially external connectors, relays and cable assemblies**

External hardware passive and active

External Low Jitter Clock generator profile 122.88 GHz

Signal Frequency 122.881337 MHz
Signal Level -1.25 dBm
Att 0 dB
RBW 0.1 %
XCORR Factor 1000
Meas Time ~62 s
SGL
Meas: Phase Noise

Spot Noise [T1]

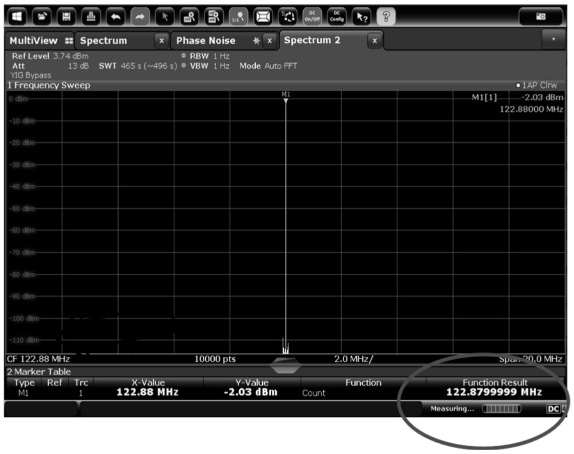
10.000 kHz	-140.93 dBc/Hz
100.000 kHz	-148.04 dBc/Hz
1.000 MHz	-153.31 dBc/Hz
10.000 MHz	-164.32 dBc/Hz
100.000 MHz	-166.10 dBc/Hz

2 Integrated Measurements

	Range 1
Trace	1
Start Offset	10.000 kHz
Stop Offset	20.000 MHz
Weighting	
Int Noise	-87.01 dBc
PM	3.62 m°/63.10 µrad
FM / AM	429.908 Hz
Jitter	81.733 fs

4 Spurious List

Trace	Spur	Offset	Power	Jitter
1	6	9.420 MHz	-123.92 dBc	1.17 fs
1	7	9.830 MHz	-123.40 dBc	1.24 fs
1	8	14.880 MHz	-103.54 dBc	12.19 fs
1	9	18.720 MHz	-119.68 dBc	1.90 fs
1	10	24.240 MHz	-105.89 dBc	9.30 fs
1	11	27.046 MHz	-120.45 dBc	1.74 fs
1	12	29.760 MHz	-112.95 dBc	4.12 fs
1	13	33.370 MHz	-101.49 dBc	15.43 fs
1	14	39.120 MHz	-112.73 dBc	4.23 fs
1		Total	Discrete Jitter	23.31 fs
1			Random Jitter	126.61 fs
2	1	2.250 MHz	-122.61 dBc	1.36 fs
2	2	3.840 MHz	-117.89 dBc	2.34 fs
2	3	4.915 MHz	-122.93 dBc	1.31 fs
2	4	5.520 MHz	-116.80 dBc	2.65 fs

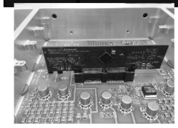


Ref Level 3.74 dBm
Att 13 dB SWT 465 s (~496 s)
RBW 1 Hz
VBW 1 Hz
Mode Auto FFT
YIG Bypass

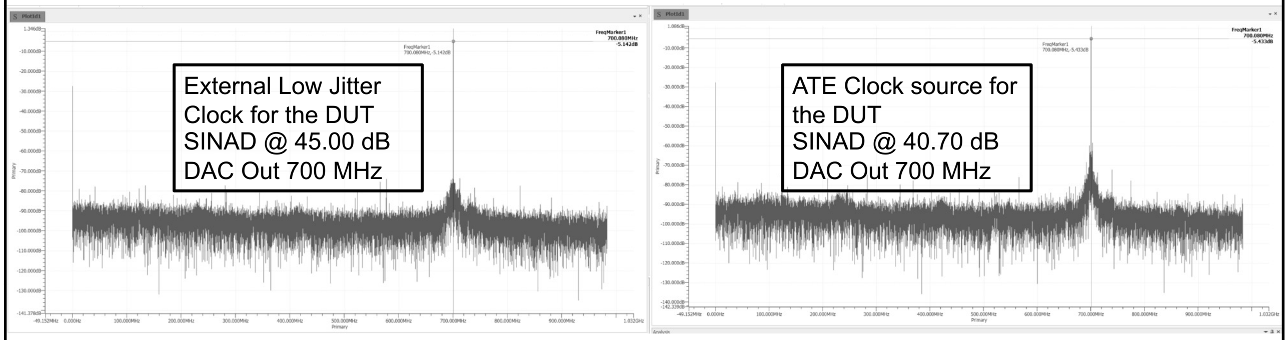
M1[1] -2.03 dBm
122.88000 MHz

2 Marker Table

Type	Ref	Trc	X-Value	Y-Value	Function	Function Result
M1		1	122.88 MHz	-2.03 dBm	Count	122.8799999 MHz



SINAD External Clock vs ATE Clock

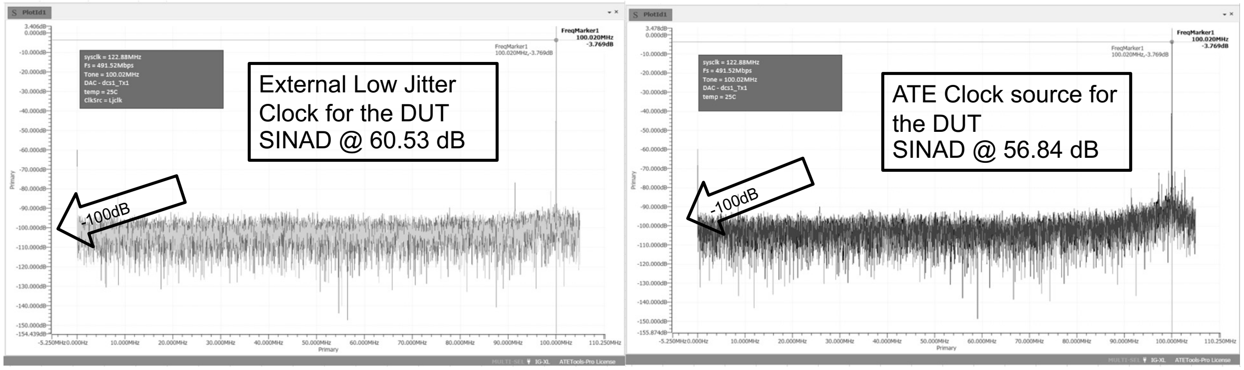


External Low Jitter Clock for the DUT
SINAD @ 45.00 dB
DAC Out 700 MHz

ATE Clock source for the DUT
SINAD @ 40.70 dB
DAC Out 700 MHz

Measurements by Kenneth Hoffman NXP EP

SINAD External Clock vs ATE Clock



sysclk = 122.88MHz
Fs = 491.52Mbps
Tone = 100.02MHz
DAC - dcs1_Tx1
temp = 25C
ClkSrc = Ljclk

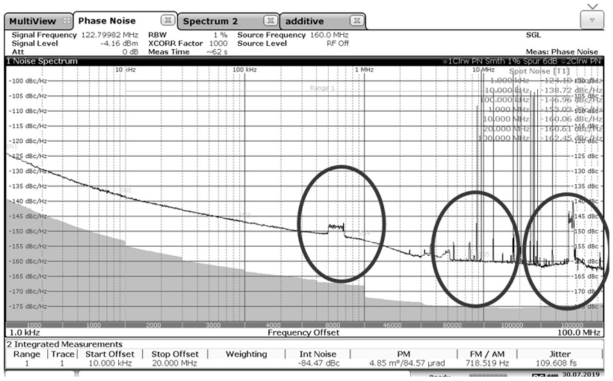
External Low Jitter Clock for the DUT
SINAD @ 60.53 dB

sysclk = 122.88MHz
Fs = 491.52Mbps
Tone = 100.02MHz
DAC - dcs1_Tx1
temp = 25C

ATE Clock source for the DUT
SINAD @ 56.84 dB

Measurements by Loc Vu NXP EP

External Hardware Passive and Active



Signal Frequency 122.79982 MHz
Signal Level -4.16 dBm
Att 0 dB
RBW 1 %
XCORR Factor 1000
Meas Time ~62 s
Source Frequency 160.0 MHz
Source Level RF Off
SGL
Meas: Phase Noise

1.000 kHz	-124.10 dBc/Hz
10.000 kHz	-138.72 dBc/Hz
100.000 kHz	-146.96 dBc/Hz
1.000 MHz	-153.03 dBc/Hz
10.000 MHz	-160.06 dBc/Hz
20.000 MHz	-160.61 dBc/Hz
100.000 MHz	-162.45 dBc/Hz

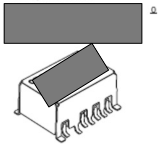
2 Integrated Measurements

Range	Trace	Start Offset	Stop Offset	Weighting	Int Noise	PM	FM / AM	Jitter
1	1	10.000 kHz	20.000 MHz		-84.47 dBc	4.85 m°/84.57 µrad	718.519 Hz	109.608 fs

Relay with -20dB Isolation rating

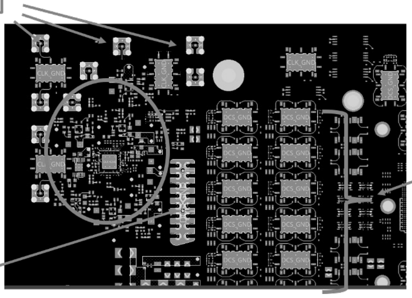
- Crosstalk between poles
- Magnetic field on the signal from the relay coil

Compatible with 3 GHz



Failed victim-aggressor test at the lab

Support Circuits, High Isolation (-40dB), Relays, and Connector Assembly



SMA

- External Low Jitter Clock Generator Circuit- Low Phase Noise
- LDO Regulators to power support circuits
- Opto Isolator to separate ground domains (i.e. D_GND and CLK_GND)

Cable Assy

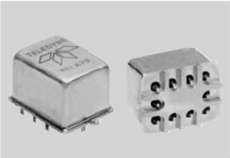
High Isolation (-40dBm) devices

- High Isolation Relays
- Cable Sets (H&S)
- SMA Connectors

Relays

Relays pass victim-aggressor test at the lab

Panasonic
ARJ20A4H DPDT



Teledyne
GRF180 DPDT

Teledyne
GRF121R SPDT

External hardware passive and active

Summary

1. External clock generator addressed the DUT requirements for ultra low phase noise , jitter differential clock (~ < 100 femto-seconds, at integration range 10Khz to 20Mhz0) for frequencies 122.88MHz, 125.00MHz, and 156.25MHz. Existing ATE RF clock source is limited to 100MHz and single frequency at a time
2. External LDO(Linear Low Drop Out) regulators are used to power external support circuits
3. High isolation relays (-40 to -50dB) RF relays to prevent
    1. Cross talk between poles on relays
    2. Electromagnetic interference from relay coil
4. High Isolation Cable Assembly & SMA connector eliminated cross talk between cables
5. Opto-Isolator MOSFETS are used to separate Digital and Analog Domain circuits. That is for both DUT Signal, and Power Regulator Controls (control for the LDO)

Moving Forward

We need to develop the analytical capability to predict NOISE FLOOR

1. Base on measured performance of ATE Instruments (ATE Channel, DUT Power Supply, RF Source/Measurement, Utility Supply)
2. Create, Use models to assess noise generators from ATE instruments and external sources
3. Manage noise
    1. Eliminate or isolate if possible
    2. Move or shift to different frequency range beyond the DUT operation of interest

Noise Floor on ATE Hardware Summary

1. **NOISE FLOOR requirements for individual IPs on the SOC block is critical in LOADBOARD Design.**
2. **Complicated problems like miscorrelation, crosstalk, can be avoided by detailed understanding of noise-floor and ground-management intricacies.**
3. **External support circuits are cost effective solutions to augment existing limitations of ATE. That is with a very focus application and understanding of intricacies to integrate with device test program on ATE environment.**
4. **Application of modeling, simulation, and validation tools is an area for improvement to better understand noise, and noise floor on ADC/DAC Testing.**

Acknowledgements

Ira Feldman & TestConX 2026 Organization

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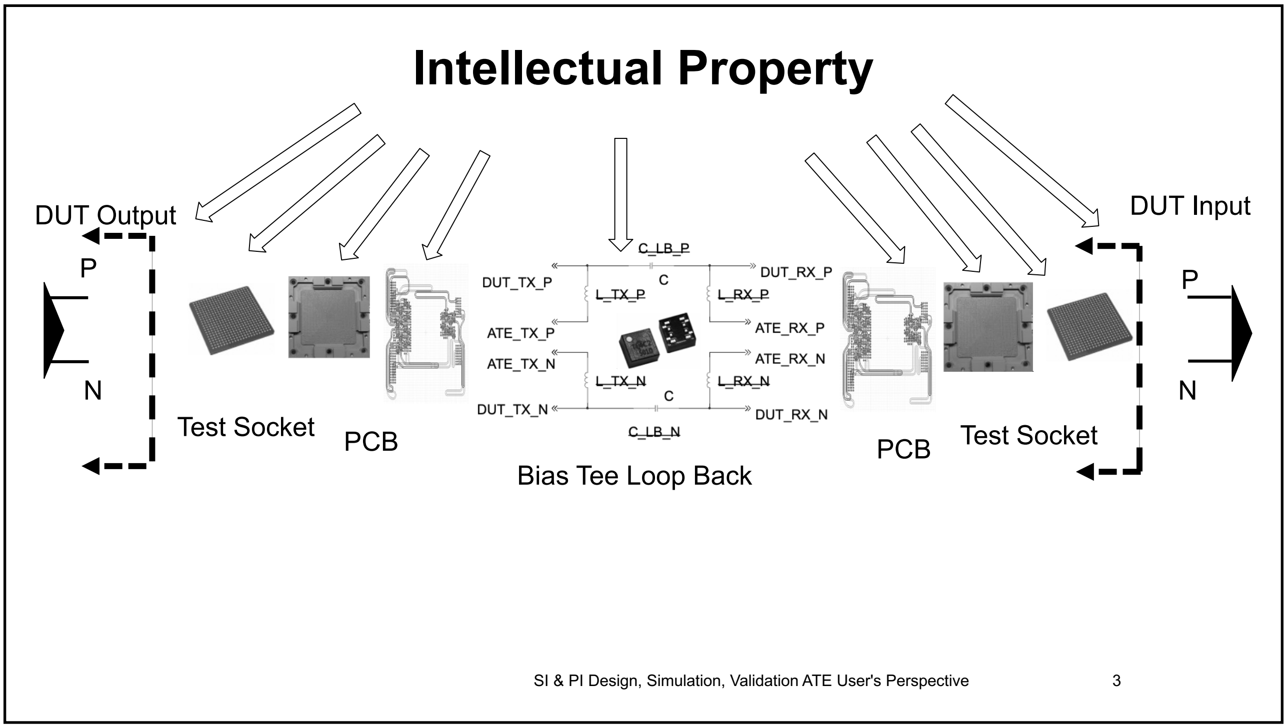
Management and Technical Team Advantest Interface Services
Kevin Kim, TSE
Anritsu USA Application Support
Jason Mroczkowski, Cohu
Cadence Apps Support
Leeno

IP SECURITY AND AI IMPLEMENTATION OPPORTUNITIES

Intellectual Property

Must be PROTECTED, RESPECTED
all the time



Intellectual Property

DUT Output

P

N

Test Socket

PCB

DUT_TX_P

ATE_TX_P

ATE_TX_N

DUT_TX_N

C_LB_P

C

L_TX_P

L_TX_N

C

C_LB_N

L_RX_P

L_RX_N

DUT_RX_P

ATE_RX_P

ATE_RX_N

DUT_RX_N

Bias Tee Loop Back

PCB

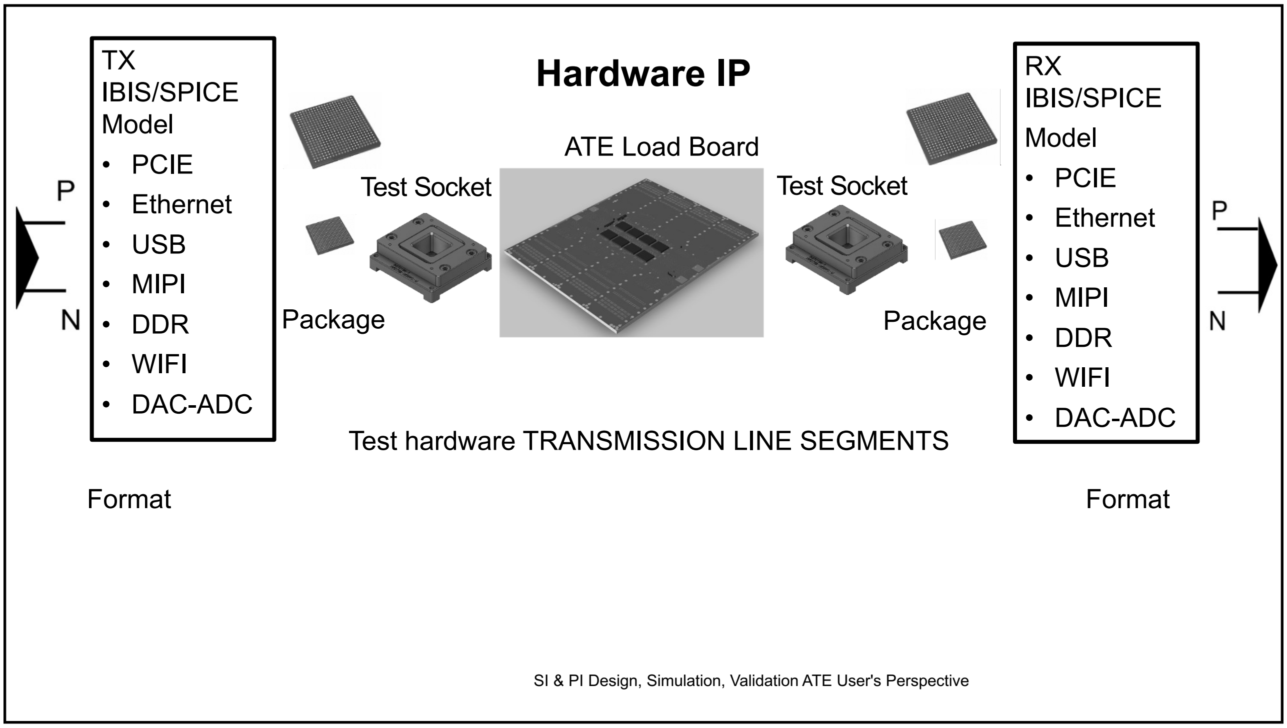
Test Socket

DUT Input

P

N

SI & PI Design, Simulation, Validation ATE User's Perspective 3



Hardware IP

TX IBIS/SPICE Model
- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

P

N

Package

Test Socket

ATE Load Board

Test Socket

Package

RX IBIS/SPICE Model
- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

P

N

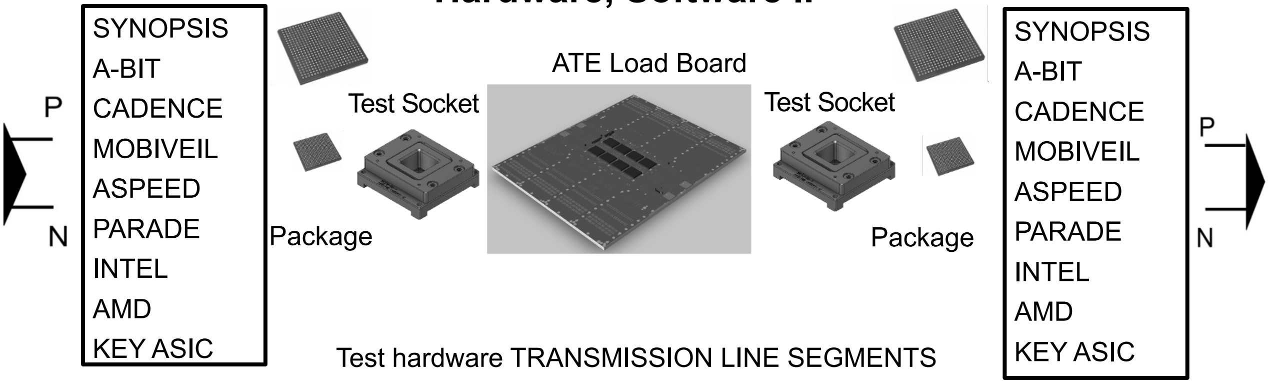
Test hardware TRANSMISSION LINE SEGMENTS

Format

Format

SI & PI Design, Simulation, Validation ATE User's Perspective

Hardware, Software IP



SYNOPSIS
A-BIT
CADENCE
MOBIVEIL
ASPEED
PARADE
INTEL
AMD
KEY ASIC

Test hardware TRANSMISSION LINE SEGMENTS

SYNOPSIS
A-BIT
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ASPEED
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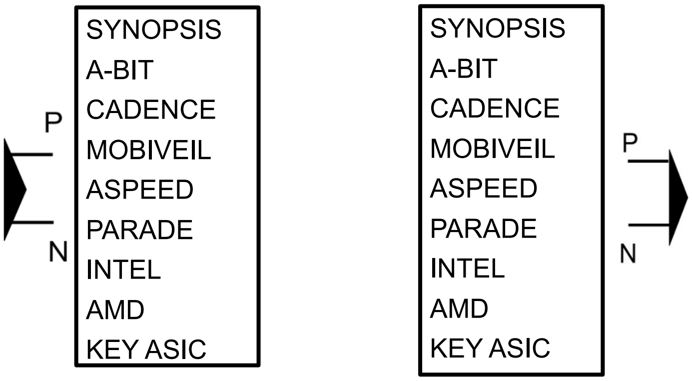
AMD
KEY ASIC

IP Technology

Format

I/O Technology and IP Providers

Business Unit (BU) have the option to use different IP solution providers from technology market



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I/O Technology and IP Providers

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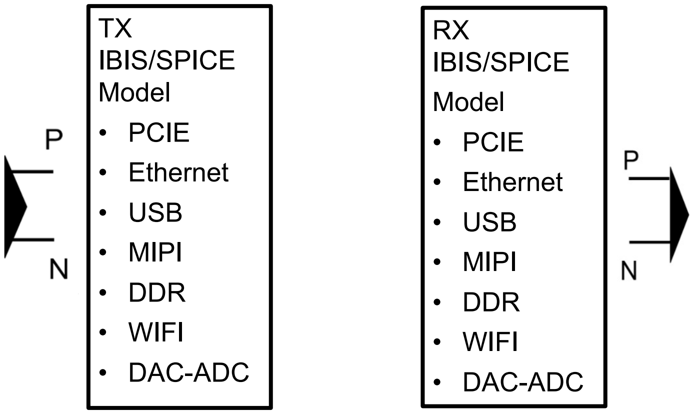


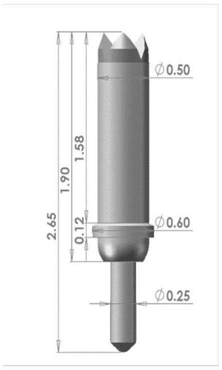
TX
IBIS/SPICE
Model

- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

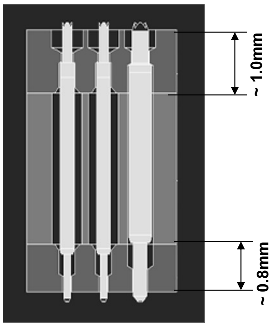
RX
IBIS/SPICE
Model

- PCIE
- Ethernet
- USB
- MIPI
- DDR
- WIFI
- DAC-ADC

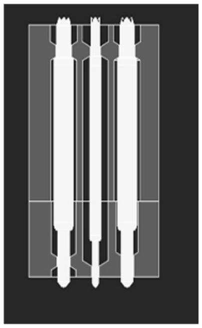
Test Socket Technology and IP



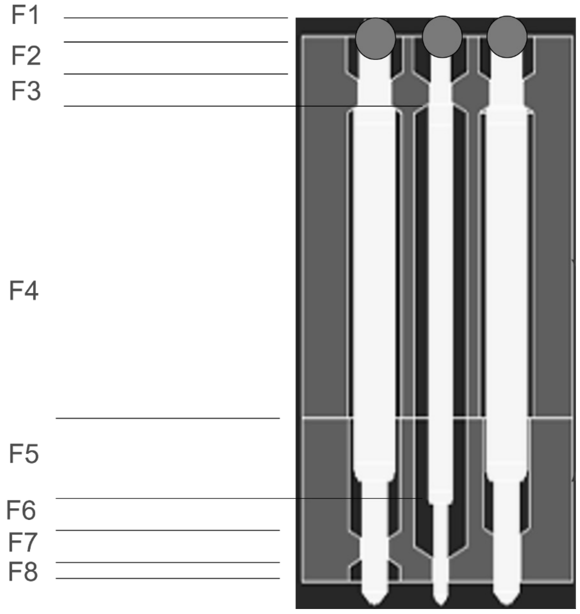
Conventional Coaxial
Limited Coax Structure



Coaxial
Optimized Coax Structure



True 3D Physical Model are the crown jewels of the industry

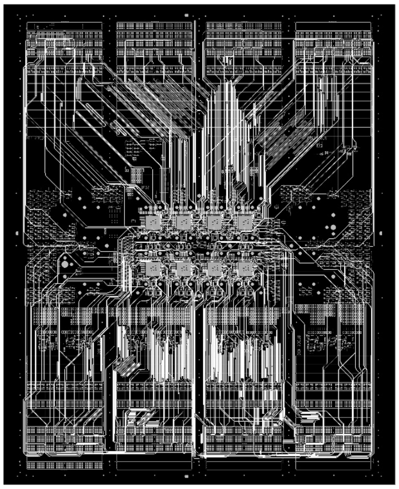


Filter Segments

- Each Segments needs to be accounted.
- Short wavelength with increasing data rate makes every segment significant.
- The interface with package ball needs to be modeled, simulated, validated.
- The interface with the board needs to be modeled, simulated, validated.

Speed of Light (air)		299702547	m/s		
Frequency					
Band Width (GHz)	Wavelength (m)	(mm)	(ft)	(in)	Period (ps)
1	0.2997	299.703	0.983	11.799	1000.000
2	0.1499	149.851	0.492	5.900	500.000
3	0.0999	99.901	0.328	3.933	333.333
4	0.0749	74.926	0.246	2.950	250.000
5	0.0599	59.941	0.197	2.360	200.000
9	0.0333	33.300	0.109	1.311	111.111
10	0.0300	29.970	0.098	1.180	100.000
15	0.0200	19.980	0.066	0.787	66.667
20	0.0150	14.985	0.049	0.590	50.000
30	0.0100	9.990	0.033	0.393	33.333
40	0.0075	7.493	0.025	0.295	25.000
50	0.0060	5.994	0.020	0.236	20.000
60	0.0050	4.995	0.016	0.197	16.667
70	0.0043	4.281	0.014	0.169	14.286

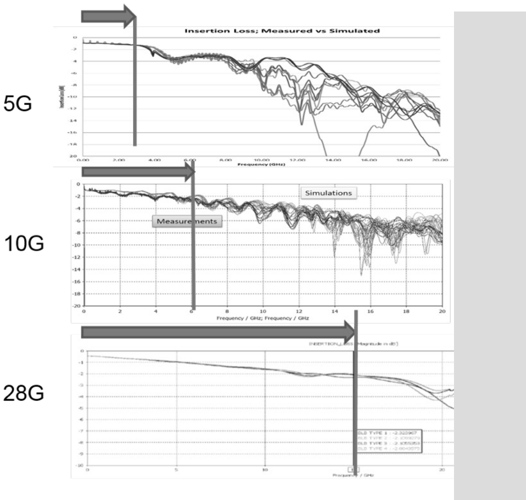
PCB BRD Design Files IP



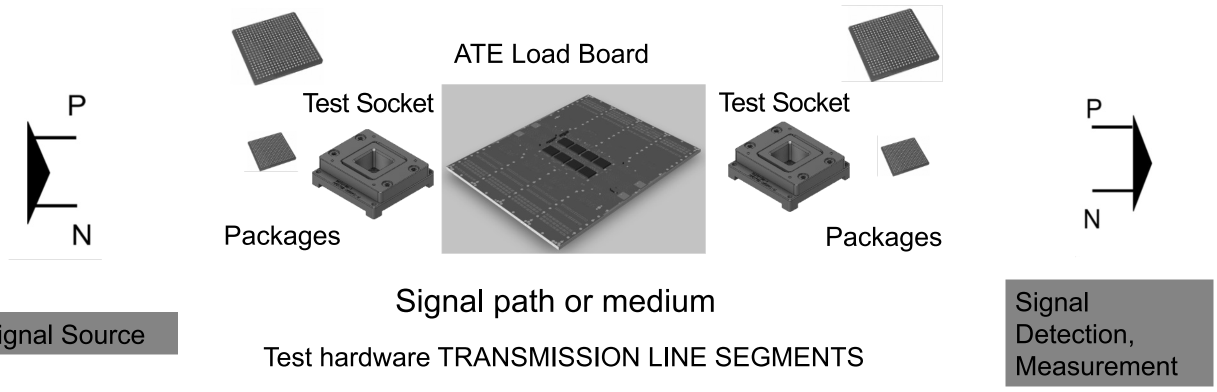
BRD Design Files
- Exclusive to user only
- Not shared to competing PCB Design House
- Not shared to Socket or Interposer HW provider

BRD Design Files
- Buried Optimization Techniques
- Special PCB Structures (VIA, PADS…)
- PCB FAB Process Information

PCB BRD Design Files IP (VIA Technology)



Hardware Signal Path Design Integration



ATE Load Board

Test Socket

Test Socket

P

N

P

N

Packages

Packages

Signal path or medium

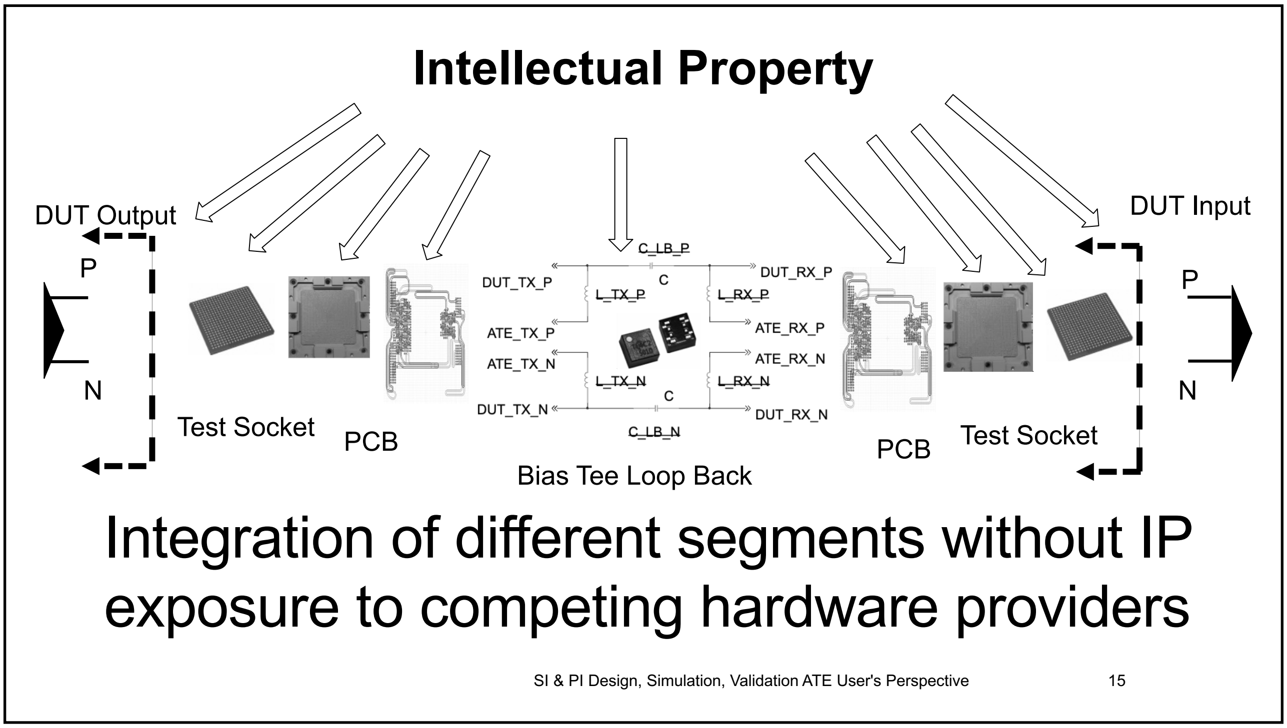
Test hardware TRANSMISSION LINE SEGMENTS

Signal Source

Signal Detection, Measurement

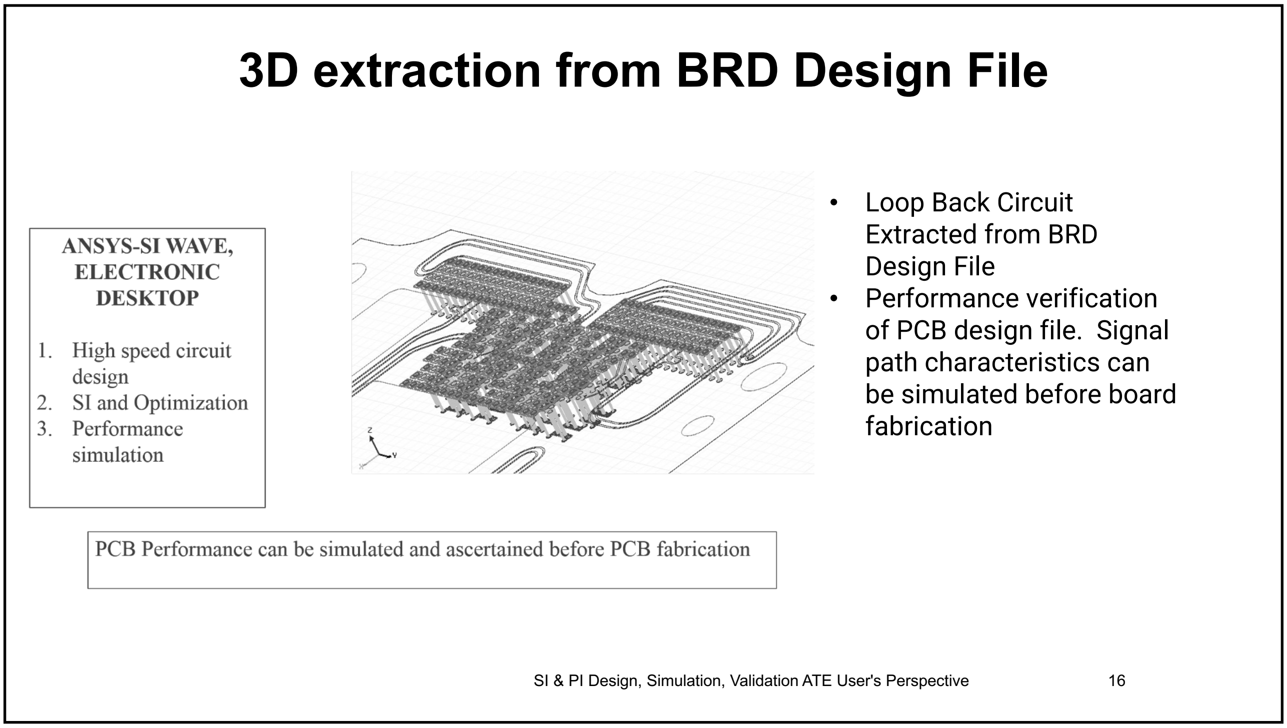
IP Security Challenges

- I/O Drivers and Receivers are controlled IP
    - Format PCIE, USB, SATA, Ethernet
    - I/O Standard Gen1, Gen2, Gen3
    - USE-Case, Business Unit specific configuration
- I/O Drivers and Receivers settings are controlled information
- IP Sharing is tricky at best to provide best approximation
    - Socket Models
    - BRD model files are treasure throve of
        - PCB Structure design
        - Circuit Optimization technique
        - Fab process technology



Intellectual Property

Integration of different segments without IP exposure to competing hardware providers



3D extraction from BRD Design File

ANSYS-SI WAVE, ELECTRONIC DESKTOP

1. High speed circuit design
2. SI and Optimization
3. Performance simulation

- Loop Back Circuit Extracted from BRD Design File
- Performance verification of PCB design file. Signal path characteristics can be simulated before board fabrication

PCB Performance can be simulated and ascertained before PCB fabrication

Socket Design & Integration :Empirical Process

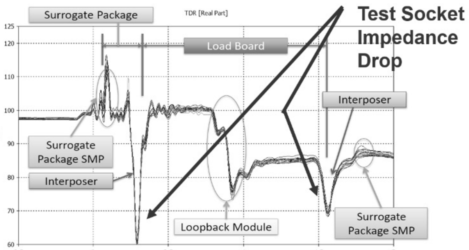
Because of IP Sensitivity Socket Integration is more of an empirical process. Success attained through observation than accuracy of models to real world and when integrated.

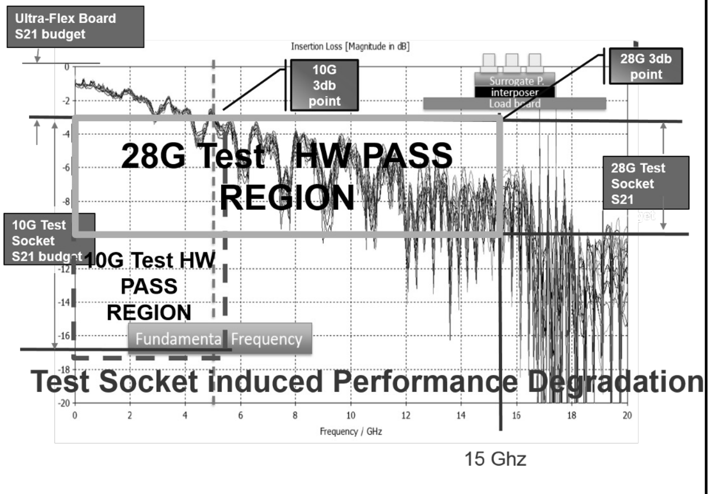
Integration with the package ball and pcb is a very tricky process.

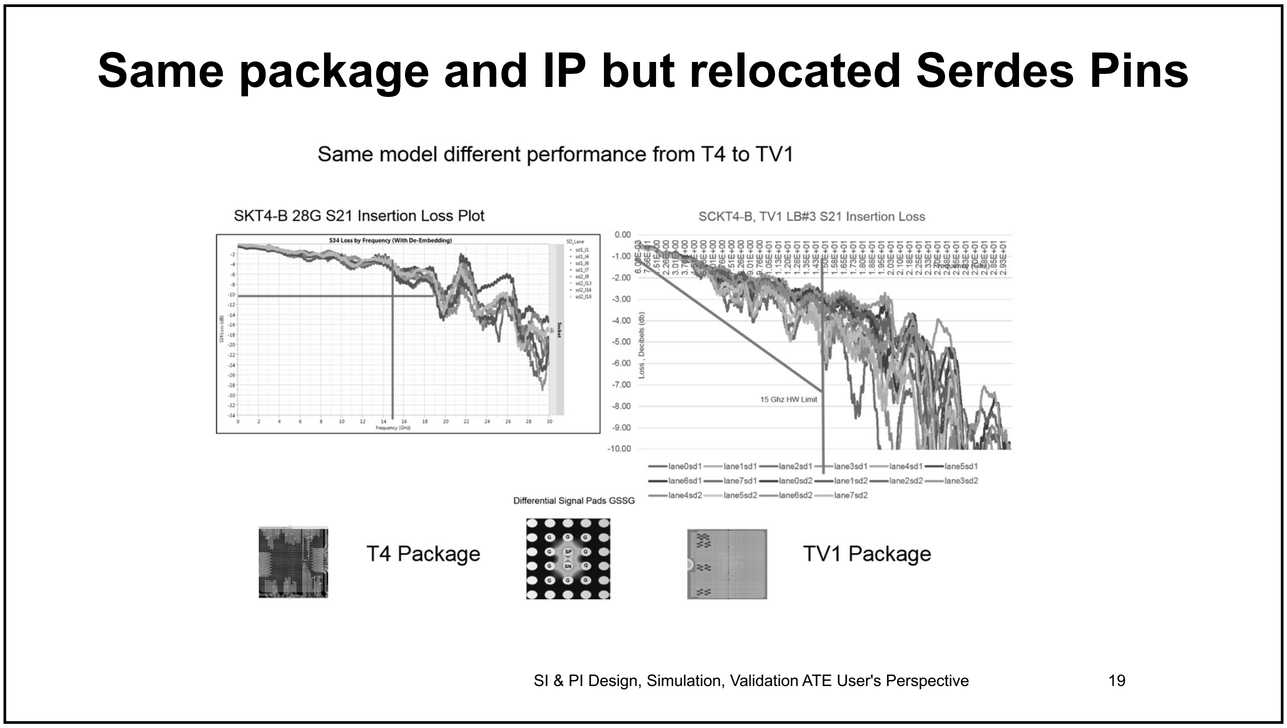
Success or compliance is attained **through commitment, multiple iterations of the socket**. Three to four iteration a common scenario.

Typical success rate is 10% to 20%. Two of 12 socket samples were compliant on the first try.

Painful Steps , Growing pains





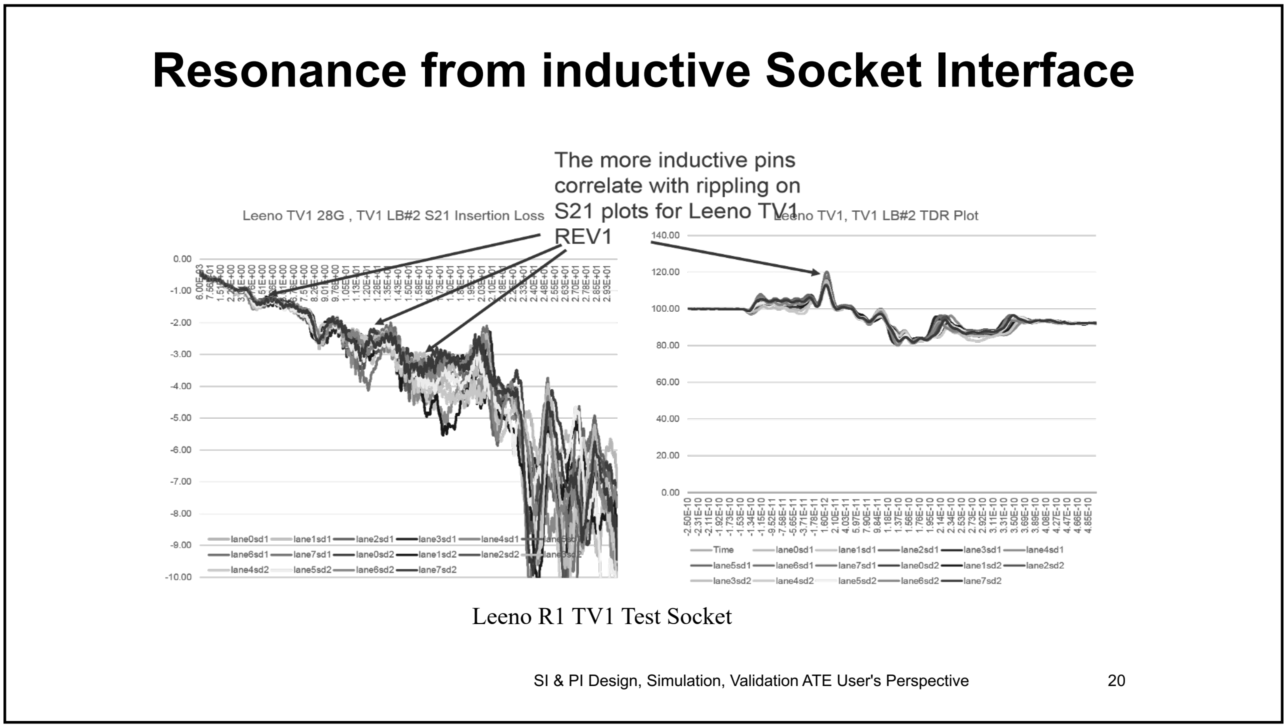


Same package and IP but relocated Serdes Pins

Same model different performance from T4 to TV1

T4 Package

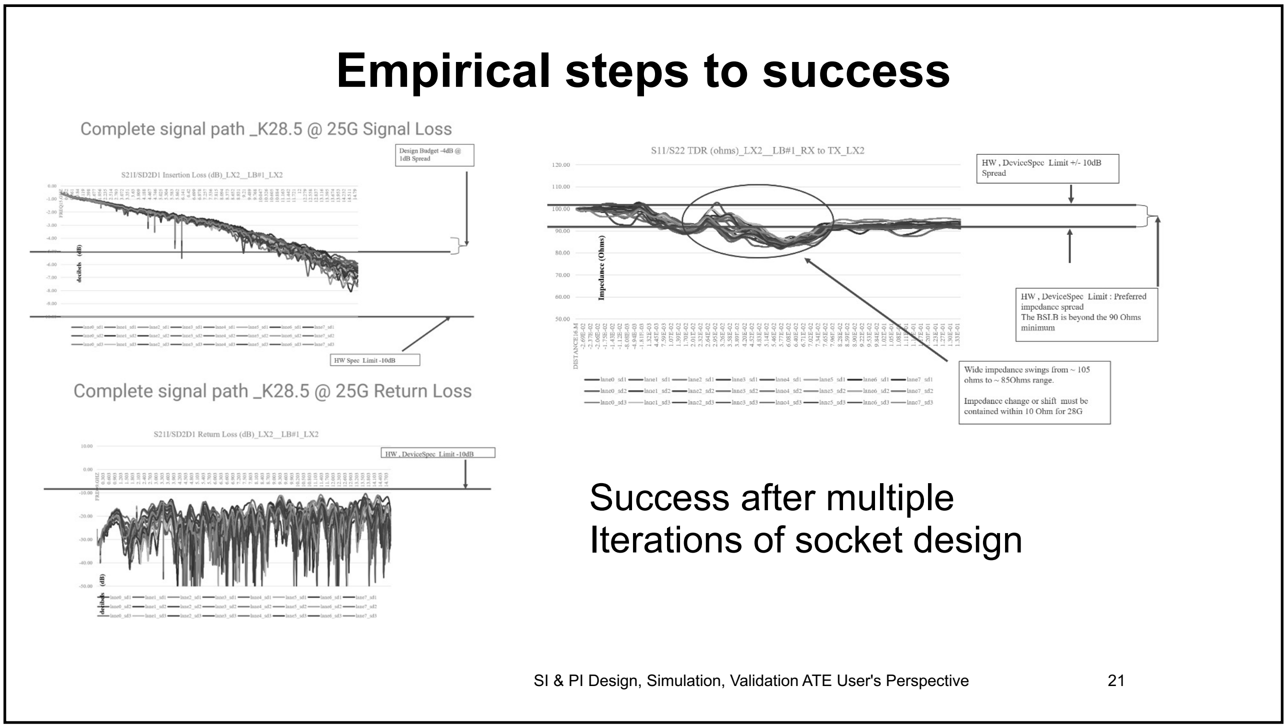
TV1 Package



Resonance from inductive Socket Interface

The more inductive pins correlate with rippling on S21 plots for Leeno TV1 REV1

Leeno R1 TV1 Test Socket

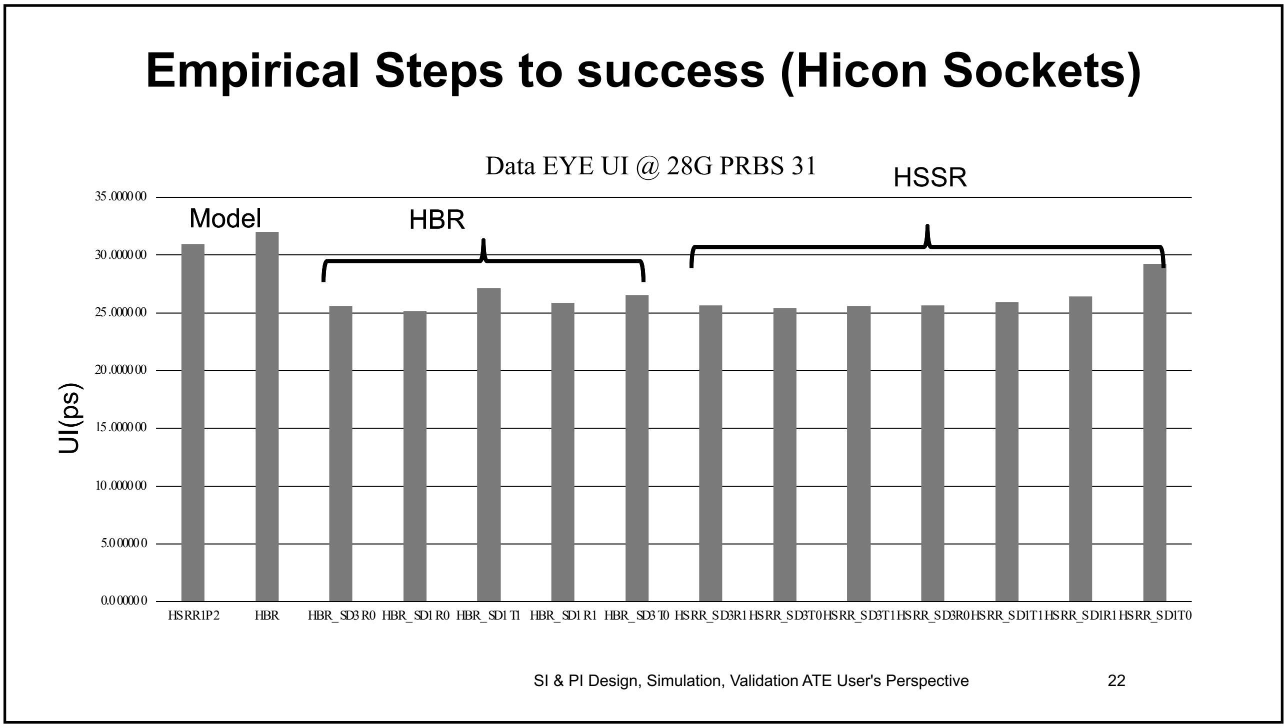


Empirical steps to success

Complete signal path _K28.5 @ 25G Signal Loss

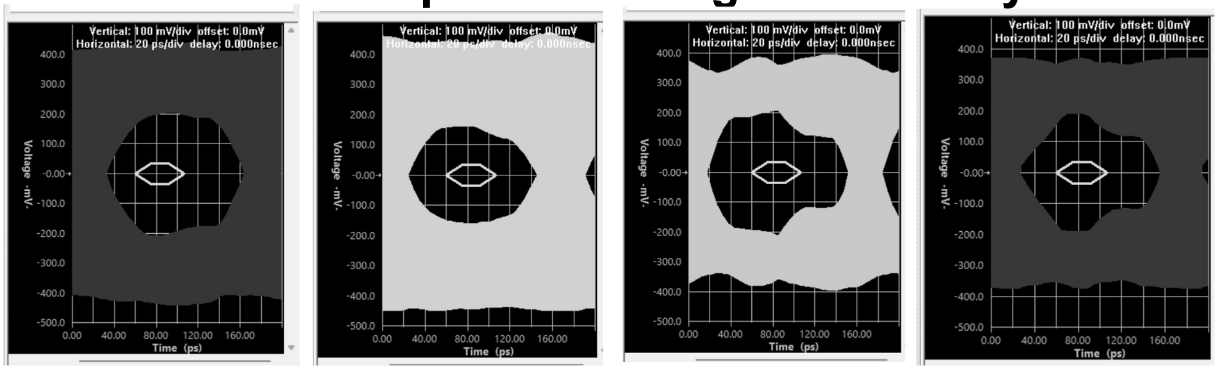
Complete signal path _K28.5 @ 25G Return Loss

Success after multiple
Iterations of socket design



Empirical Steps to success (Hicon Sockets)

Inductive Spike Modeling and Data Eye



90 Ohms Socket

90 Ohms Socket
W/ 120 ohms Spike

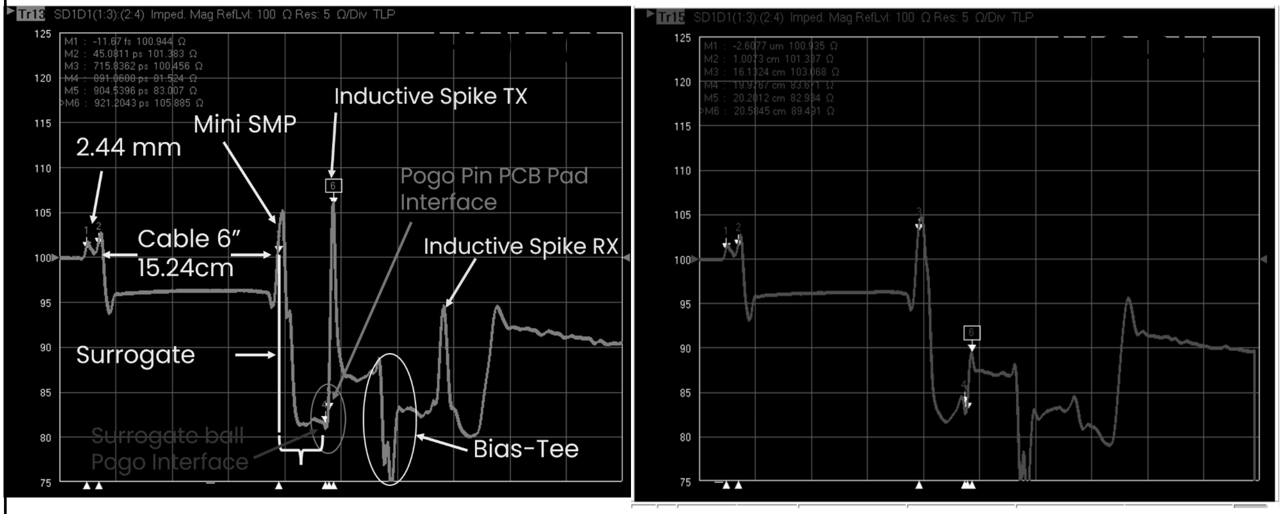
95 Ohms Socket

95 Ohms Socket
W/ 120 ohms
Spike

Data Eye deformation, degradation

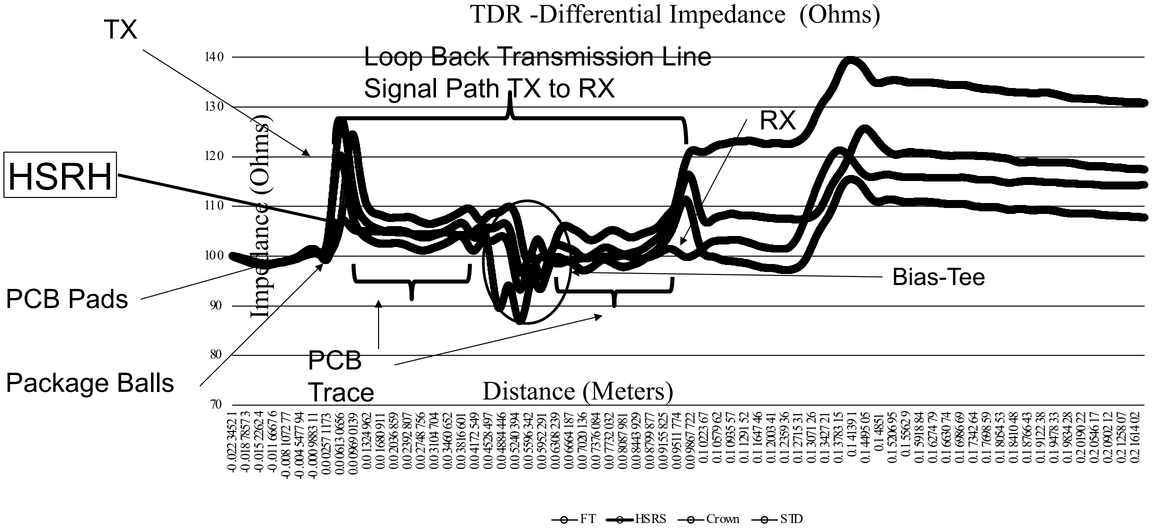
1. From 90 Ohms differential impedance to 95 ohms
2. From 120+ ohms inductive spike @ pogo-pin board pad interface

Board TDR profile Pogo pin vs HSRH

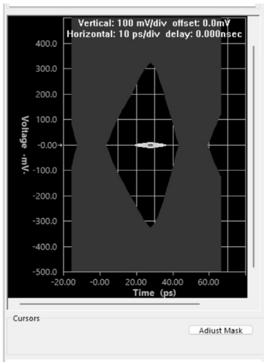

```
Tr13 SD1D1(1:3):(2:4) Imped. Mag RefLvl: 100 Ω Res: 5 Ω/Div TLP
M1 : -11.67 fs 100.944 Ω
M2 : 45.0811 ps 101.383 Ω
M3 : 715.8362 ps 100.456 Ω
M4 : 891.0600 ps 81.524 Ω
M5 : 904.5396 ps 83.007 Ω
>M6 : 921.2043 ps 105.885 Ω
```

```
Tr15 SD1D1(1:3):(2:4) Imped. Mag RefLvl: 100 Ω Res: 5 Ω/Div TLP
M1 : -2.6077 um 100.935 Ω
M2 : 1.0073 cm 101.387 Ω
M3 : 16.1324 cm 103.068 Ω
M4 : 19.9767 cm 83.671 Ω
M5 : 20.2012 cm 82.984 Ω
>M6 : 20.5845 cm 89.491 Ω
```

HSRH-TDR Profile with Reduced Inductive Spike (Measured Data)



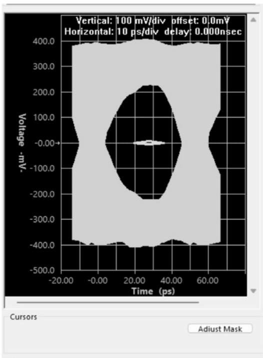
PRBS-31 18G Equal=5, DFE=5, CTLE=Disabled, HSRH (Prototype-Board, 1 inch trace, 3.5 mil wide trace Bias-tee)



HICON-HSRH
PRBS-31

Comments:

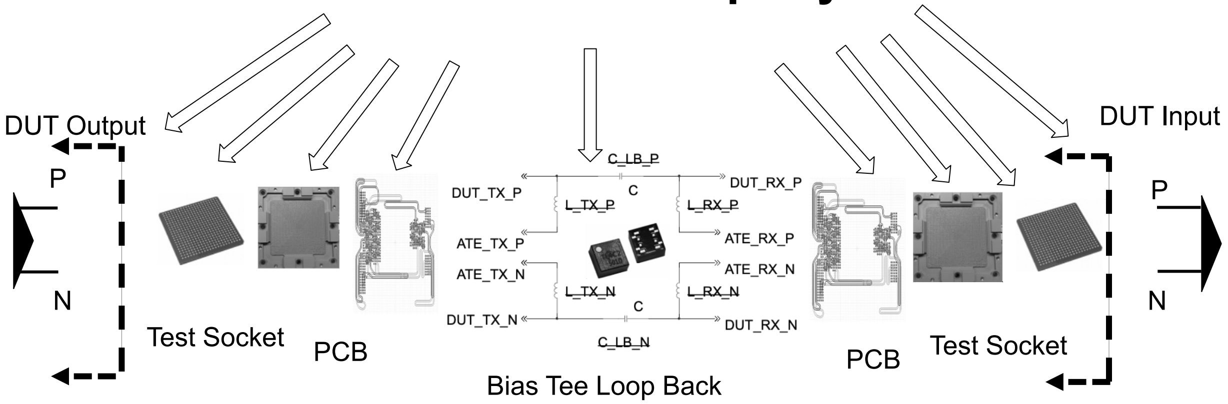
- **HSRH Test Socket has the best data eye for the project**
- **Soldered devices show the impact on Rise/Fall time of the test socket**



Soldered Device
PRBS-31

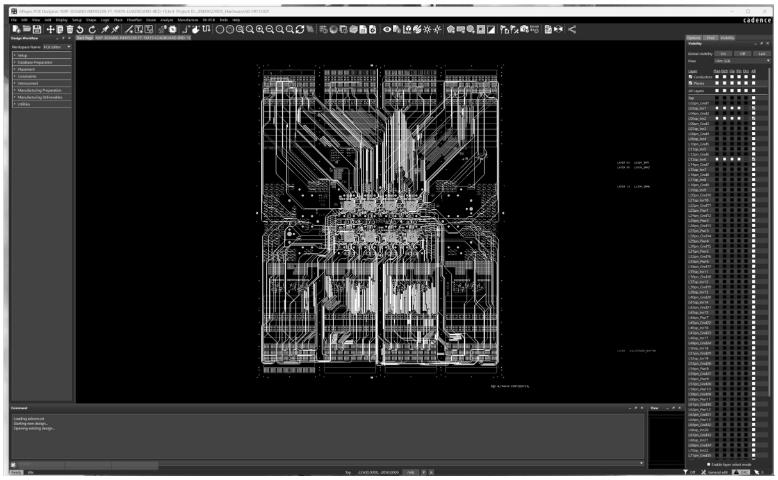
AI(ARTIFICIAL INTELIGENCE)
THE IP-TECHNOLOGY THEFT TODAY

Intellectual Property



Secured eco system is a must to prevent IPs and associated data don’t end up on public AI data base

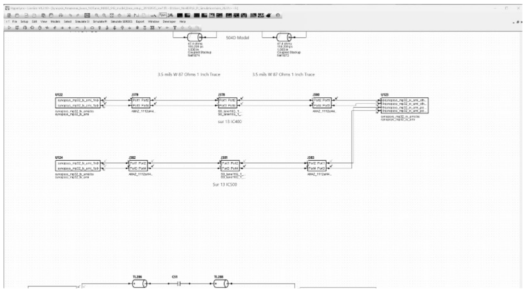
Cadence: EDA Tool Specific AI Implementations



AI Tools for
- PCB Design
- Package Design
- SI Analysis
- PI Analysis

AI IP Security
- AI eco system with Cadence
- Exclusive eco-system
- IP Security
- Exposure and accountability

Siemens: EDA Tool Specific AI Implementations



Key Aspects of the HyperLynx AI Capabilities
- AI-Assisted User Experience (UX):
- Predictive Engineering & Optimization:
- Automation of Routine Tasks:
- Intelligent Support: Unified Platform:

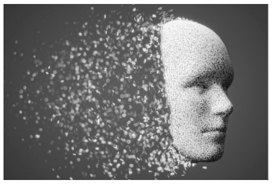
AI IP Security
- AI eco system with Siemens
- Exclusive eco-system
- IP Security
- Exposure and accountability

Siemen HyperLynx AI Tool Kit

Key Aspects of the HyperLynx AI Capabilities

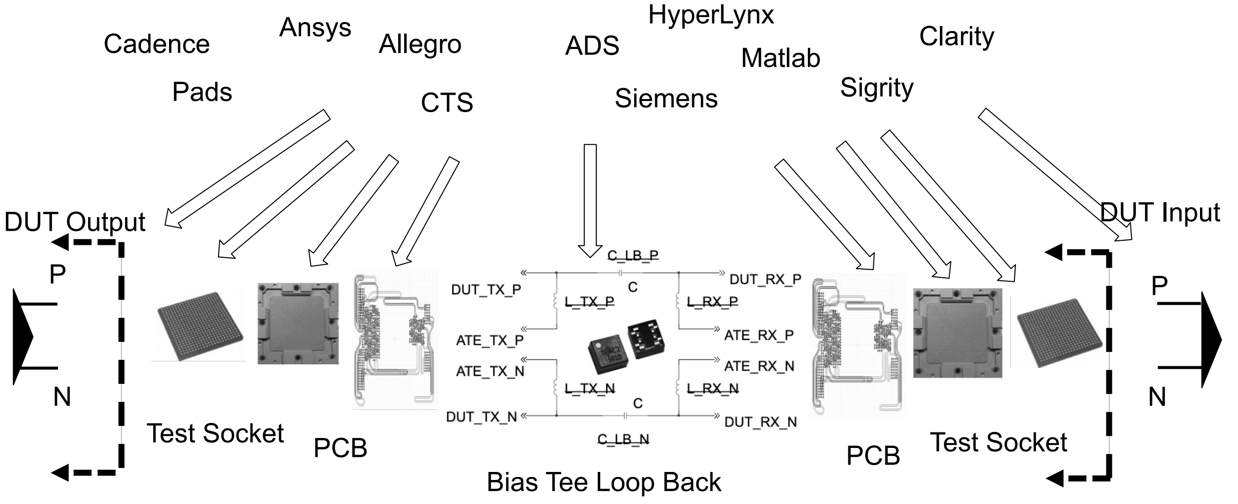
- **AI-Assisted User Experience (UX):** The next-generation release features a modern, intuitive UX designed to improve productivity. It includes AI-driven command prediction, which utilizes trained models to anticipate the next steps in the design process, reducing the need for manual searching and menu navigation.
- **Predictive Engineering & Optimization:** The toolkit uses AI/ML techniques to optimize design workflows. It provides intelligence for early detection of design flaws and suggests improvements to optimize performance.
- **Automation of Routine Tasks:** AI helps automate repetitive, non-expert tasks, allowing designers to focus on high-level innovation rather than tedious simulation setup.
- **Intelligent Support:** The AI-enhanced tools can analyze design data sheets and learn the software's functionality to provide relevant, context-aware help, reducing the learning curve for new users.
- **Unified Platform:** The AI features are integrated into a unified environment connecting Xpedition, PADS Professional, and HyperLynx, enabling seamless data flow between schematic, layout, and simulation

Inference from a limited database or eco-system to protect IP



Limited Learning to start with

Intellectual Property; Fragmented Design Ecosystem



Cadence

Pads

Ansys

Allegro

CTS

ADS

HyperLynx

Siemens

Matlab

Sigrity

Clarity

DUT Output

DUT Input

Test Socket

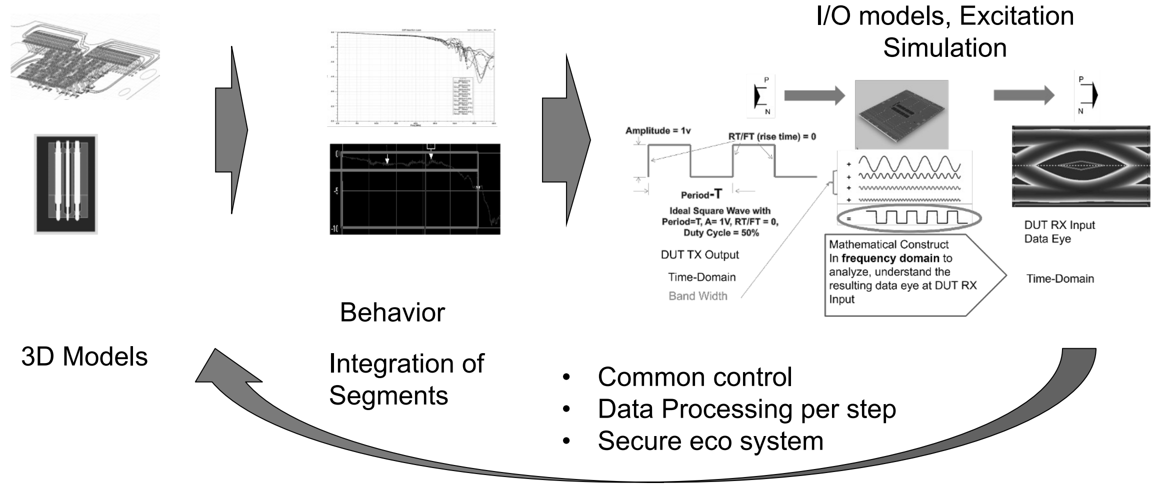
PCB

Bias Tee Loop Back

PCB

Test Socket

Complex Technology to maximize capability and or specialized EDA tools



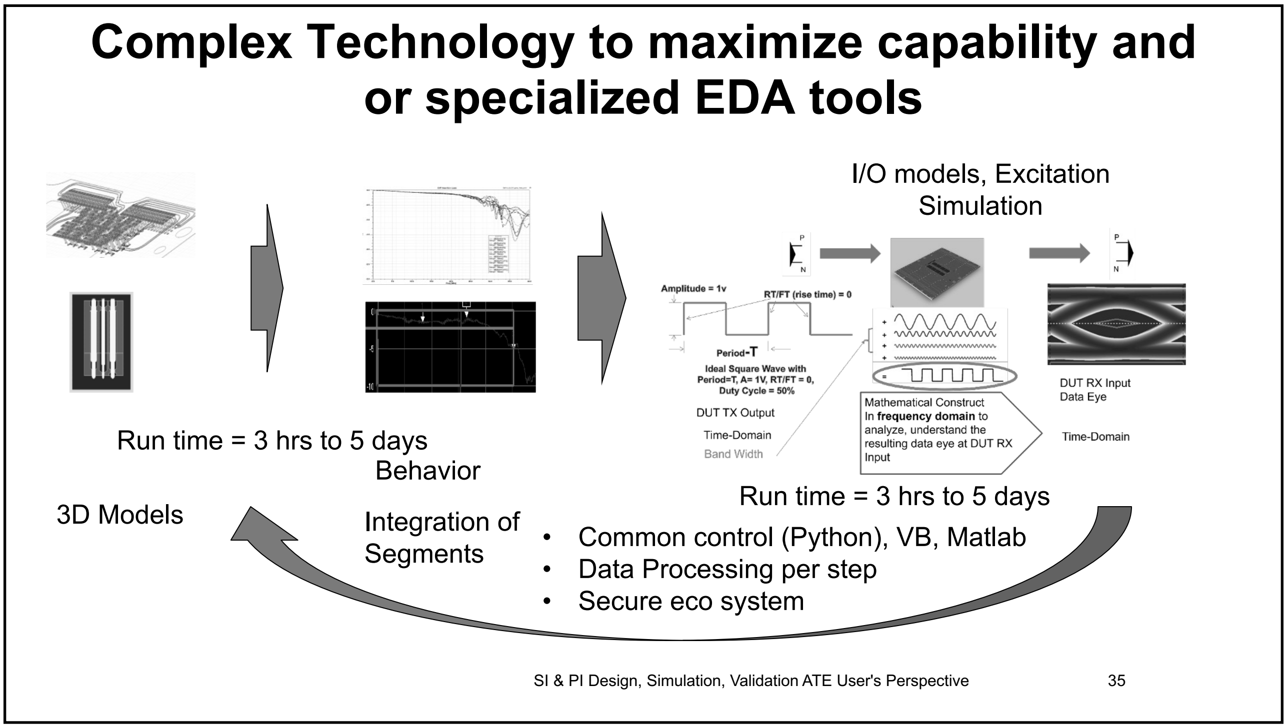
I/O models, Excitation Simulation

3D Models

Behavior

Integration of Segments

- Common control
- Data Processing per step
- Secure eco system



Complex Technology to maximize capability and or specialized EDA tools

Mathematical Construct In **frequency domain** to analyze, understand the resulting data eye at DUT RX Input

Run time = 3 hrs to 5 days

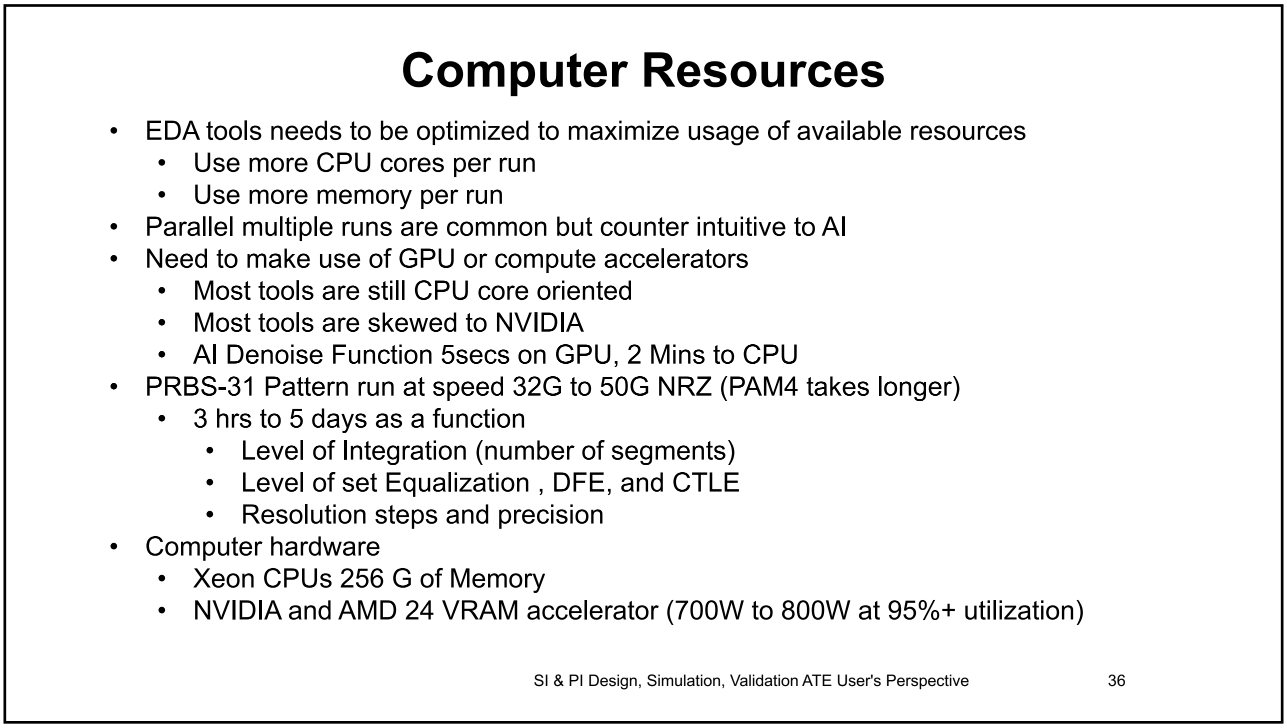
Behavior

3D Models

Integration of Segments

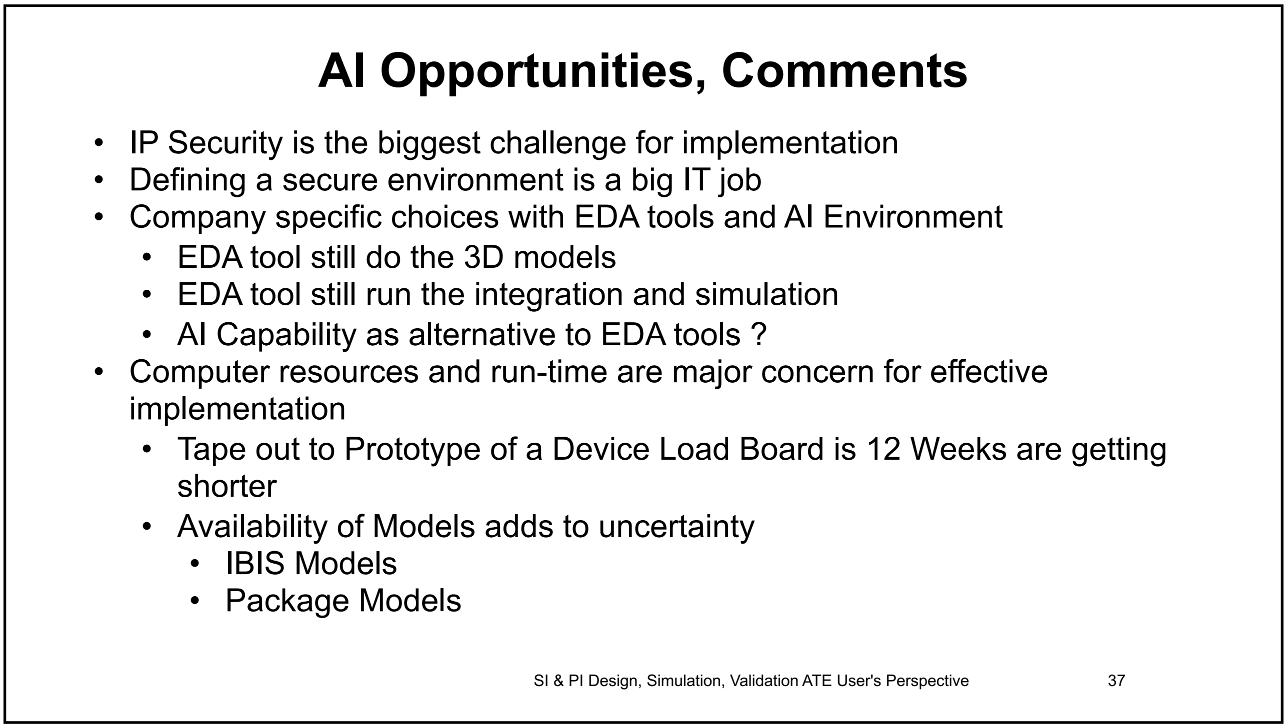
Run time = 3 hrs to 5 days

- Common control (Python), VB, Matlab
- Data Processing per step
- Secure eco system



Computer Resources

- EDA tools needs to be optimized to maximize usage of available resources
  - Use more CPU cores per run
  - Use more memory per run
- Parallel multiple runs are common but counter intuitive to AI
- Need to make use of GPU or compute accelerators
  - Most tools are still CPU core oriented
  - Most tools are skewed to NVIDIA
  - AI Denoise Function 5secs on GPU, 2 Mins to CPU
- PRBS-31 Pattern run at speed 32G to 50G NRZ (PAM4 takes longer)
  - 3 hrs to 5 days as a function
    - Level of Integration (number of segments)
    - Level of set Equalization , DFE, and CTLE
    - Resolution steps and precision
- Computer hardware
  - Xeon CPUs 256 G of Memory
  - NVIDIA and AMD 24 VRAM accelerator (700W to 800W at 95%+ utilization)



AI Opportunities, Comments

- IP Security is the biggest challenge for implementation
- Defining a secure environment is a big IT job
- Company specific choices with EDA tools and AI Environment
  - EDA tool still do the 3D models
  - EDA tool still run the integration and simulation
  - AI Capability as alternative to EDA tools ?
- Computer resources and run-time are major concern for effective implementation
  - Tape out to Prototype of a Device Load Board is 12 Weeks are getting shorter
  - Availability of Models adds to uncertainty
    - IBIS Models
    - Package Models

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February 28 - March 3, 2027 ◆ **Mesa, Arizona**

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Share your latest work and advancements as an **AUTHOR**! Your presentation or poster will be part of a stimulating and comprehensive program. Explore a demanding topic as a **TUTORIAL INSTRUCTOR**. Share your expertise with participants eager to build their leading-edge skills. Proposals addressing a broad range of burn-in and test subjects are welcome, including, but not limited to:

- Socketing/Contacting of Contemporary and Advanced Packaging Technologies
- PCBs, Materials, Handlers, Contact
- Technologies, Burn-in Tooling
- Modeling, Characterization & Analysis
- Process & Operational Challenges
- WLCSP Test for KGD or Final Test
- MEMS and Non-Electrical Stimuli Test

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