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Thermal Risk Mitigation Strategies for Back-End Testing in Emerging HPC Test Equipment

Bunmi Popoola
Paul Kim
Intel



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Introduction

- Rapid advancements in high-performance computing (HPC) have significantly increased semiconductor complexity.
- Emerging materials, architectures, and packaging techniques are driving power densities beyond the limits of conventional cooling, intensifying thermal challenges during back-end Testing.
- Back-end (BE) test is now a primary control point for managing thermal risk before products reach burn-in and system deployment

Presentation Goals

- Describe how advancements in high-performance computing (HPC) are reshaping thermal challenges in back-end test environments
- Identify the key technology drivers contributing to these evolving thermal risks
- Provide actionable recommendations to improve thermal control, correlation, and scalability in back-end test

Technology Drivers and Device Evolution

- Wafer- and Package-Level Scaling
- Specialized Packaging Techniques
- Advanced Materials and Interfaces
- Evolving Cooling Architectures



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Thermal Risk Mitigation Strategies for Back-End Testing in Emerging High Performance Computing Test Equipment

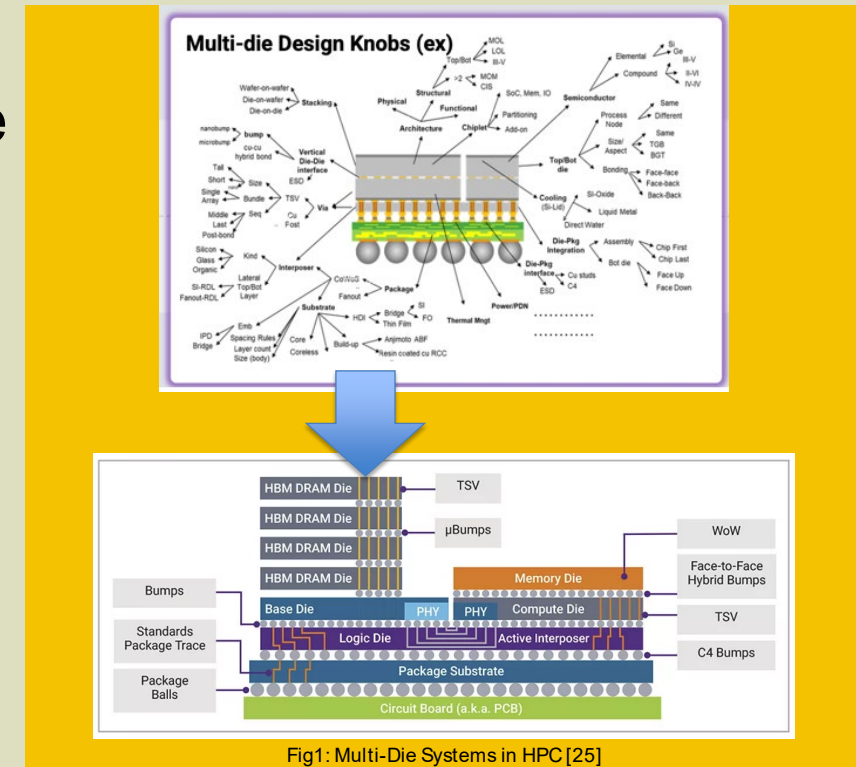
Specialized Packaging Techniques

Advanced Packaging Technologies

- 2.5D/3D integration, chiplet architectures, hybrid bonding, and multi-die systems significantly increase interconnect density and architectural complexity

Modular System Design

- Modular designs decompose monolithic dies into multiple functional blocks (chiplets, tiles, stacked dies).
- While total package power may remain similar, power is no longer spatially averaged.



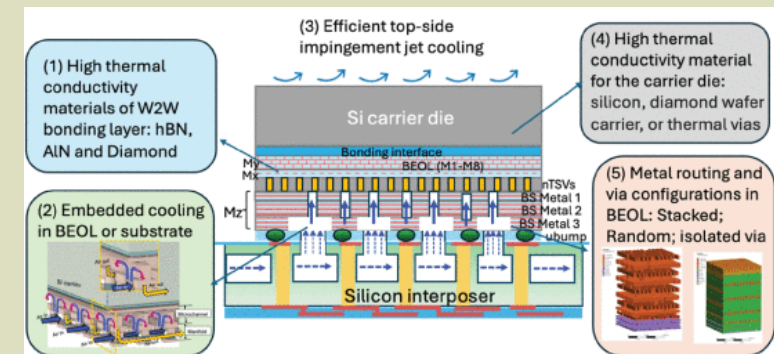
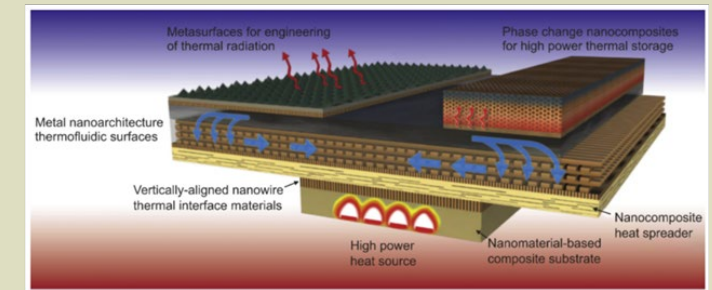
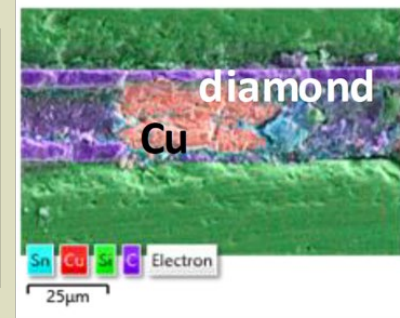
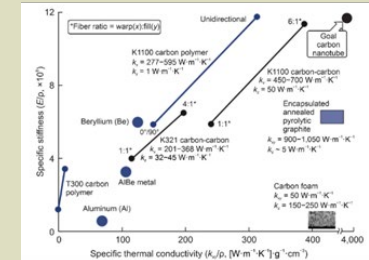
Thermal Implications of Advanced Packaging

- Localized power density & hotspots formation
- Strong die-to-die / block-to-block thermal crosstalk
- Vertical & lateral thermal gradients across the package
- Parallel die activation during test Operations
- Increased transient heating during power steps
- These effects undermine steady-state assumptions and reduce thermal controllability during back-end test.



Advanced materials innovation & integration

- Toward a “Material Architecture” Approach
 - Silicon packaging is evolving beyond passive encapsulation toward integrated, multi-material and multi-phase thermal solutions.
 - Solid, liquid, and gas phases are increasingly combined to manage extreme heat flux densities.
- This shift goes beyond basic encapsulation, aiming to develop active, multi-material, and multi-phase thermal management solutions integrated directly within the package.
 - By embedding active, multi-material, and multi-phase thermal solutions inside the package, advanced materials fundamentally alter thermal physics



Advanced materials innovation & integration (Multi-material, multi-phase, active thermal elements)

- Key Advanced Materials
 - Diamond films & carbon composites:
 - Diamond films can exceed $1000 \text{ W/m}\cdot\text{K}$, enabling rapid heat spreading but amplifying transient behavior.
 - Carbon nanotubes (CNTs): extremely high theoretical conductivity at nanoscale
 - Thermal interface materials (TIMs) & phase-change materials (PCMs): buffer transient loads and reduce interface resistance

Advancement in Cooling Technologies

- Cooling Capability Is Increasing Rapidly.

Cooling Innovation	Power Density (W/cm ²)	Thermal Ramp Rates (°C/s)
Silicon microchannels	100–1000	20–30
Diamond microchannels	250–1000	200–300
Direct-on-chip / package-level microfluidic cooling	300–1700	20–100

- Key Observations
 - Advanced cooling technologies enable unprecedented power densities and heat flux removal.
 - While aggressive cooling improves survivability, it can mask intrinsic silicon and package weaknesses, reduce test correlation, and destabilize closed-loop thermal control.
 - Cooling capability is no longer the limiter—thermal controllability and correlation are.

Challenges for Back-End Test Thermals

- Emerging HPC devices introduce non-linear, transient, and spatially non-uniform thermal behavior that challenges traditional back-end test methods.
- Enabled through early thermal modeling, active thermal control (ATC), advanced cooling solutions, comprehensive metrology, and cross-functional collaboration.

BE Test Risk —Thermal Management

- Masked worst-case conditions during test
 - Aggressive cooling and spreading can hide intrinsic weaknesses, leading to escapes later in burn-in or system use.
- Reduced test correlation & predictability
 - Test outcomes increasingly reflect package-thermal behavior rather than silicon health.
- Increased yield, ramp, and schedule risk
 - More false fails, longer debug cycles, late recipe changes, and delayed production readiness.
- Requirement for Flexible and Adaptive Cooling Design tools
 - Convert design data into thermal / multiphysics models automatically

BE Test Risk — Thermal Management

- Non-linear & transient thermal behavior
 - Breaks steady-state test assumptions and destabilizes thermal control during power steps and DVFS.
- Amplified thermal crosstalk
 - Heat spreads more efficiently across dies/blocks, causing failures unrelated to test stimulus.
- Non-uniform cooling & localized hotspots
 - Average temperature looks safe while local regions exceed limits.
- High sensitivity to interfaces & mechanics
 - Results depend strongly on socket contact, pressure, flatness, and TIM uniformity—driving tool-to-tool variation.

Thermal Reliability — Early Detection and Mitigation Needs

- **Cross-functional thermal coordination**
Align silicon, package, test, and system architecture teams early in the design cycle.
- **Early detection and mitigation of thermal failures**
Identify risk conditions before burn-in, system validation, and field deployment.
- **Adaptive control of thermal zones**
Dynamically manage spatial and temporal temperature variation during test.
- **Full traceability of thermal events**
Capture, correlate, and analyze temperature excursions across tools, lots, and time.
- **Continuous improvement of test protocols**
Use data-driven feedback to refine test limits, recipes, and control strategies.

Thermal Reliability — Holistic Thermal Management Needs

- **Quantify, validate, and mitigate complex 3D and time-dependent thermal behavior**

Advanced packages exhibit spatial, temporal, and operational ("4D") thermal interactions that cannot be addressed with isolated test fixes.

- **Vertical stacking and ultra-thin dies (<100 µm)**

Increase power density while limiting heat dissipation paths.

- **Complex thermal pathways**

TSVs, micro-bumps, hybrid bonding, and interposers introduce non-uniform and coupled heat-flow behavior

- **Thermal reliability can no longer be addressed at a single layer—**

Silicon, package, test, and system behavior must be managed together.

Thermal Reliability — Proactive Methods and Modeling Gaps

- **Accurate modeling of materials and interfaces**
Capture temperature-dependent properties, contact resistance, and mechanical effects.
- **Coupled power and electro-thermal analysis**
Incorporate Joule heating, power transients, and multi-physics interactions.
- **Iterative, scalable modeling workflows**
Start with simplified models and progressively refine them as design and test data become available.
- **System-level consistency across design phases**
Preserve model fidelity and assumptions from silicon through package, test, and system to avoid correlation loss and manual errors.
- **Without proactive and consistent modeling, backend test becomes reactive rather than predictive.**



Advancement in Active Thermal Control (ATC) Required

- **Active Thermal Control Strategies**

- Closed-loop PID-based thermal control with dynamic set-point adjustment
- Device power following to coordinate electrical and thermal transients
- Strategic sensor placement for spatially resolved temperature feedback
- Continuous multi-stream data logging across time, sites, and zones
- Multi-site handlers and tri-temperature testing to support heterogeneous integration

- **Why ATC Is Required**

- Enables real-time adjustment, anomaly detection, and stable control under non-linear and transient thermal conditions.
- Supports parallel testing and improved correlation for advanced, multi-die HPC devices.

Eliminating Barriers to Innovative Cooling Technologies

Advanced cooling solutions are technically viable for high-volume manufacturing (HVM), but adoption is limited by system-level constraints.

Key Barriers

- **System integration and design complexity**
Advanced cooling must coexist with sockets, handlers, probes, and automation.
- **Material compatibility and long-term reliability**
New materials introduce risks related to aging, corrosion, and mechanical stability.
- **Leakage, contamination, and maintenance concerns**
Liquid-based solutions require strict control and monitoring.

Eliminating Barriers to Innovative Cooling Technologies

Key Barriers Cont'd

- **Standardization, cost, and scalability**
Lack of standards and high implementation cost limit widespread HVM deployment.

What Is Required

- A disciplined methodology to help test engineers balance thermal risk, performance, yield, and manufacturability.

Thermal Reliability — Thermal Mechanical Test Vehicle (TMTV)

- **TMTV is a thermal Twin of the package**
 - TMTVs emulate real product thermal and mechanical behavior under controlled conditions.
 - Configurable for chip topology, interconnects, substrates, memory, lid assembly, and TIM structures
- **Measurement and Data Collection**
 - Embedded heaters and sensors measure heat flow, temperature gradients, warpage, and mechanical deformation precisely.
 - Benchmarking cooling strategies, validating thermal models, Lid Assembly, TIM aging etc.
 - Controlled testing with TMTV to help refine designs and reduce risks prior to final silicon manufacturing.
- **Intel offers TMTV ☺**
 - TMTV platforms are available internally and through industry partners to support collaborative thermal validation.



Key Takeaways

- **Thermal behavior now drives BE test risk**
- **Cooling $\neq$ Control**
- **Holistic Methods Beat Local Fixes**
- **Discipline Enables HVM**

**Thermal reliability is no longer a downstream problem
— it must be designed, measured, and controlled from the start.**

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