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Test Strategies for Coaxial Socket Performance and Reliability

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Introduction

The growth of AI processors and GPUs drives increased use of coaxial sockets for component testing.

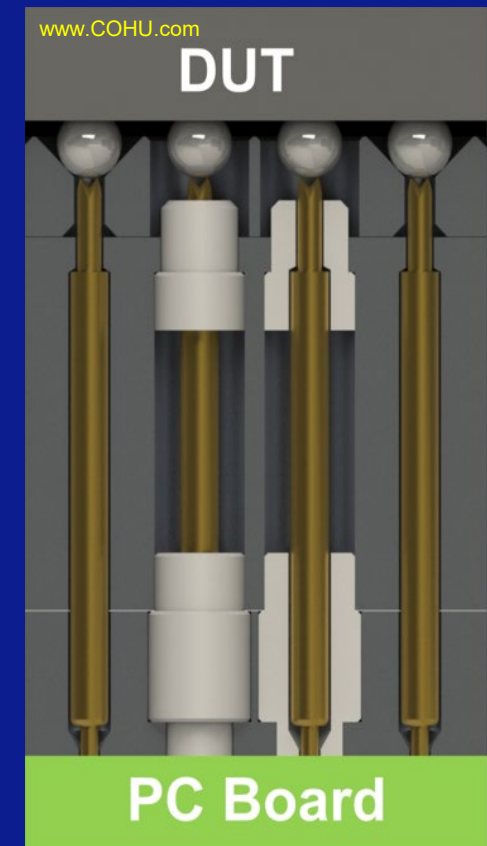
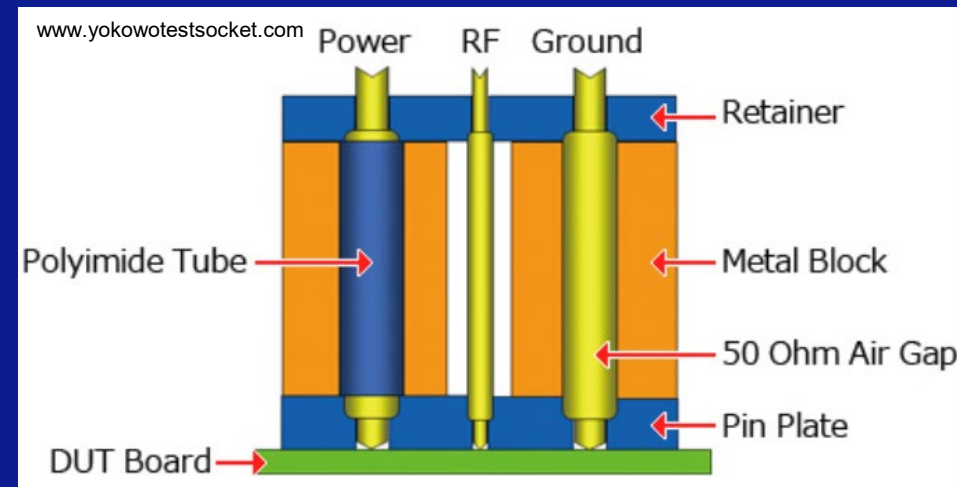
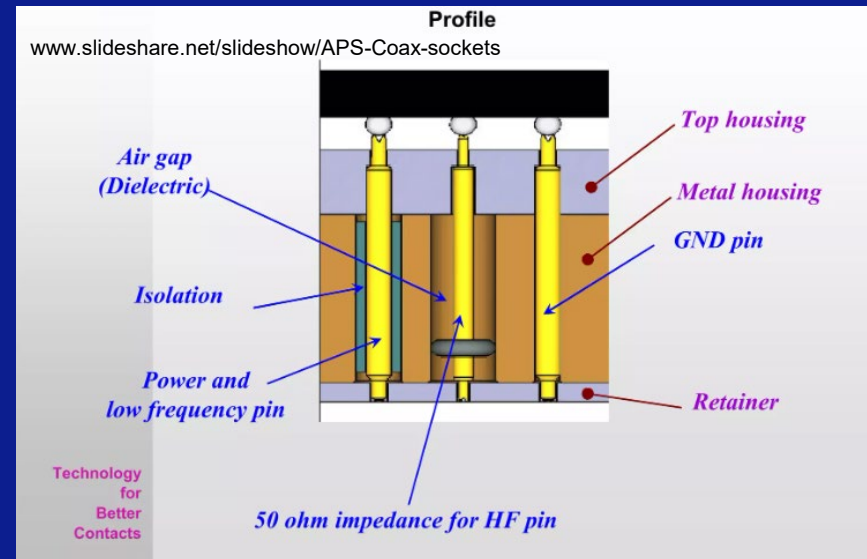
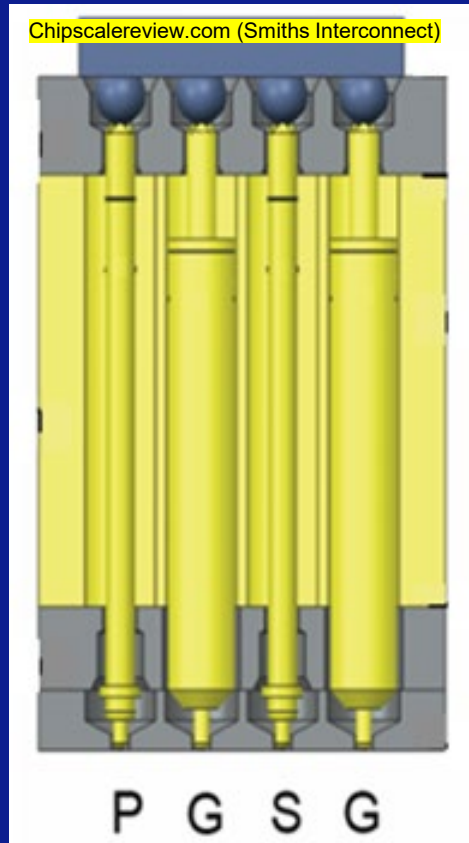
Coaxial sockets require precise contact resistance and shielding effectiveness measurements to ensure reliability.

Innovative testing strategies on these coaxial sockets improve performance of both first pass yield as well as improvement of speed bin performance.

Coaxial Socket Structure

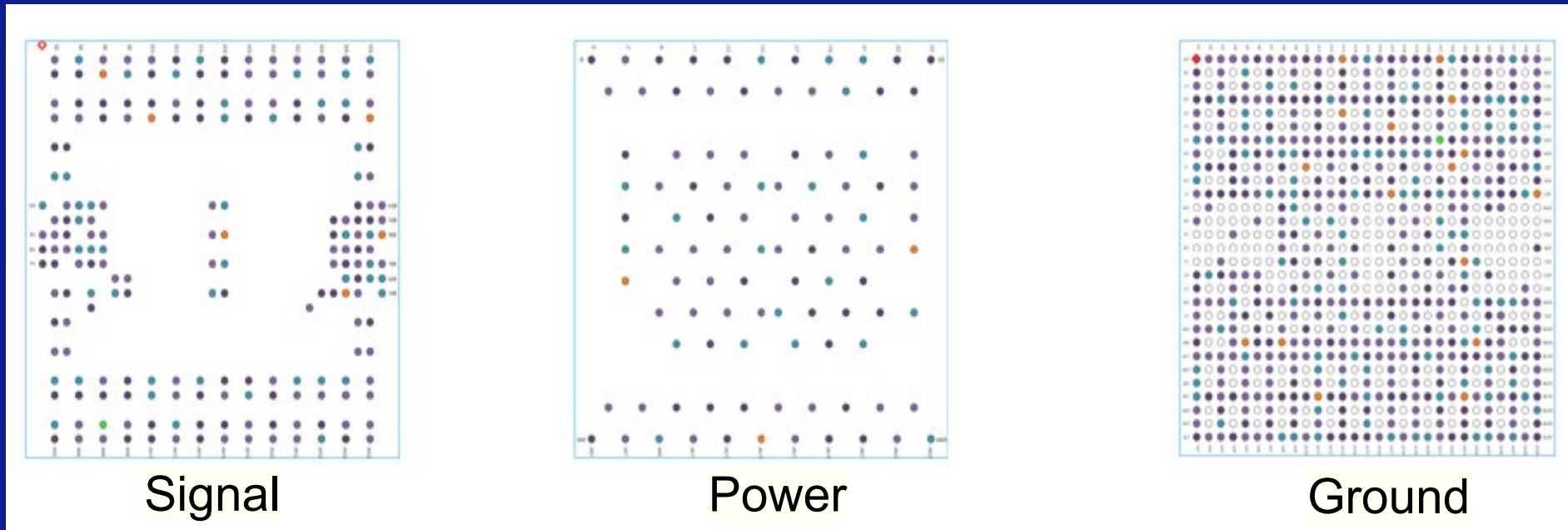
- Coaxial sockets feature three types of pin configurations
 - High speed signal pins (fully isolated)
 - High current power pins (fully isolated or isolated by domain)
 - High current VSS pins tied to an internal common ground plane.
- Shielding of the VSS pins is critical for maintaining signal integrity during high-speed testing and operation.
 - The internal common ground plane shields signal and power pins, reducing signal loss and crosstalk in high-speed applications.

Coaxial Socket Structures

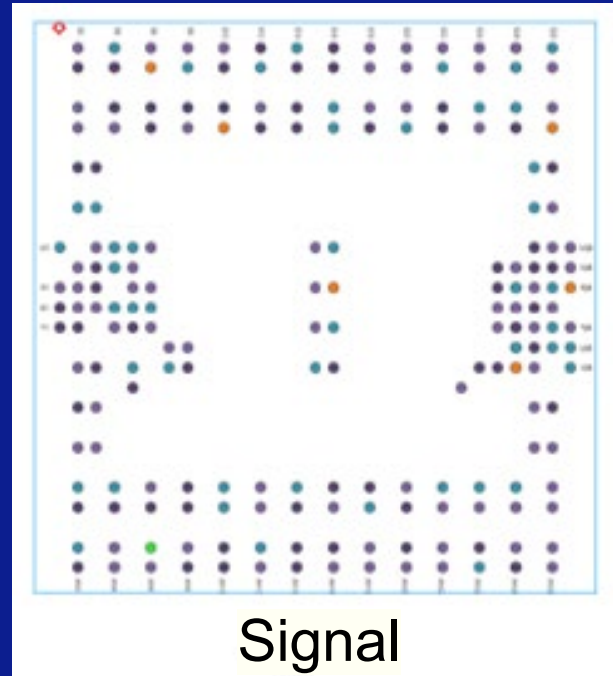


CRES Measurement Best Practice for Signal, Power, and Ground Pins

- For CRES testing, the socket is separated into 3 domains, Signal, Power, and Ground for independent measurement and better control of CRES limits per domain.

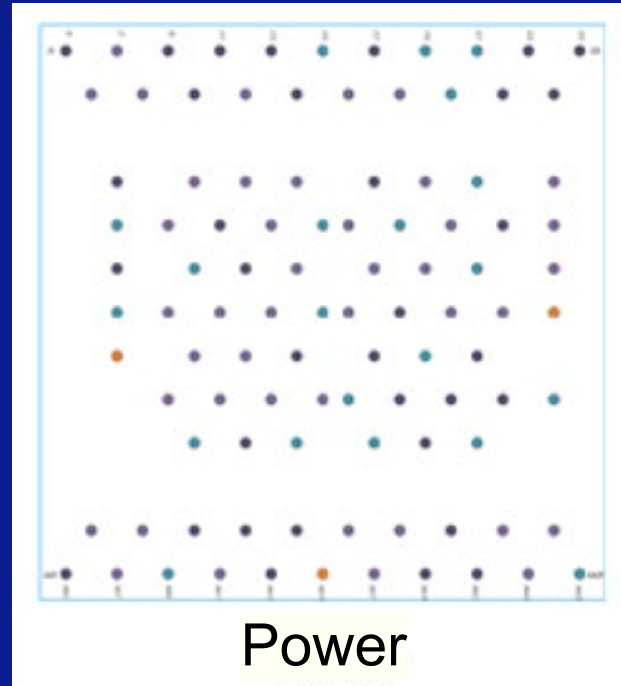


CRES Measurement Best Practice for Signal Pins



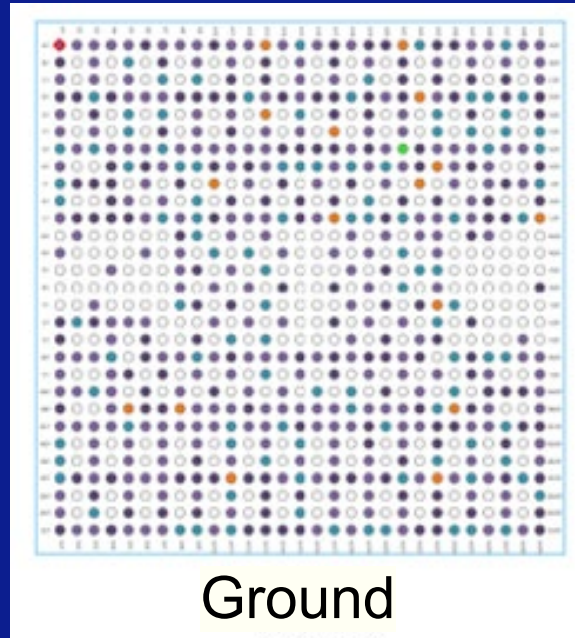
- Signal pins are measured using only other signal pins for the force/sense return paths. This prevents contamination of the distribution with data from other pin types in the array.

CRES Measurement Best Practice for Power Pins



- Power pins are measured using only other power pins for the return force/sense return paths. This prevents contamination of the distribution with data from other pin types in the array.

CRES Measurement Best Practice for Ground Pins



- VSS pins are measured using signal/power pins for the force/sense return paths.
- This ensures the point of the sense connection is within the shorting device and not the shielded housing.

Signal and Power Pin to Shielding Block Shorts Detection

- Signal and Power pins must be properly insulated from the pin body shield.
 - Shorts between power and ground pins can cause failures within the test module.
- The SHORT test method is used to check for shorts/leakage between the Signal/Power pins to the shielding block.
 - This method grounds all other points in the socket and measures the pin under test for shorts/leakage to all points in the array.
- Periodic testing of this isolation is recommended especially when any maintenance requiring pin replacement has occurred.

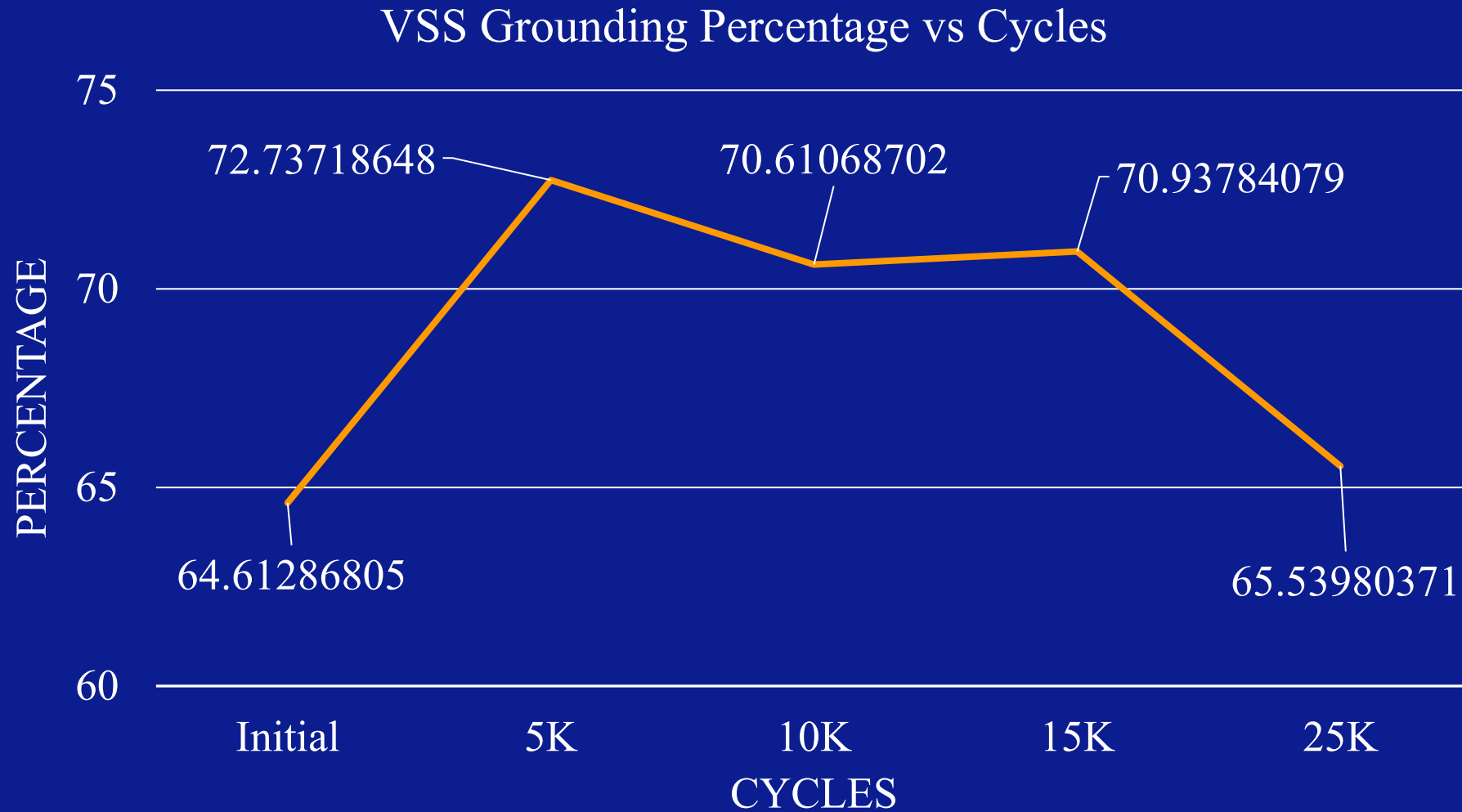
Ground Pin Contact to Shielding Block Percentage

- Ground pins that are electrically tied to the shielded block are designed to create a shield around the signal and power pins.
 - The shield performance is impacted by the DC resistance of the contact from the VSS pin to the shielding body. If the DC resistance is high, the shield will not provide an effective coaxial path for the signal pins.
- A measurement to determine the resistance of the VSS pin to the shield is required to determine the quality of the connection.
 - Unlike the pin tip contact which is designed for a high PSI point of contact to achieve low CRES this pin to housing connection is not typically designed to achieve a high PSI contact point. This results in resistance values typically in the low Ohm to Kohm range.

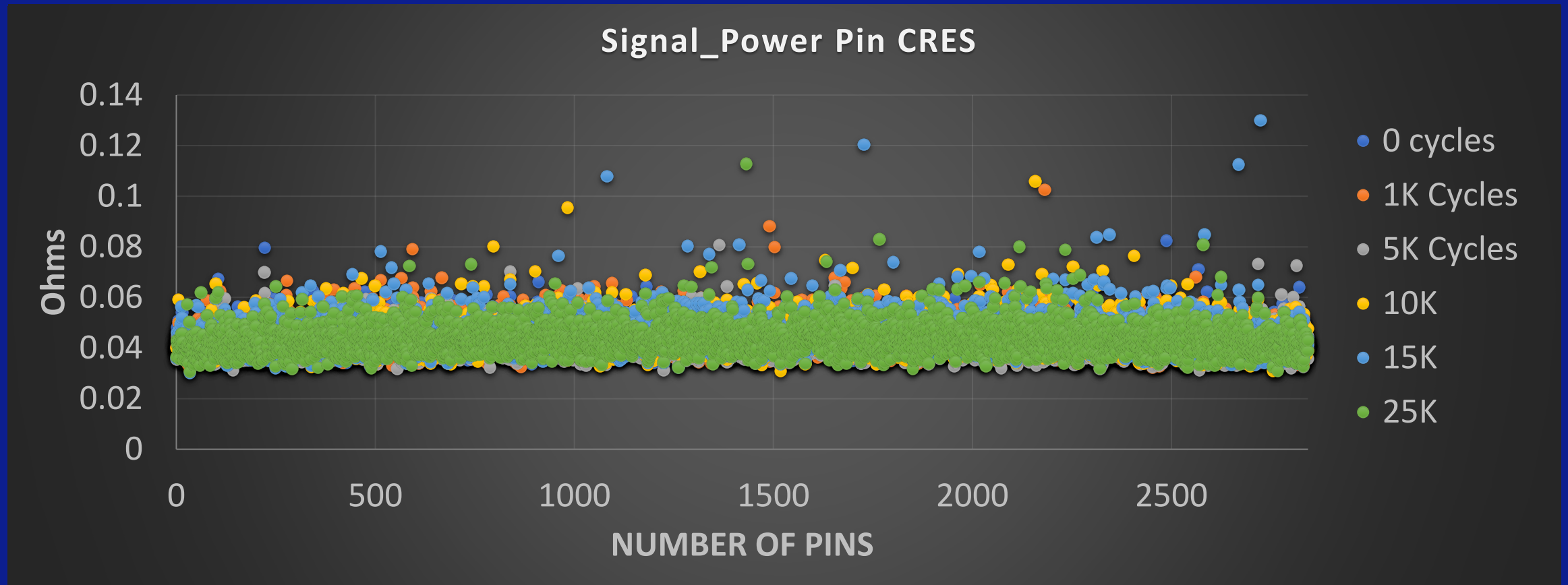
Ground Pin Contact to Shielding Block Percentage

- The OPEN test method measures the goodness of contact between the VSS pins and the shield housing. This method grounds all other points in the socket and measures the pin under test for contact to the shielded block.
- As a starting point confirm a very high percentage (>80% typical) of the VSS pins to make contact to the shield with a sufficiently low resistance value (<10 Ohm typical).
 - Limits need to be set based on socket design and correlation activities.
- This connection can degrade over time routine checks are recommended to guarantee performance over time.

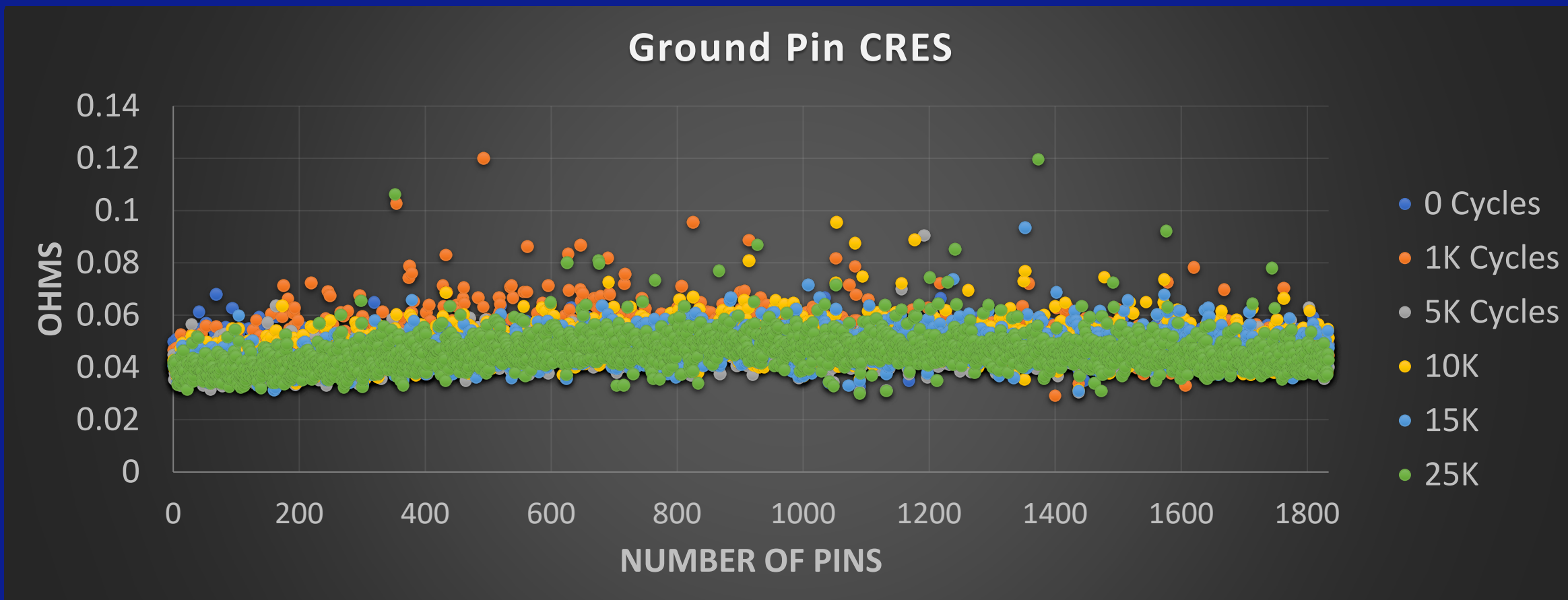
Ground Pin Contact <10 Ohm to Shielding Block Percentage



CRES Data Signal and Power Pins



CRES Data for Ground Pins



Benefits of Coaxial Socket Testing Strategy

- Optimized Socket Design
 - Data driven characterization enables improved socket designs, ensuring higher performance confidence,
- Quality Control Implementation
 - Applying testing strategies at outgoing quality control and customer sites maintains consistent socket performance.
- Enhanced Reliability and Yield
 - These strategies reduce module downtime, improve yields , and enhance reliability in high-speed device testing.

Conclusion

- The performance of coaxial sockets cannot be predicted by CRES measurements alone.
 - CRES alone is not a predictor of good test module yield.
- The shielding performance can and will likely change over time due to wear in the housing and the pins.
- Presence of oxides or foreign materials such as lubricants or cleaning solvents used in the manufacturing of the shielded housing can also affect performance.
- This can result in sockets that are passing from a CRES test perspective but are not yielding after extended use.

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