TWENTY-SEVENTH ANNUAL

TestConX™

Archive

DoubleTree by Hilton
Mesa, Arizona
March 1-4, 2026

Spring Pin Interconnects for ATE Test Fixtures: Myths vs Reality

Jose Moreira, Advantest Germany
Roland S. Timsit, Timron Scientific Consulting Inc.

Mesa, Arizona • March 1–4, 2026

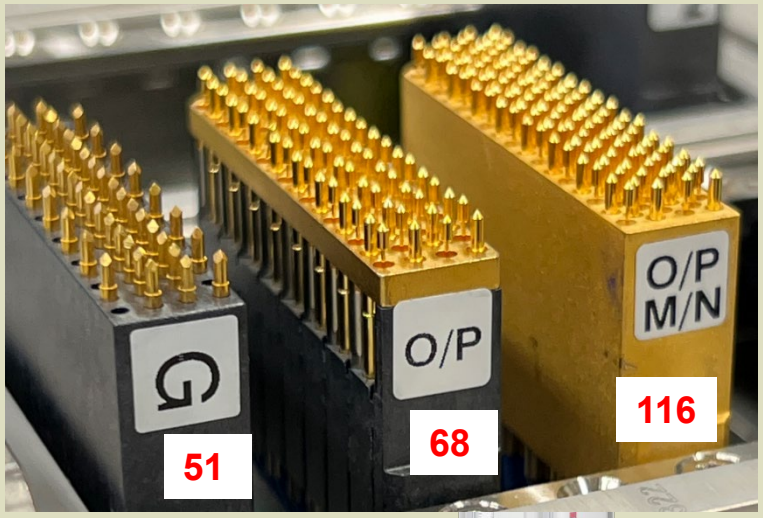
Contents

- ATE Spring Pin Interconnect Challenges
- Spring Pin to DUT Board PCB Mating Scenarios
- Computing the Interconnect Contact Resistance
- Measurement Results
- Conclusions

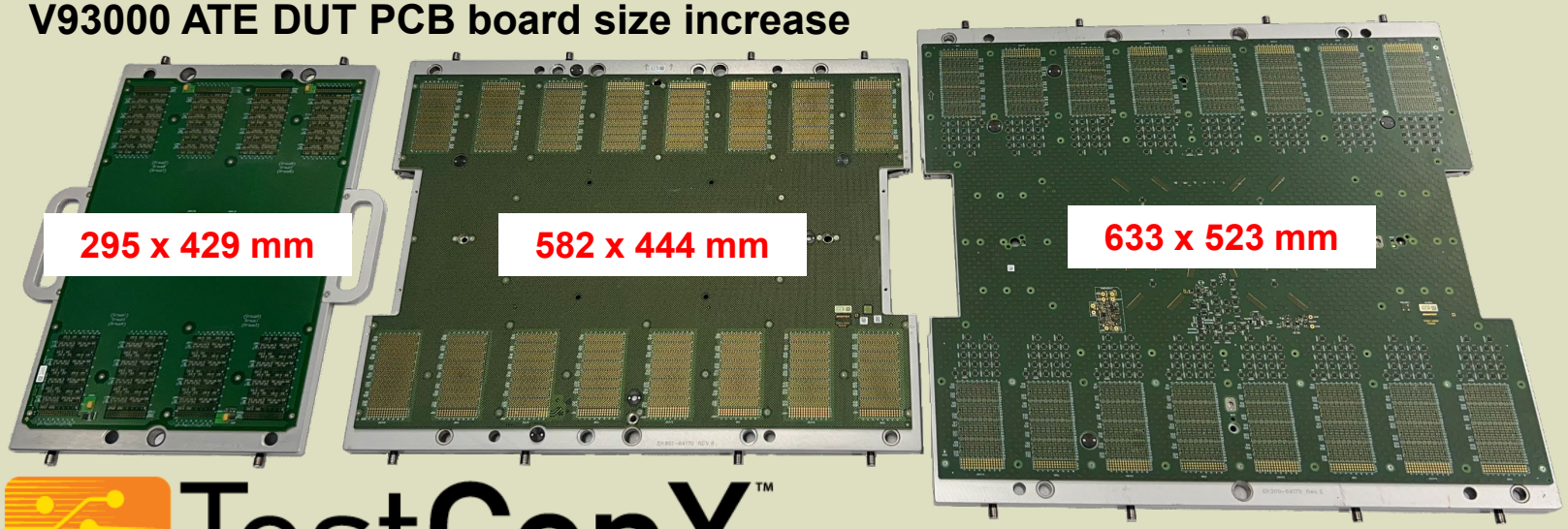
ATE Spring Pin Interconnect Challenges

- Spring pin interconnects (aka pogo pins) are the workhorses of automated test equipment (ATE).
- They are used in the ATE test head to connect to the DUT test fixture, in the DUT socket and in vertical wafer probe cards.
- AI/ML applications have created new challenges for ATE spring pin interconnects:
  - Large number of digital channels and power: requiring smaller spring pin pitch and lower contact force.
  - Larger size DUT Board PCBs and thicker (increased number of layers).

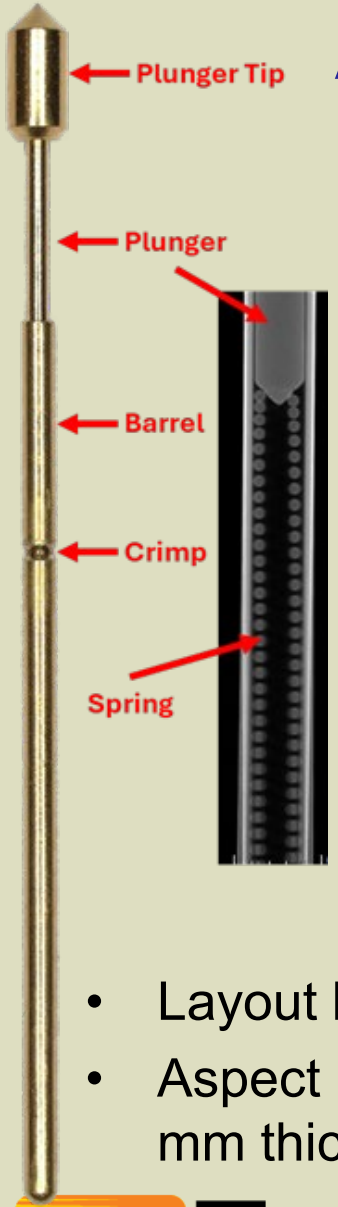
V93000 ATE pogo block density increase



V93000 ATE DUT PCB board size increase



ATE Spring Pin Interconnect Challenges



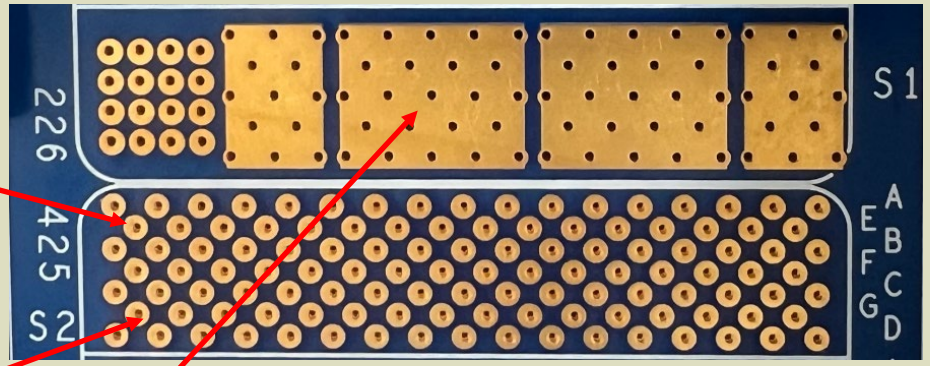
Spring pins in ATE test head interface

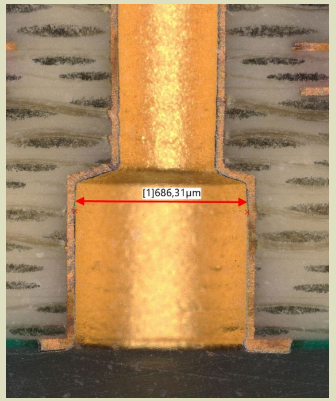
Digital

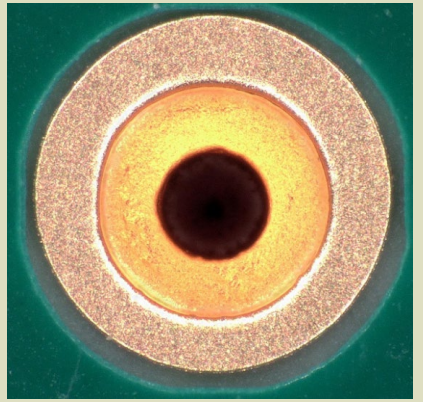
Power Supply

High-Current Power Supply

ATE DUT Board PCB footprint



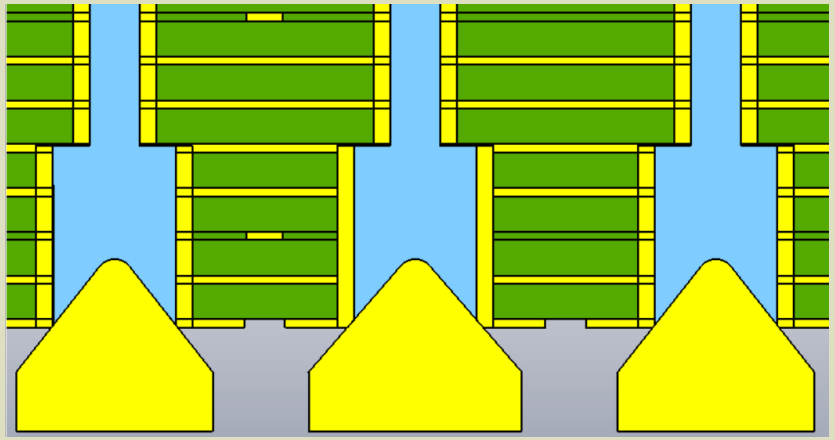




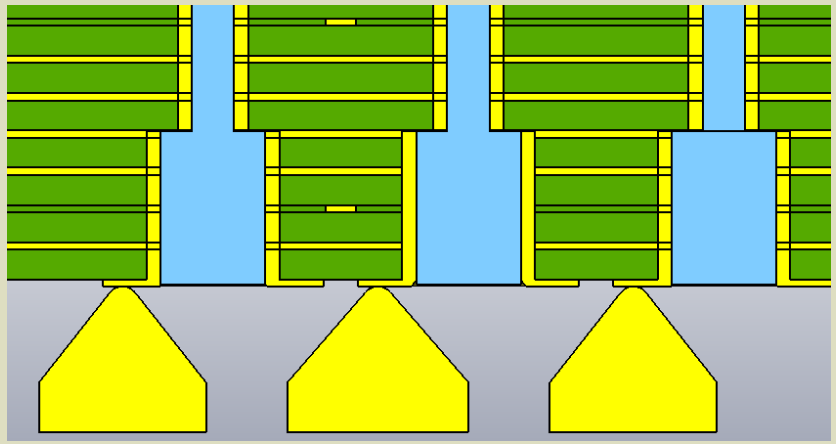
- Layout breakout in the spring pin area can be very challenging for very high-density DUT Boards.
- Aspect ratio and plating can be challenging for DUT boards with a large number of layers (e.g. 10 mm thickness)

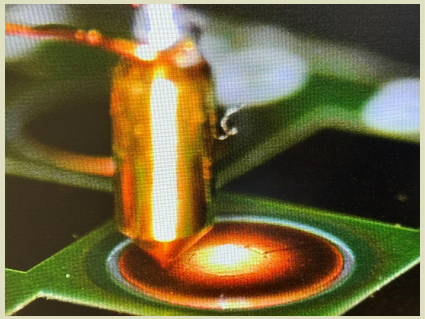
Spring Pin to DUT Board PCB Mating Scenarios

Spring Pin in Via Hole



Spring Pin in Via Pad



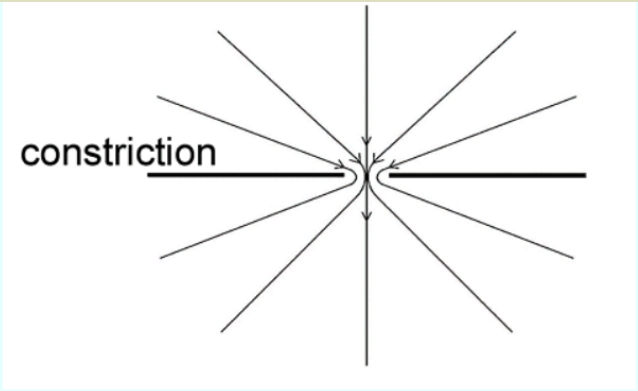


- The traditional expectation is to have a spring pin in via hole mating for optimal contact resistance.
- There are multiple factors contributing to the pointing accuracy of the spring pin tip and it's not possible to guarantee a 100% spring pin in via hole contact for every pin at every insertion. The via pad design rules are defined to guarantee there is always an electrical contact.
- A key question is what is the contact resistance difference in both scenarios.

Computing the Interconnect Contact Resistance

Fundamental law of contact surfaces:

$$\text{True Contact Area} = \frac{\text{Applied Contact Load}}{\text{Hardness}}$$

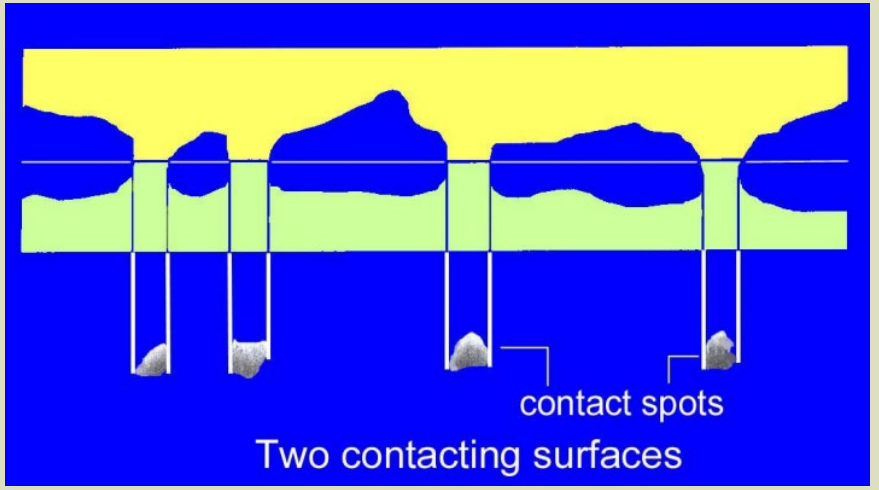


The *constriction resistance* or *contact resistance* of a single contact spot of average radius *a* is

$$R_C = \rho/2a$$

where ρ is the electrical resistivity

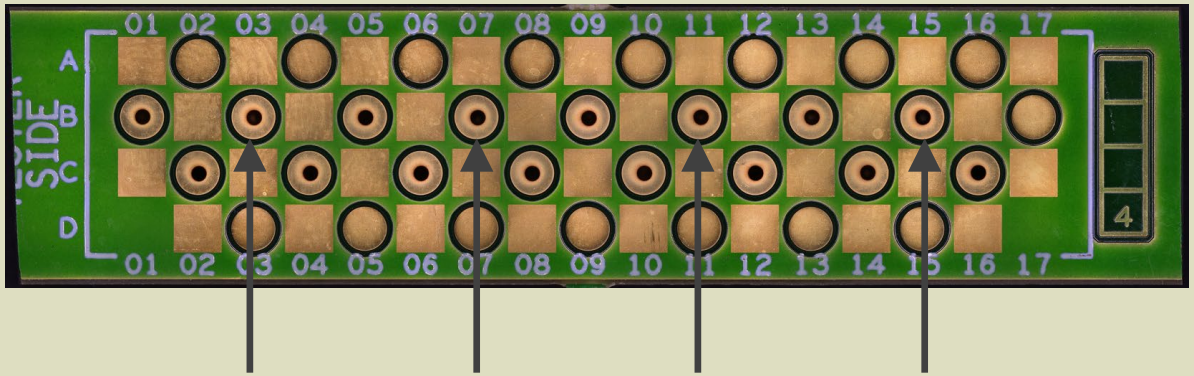
Area of mechanical contact between two solid surfaces



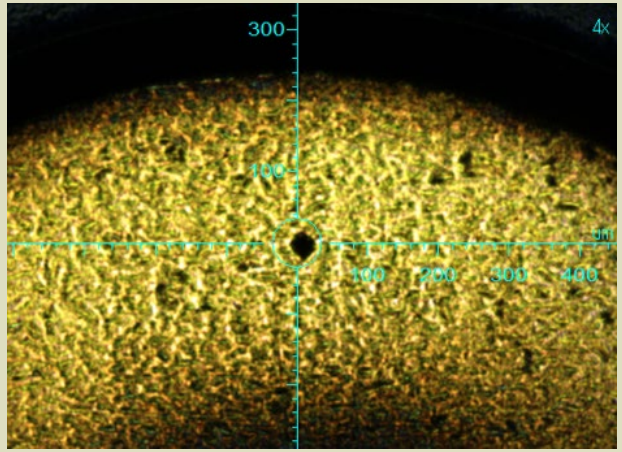
For computing the contact resistance, we need:

- The target spring pin nominal force.
- The material hardness.
- The Nickel/Gold plating applied to the spring pin and PCB via creates an added layer of complexity for the contact resistance computation.

PCB Plated Mating Via Hardness Measurement



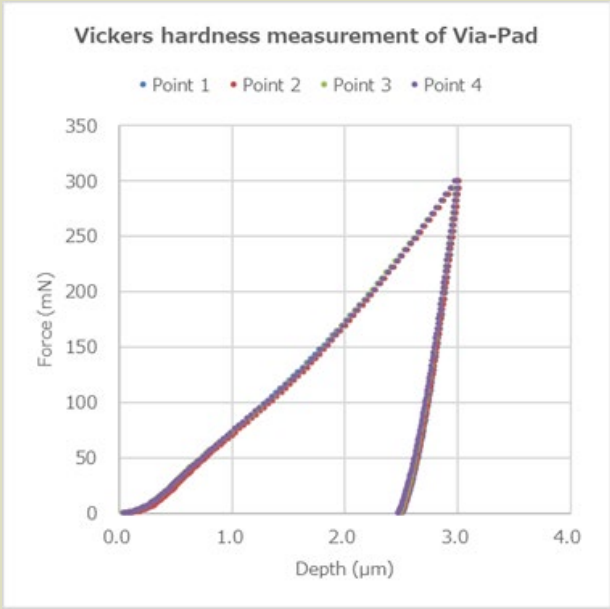
Measurement points



Vickers test marks

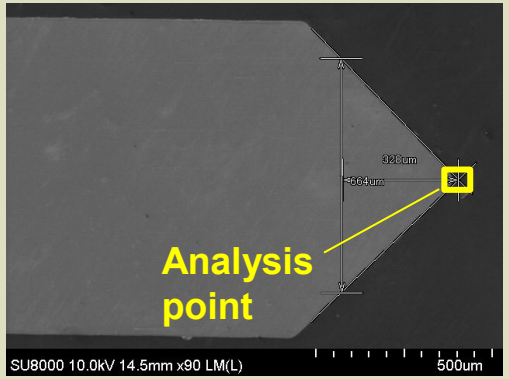
Vickers test results

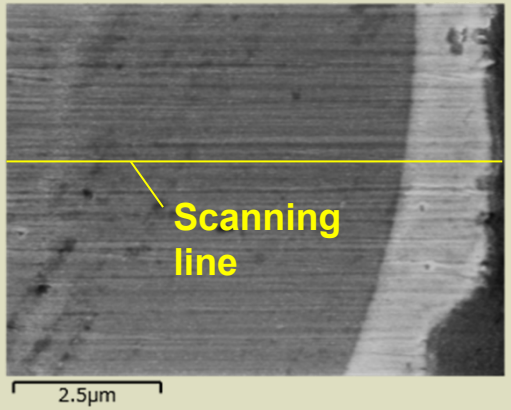
Test force	Point 1	Point 2	Point 3	Point 4
300 mN	185.7 HV	186.5 HV	189.0 HV	190.1 HV
600 mN	158.1 HV	147.1 HV	169.4 HV	141.7 HV

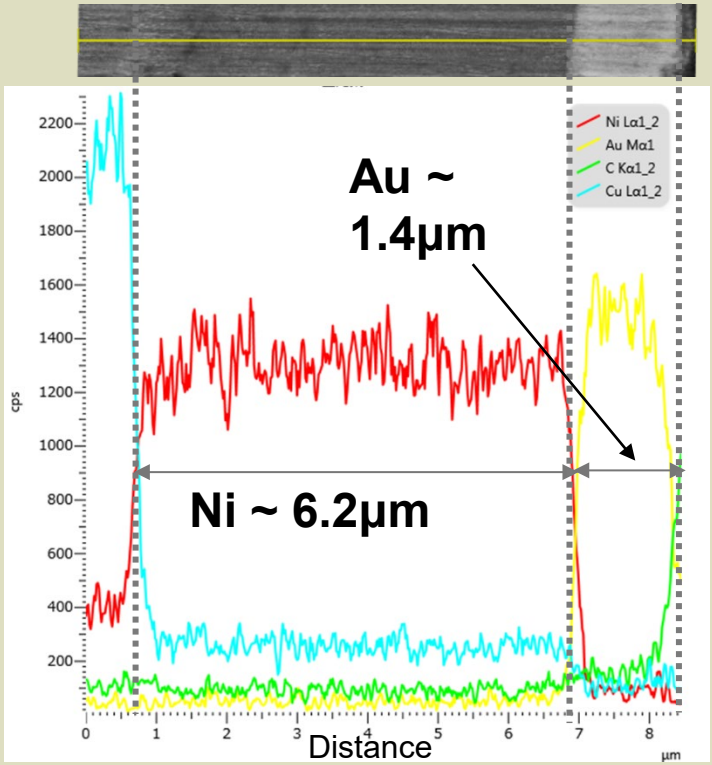


Plating Thickness Measurement

Spring Pin

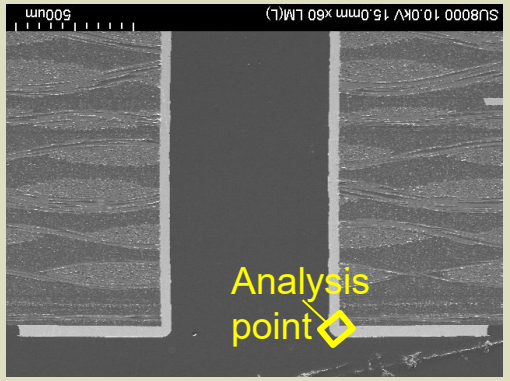


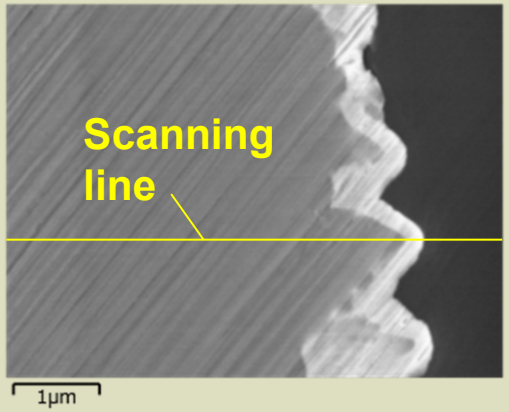


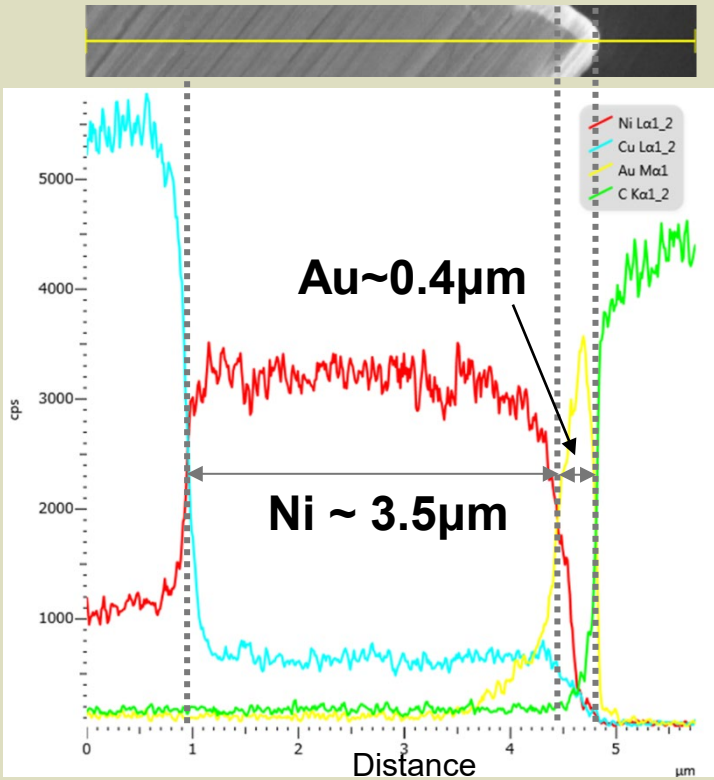


- Au Thickness: 1.4 µm.
- Ni Thickness: 6.2 µm.

PCB via





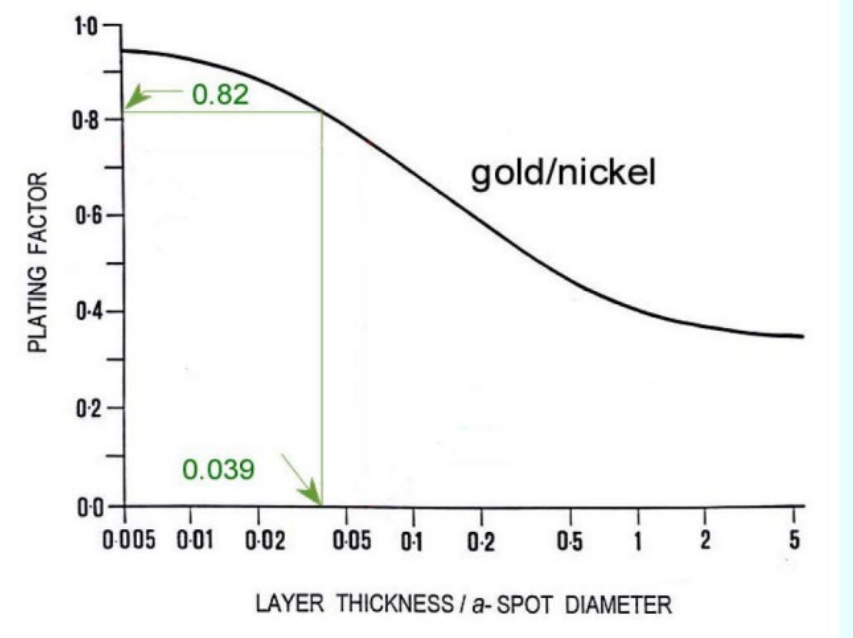


- Au Thickness: 0.4 µm.
- Ni Thickness: 3.5 µm.

Scanning Electron Microscopy (SEM) with Energy Dispersive Spectroscopy (EDS)

Contact Resistance Theoretical Computation

- The detailed computation of the contact resistance is outside the scope of this presentation and is planned to be presented in detail in a future paper.
- One key computation is the Plating Factor for the Au/Ni/Cu interface. Also, the geometry differences of the two scenarios play a critical role



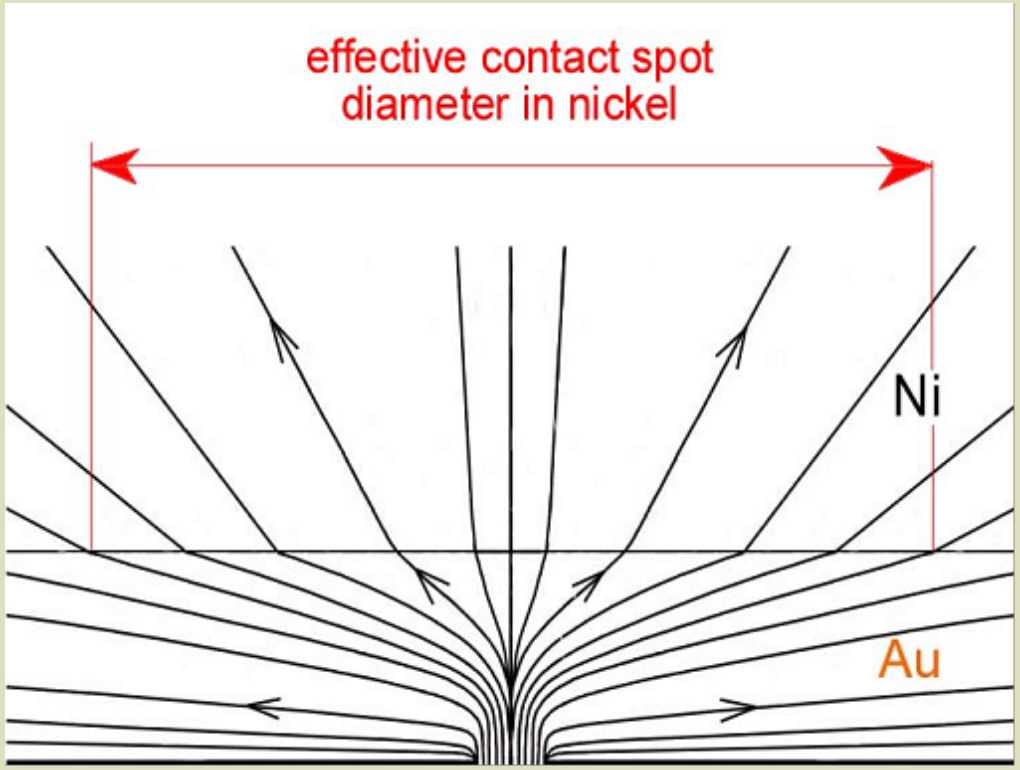
The Plating Factor is defined as

$$P_f = \rho_{eff}/\rho_{substrate}$$

where ρ_{eff} = the "effective" resistivity of the coated surface system (e.g. Au/Ni in this example)

$\rho_{substrate}$ = the resistivity of the substrate (e.g. Ni in this example)

Contact Resistance Theoretical Computation



The contact resistance due to a contact spot of radius *a* is then given as

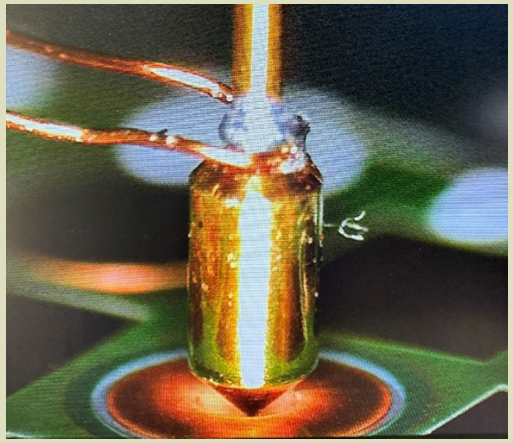
$$R_C = \rho_{eff}/2a = P_f \rho_{Ni}/2a = \rho_{Ni}/(2a/P_f)$$

This may be viewed as the contact resistance with a bare Ni surface with an effective radius a/P_f , **i.e. the presence of Au spreads current lines on Ni, thus effectively increases the contact spot radius if P_f <1. This reduces contact resistance.**

This effect is more pronounced in the case of a large ring contact, for example with the edge of a via hole.

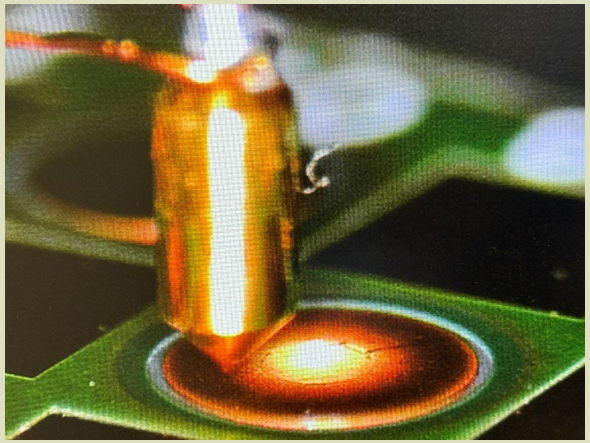
Contact Resistance Theoretical Computation

Spring Pin in Via Hole



- Force = 0.6 N.
- Plating Factor (Au/Ni/Cu) ~1 (because of the contact geometry).
- Rc=0.8 mOhm

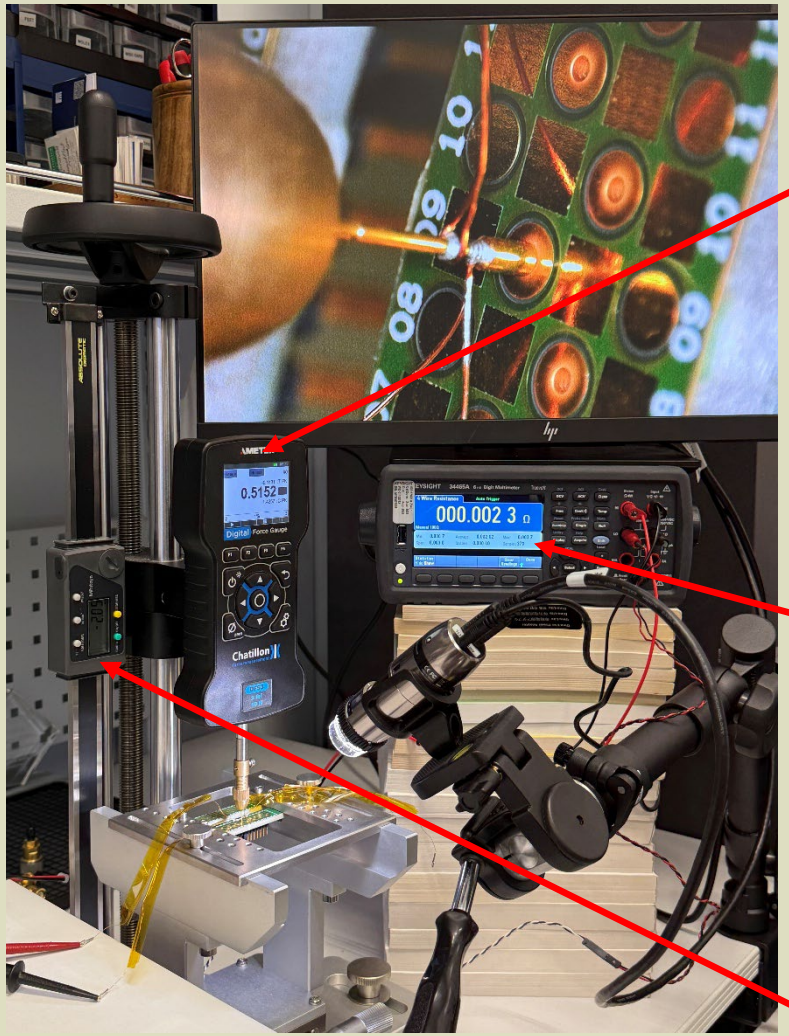
Spring Pin in Via Pad

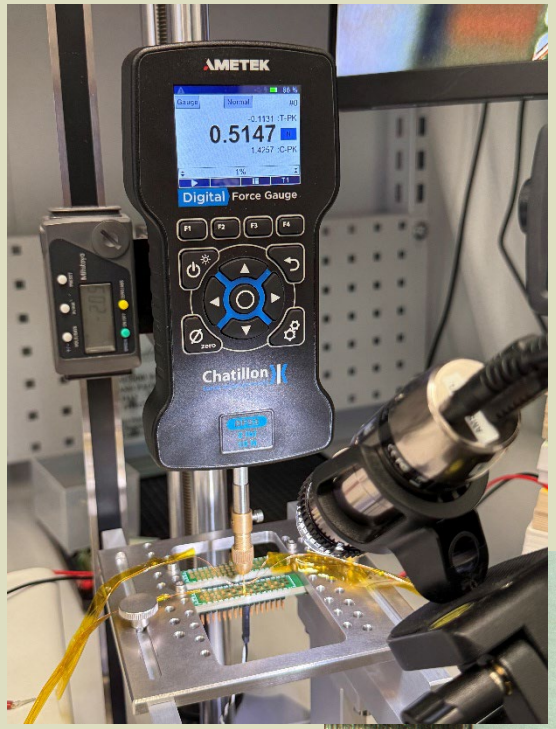


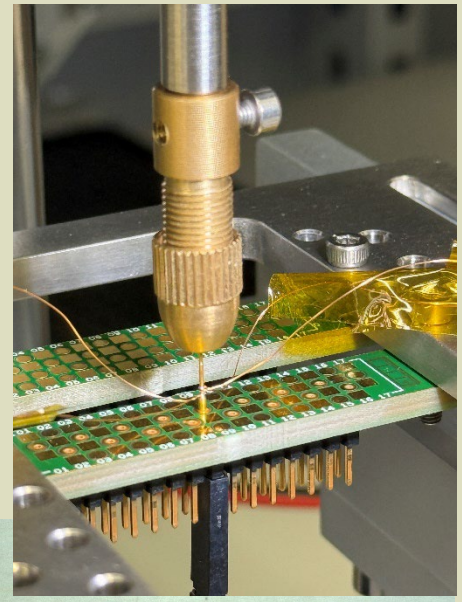
- Force = 0.6 N.
- Plating Factor (Au/Ni/Cu) = 3.2
- Rc=2.1 mOhm

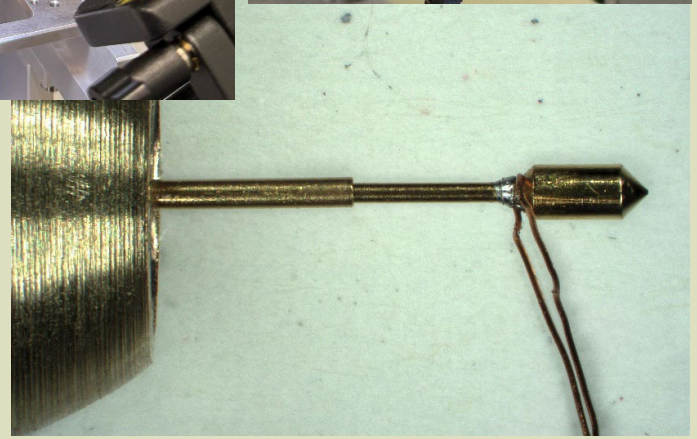
The contact resistance factor between both mating geometries is ~2.5

Contact Resistance Measurement Setup

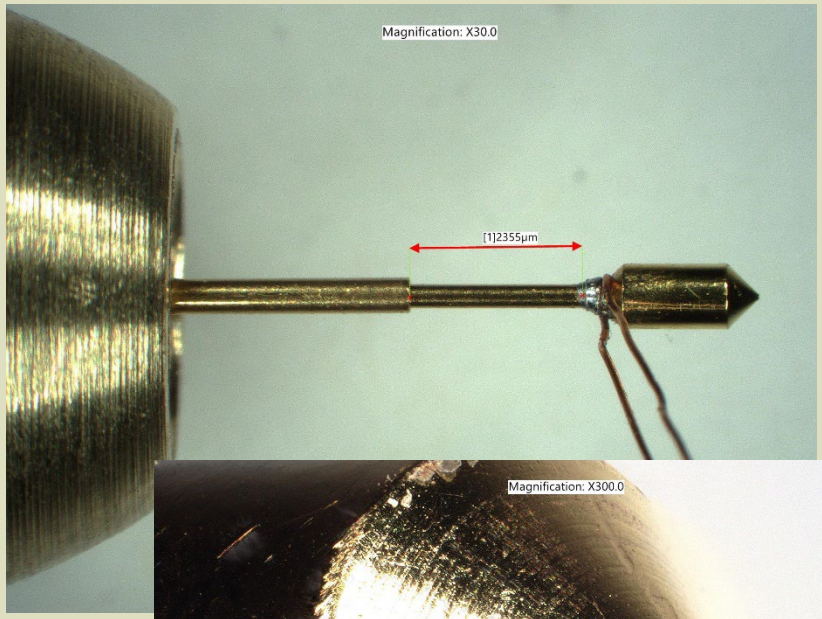


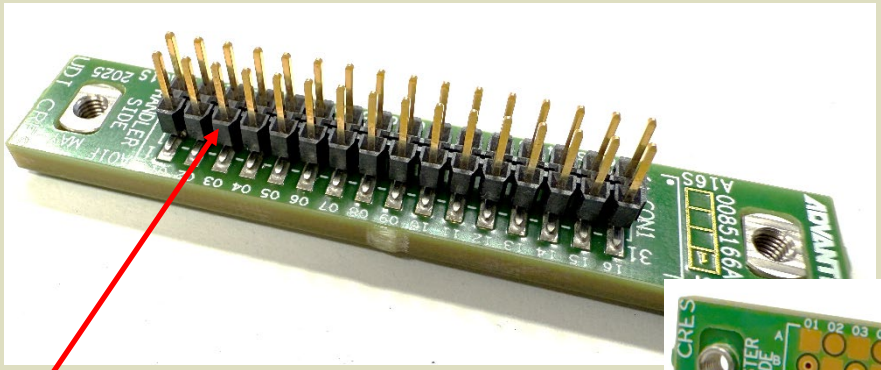




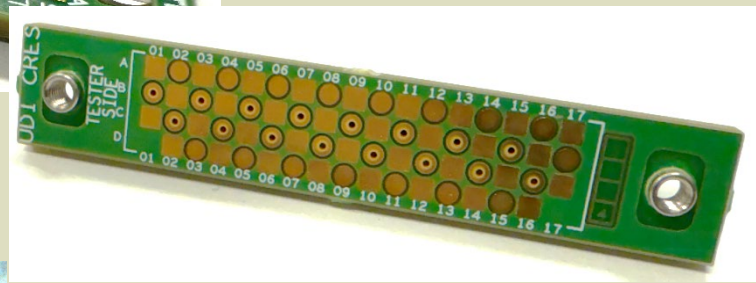


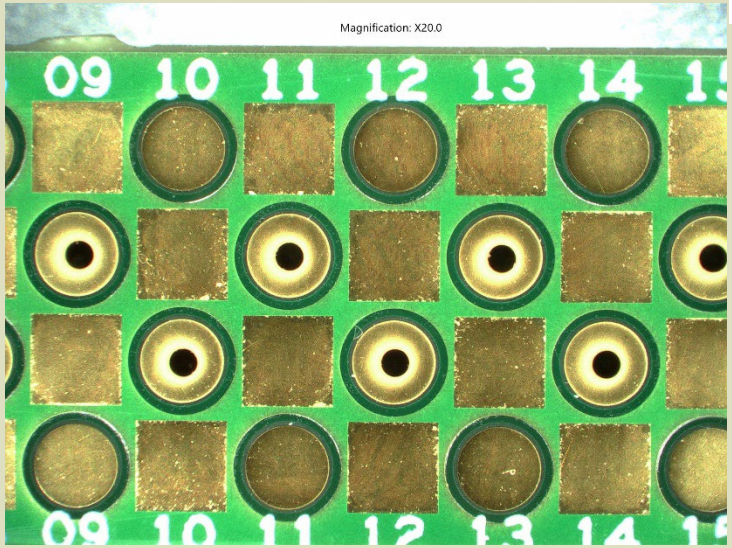
Contact Resistance Measurement Setup

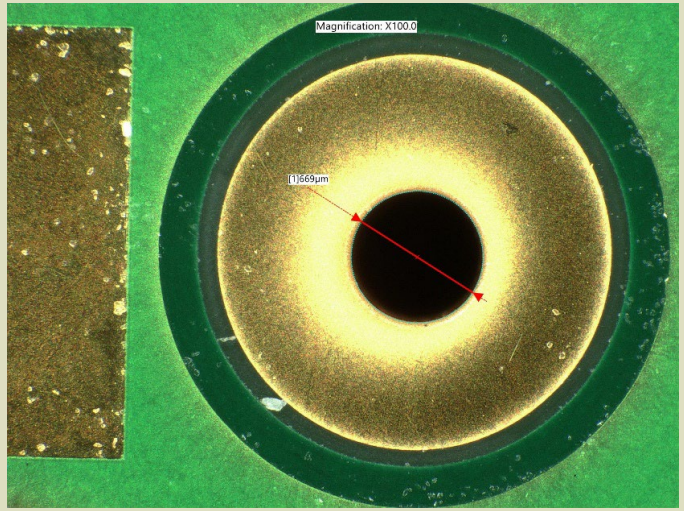




Force/Sense connector to instrumentation (Force/Sense connected at the via)



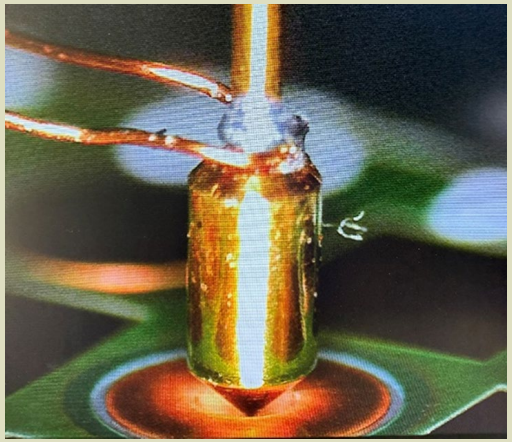




PCB: Mating via with force/sense connection

Measurement Results

Spring Pin in Via Hole



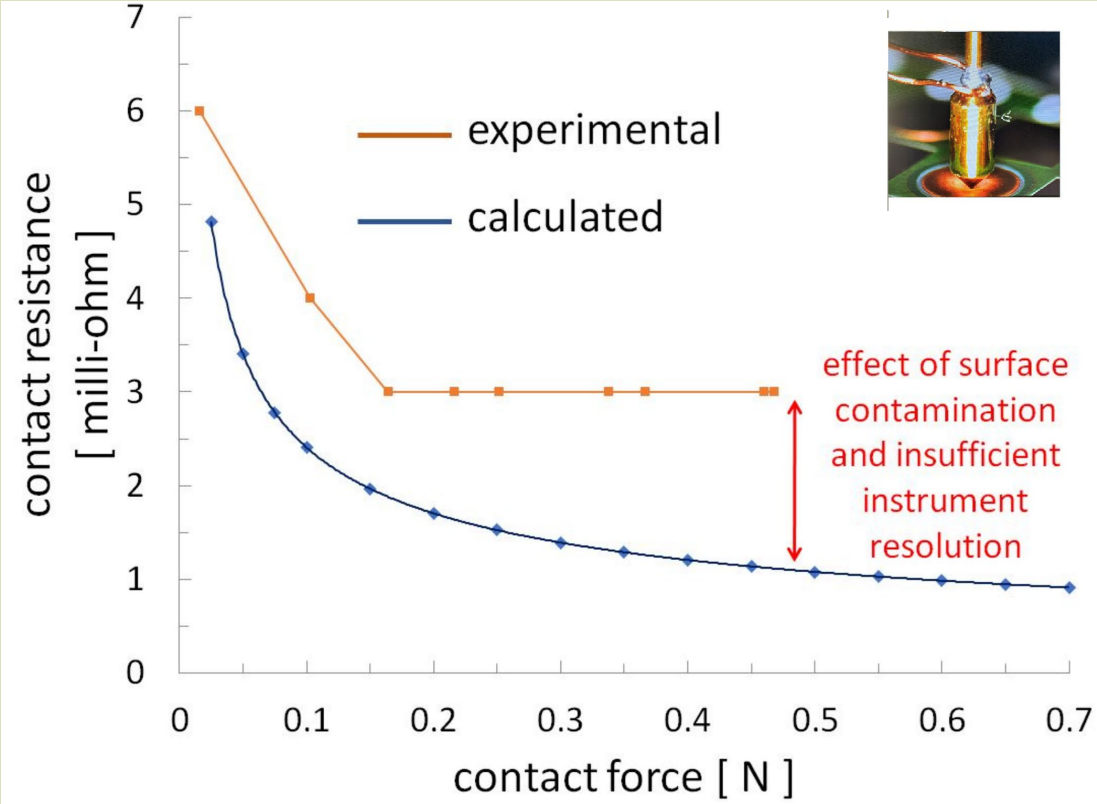
Spring Compression (mm)	Force (N)	Contact Resistance (Ohm)
~0	0.016	0.006
0.25	0.103	0.004
0.5	0.164	0.003
0.75	0.216	0.003
1	0.251	0.003
1.25	0.338	0.003
1.5	0.366	0.003
1.75	0.460	0.003
2	0.468	0.003

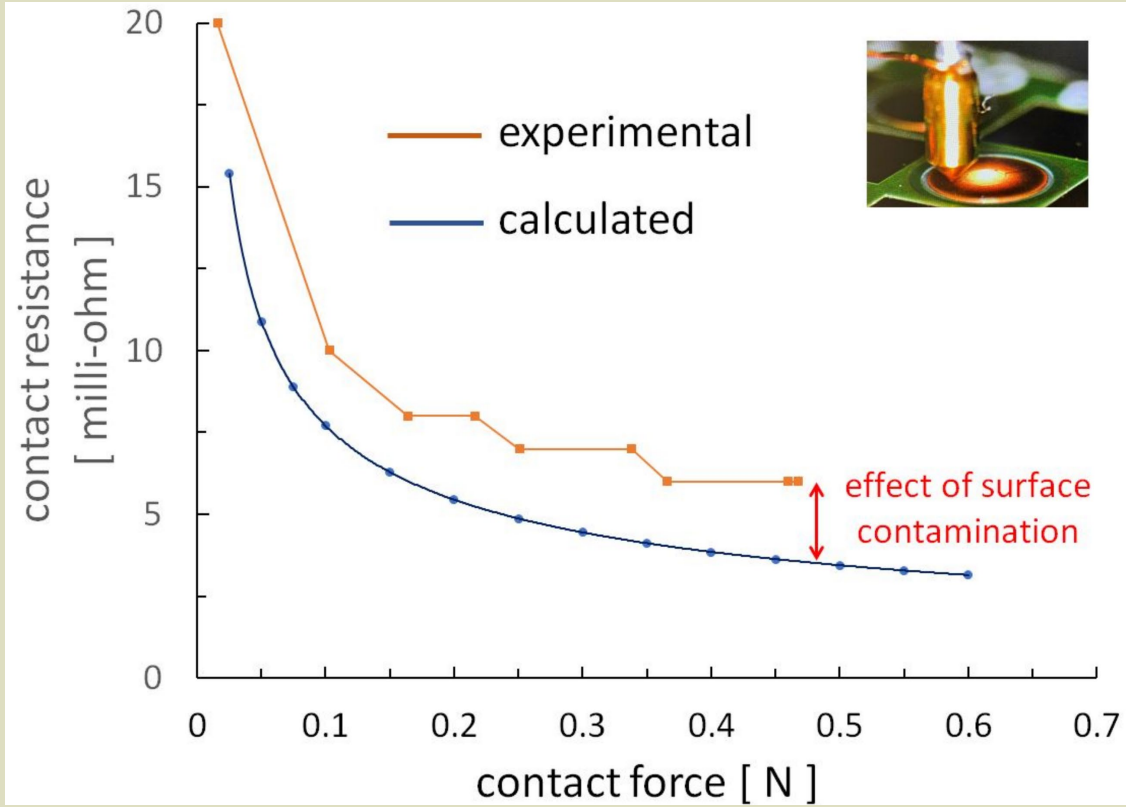
Spring Pin in Via Pad

Spring Compression (mm)	Force (N)	Contact Resistance (Ohm)
~0	0.016	0.02
0.25	0.103	0.01
0.5	0.164	0.008
0.75	0.216	0.008
1	0.251	0.007
1.25	0.338	0.007
1.5	0.366	0.006
1.75	0.460	0.006
2	0.468	0.006

Contact Resistance vs Spring Force

- There is a continuous need from the semiconductor industry for a larger number of spring pin interconnects in an ATE system.
- This creates mechanical challenges due to the total force from all the spring pin interconnects.
- One option is to reduce the spring force but that has consequences on the contact resistance.

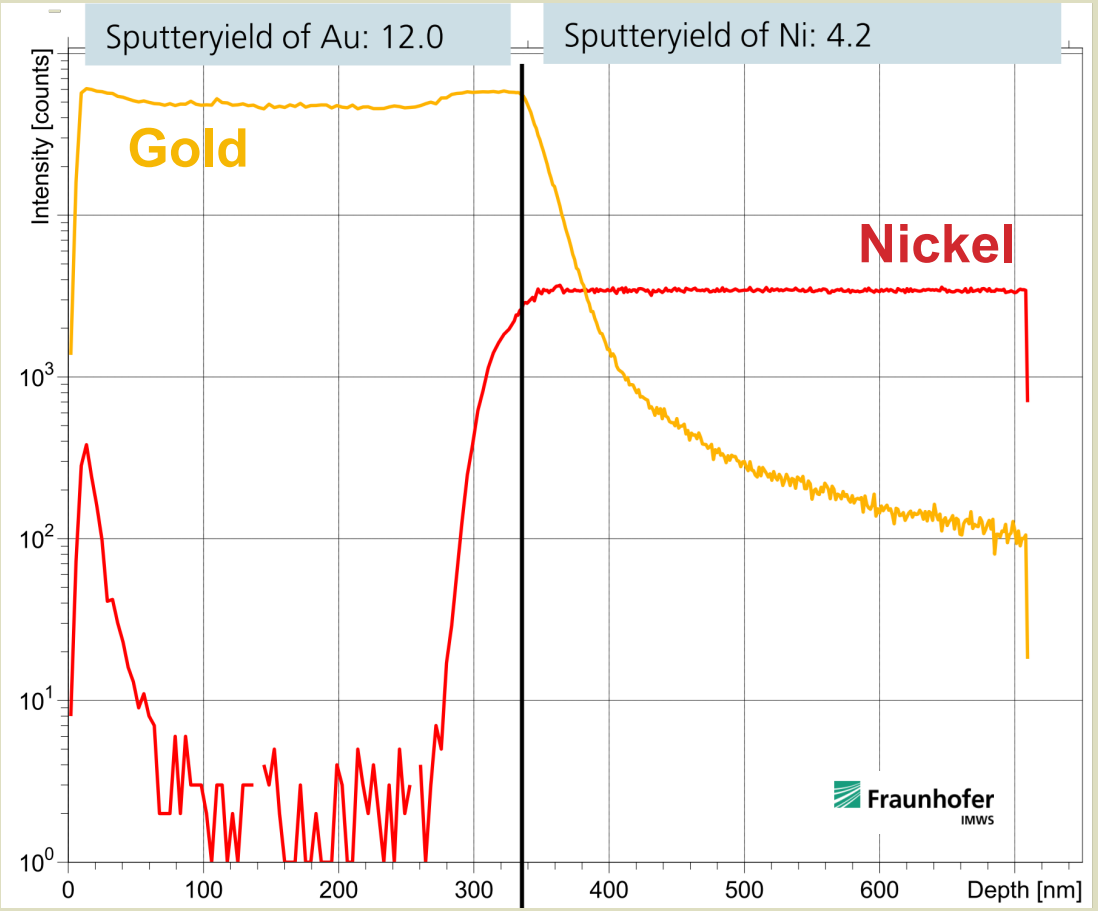




Theory to Measurement Results Differences

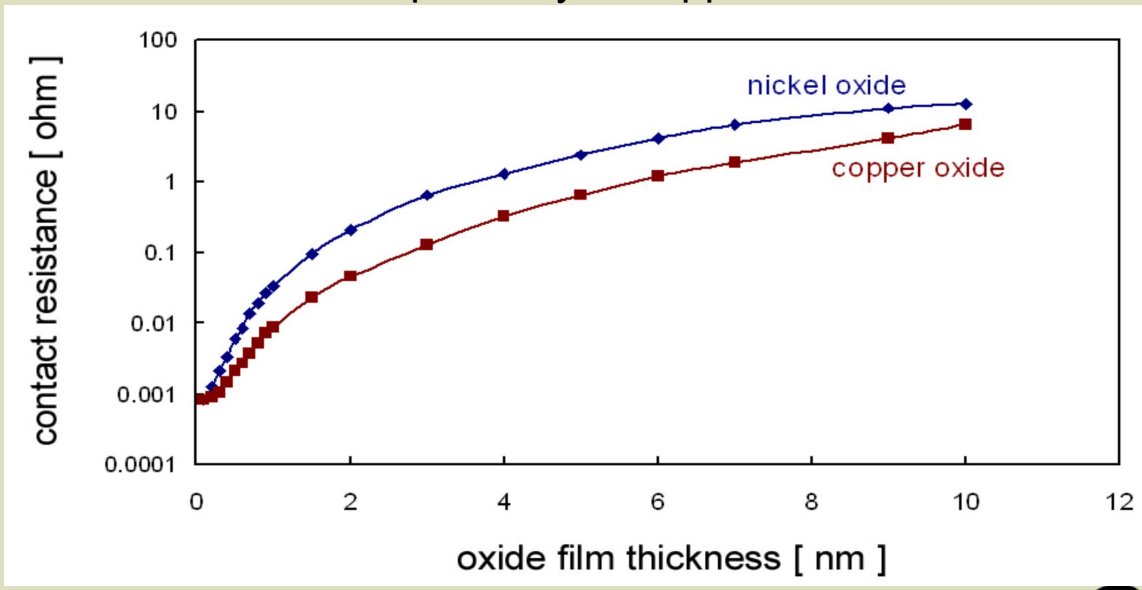
- The ratio of the contact difference between the two configurations correlates well between measurement and the theoretical computation.
- There are several reasons for the difference on the absolute values between the measurement and theoretical computations:
  - Surface contamination.
  - Ni contamination on the Au layer.
  - Measurement setup errors.
  - ***These factors are being quantified.***

Ni Contamination on the Au Layer (PCB Via)

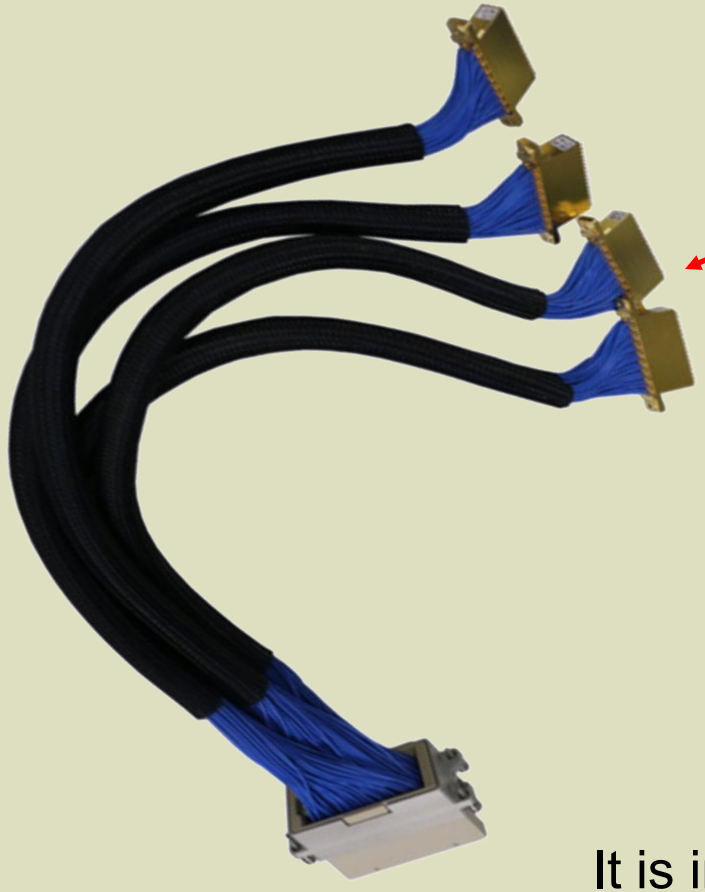


- Depth profile from TOF-SIMS [Time-of-Flight Secondary Ion Mass Spectroscopy] analyses, using positive polarity (2keV).
- Nickel is clearly present in the via plated Au surface increasing the contact resistance.

Contact resistance of a circular contact spot with a radius of 10 µm located at a copper-copper and a nickel-nickel interface but covered with an oxide film respectively of copper oxide and nickel oxide

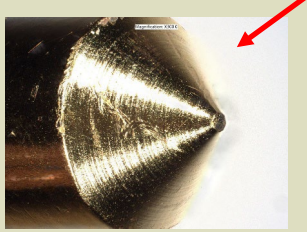


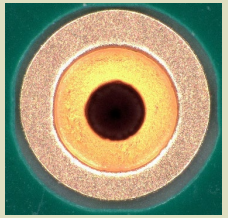
Full Spring Pin Cable Assembly vs Individual Spring Pin Contact Resistance



ATE spring pin cable assembly (~185 mOhm)

Spring pin tip interconnect (3 to 6 mOhm)





It is important to understand spring pin to PCB via contact resistance values in the context of the entire ATE spring pin cable assembly resistance.

Conclusions

- Spring pin interconnects are critical in ATE applications.
- When analyzing any interconnect (like a spring pin) both sides of the interconnect are critical and need to be analyzed together.
- Although the contact resistance of a spring pin tip in via hole configuration is twice of the spring pin tip in via pad configuration, this difference is small in absolute values compared to the total resistance of the ATE spring pin assembly.
- The key challenge for ATE applications is not the absolute value of the total resistance between the ATE measurement instrumentation and the DUT (this is addressed by calibration and 4-wire measurement) but guaranteeing the repeatability of the measurement setup.

Acknowledgements

We would like to thank Junichiro Tanihara, Ayano Tamura, Chihiro Murakami, Toru Hachiya and Masato Urushibara from the Advantest failure analysis lab team in Gunma, Japan and Edin Seferovic from Advantest Germany.

COPYRIGHT NOTICE

www.testconx.org