TWENTY-SEVENTH ANNUAL

TestConX™

Archive

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Mesa, Arizona
March 1-4, 2026

Advancing Final Test Interface Hardware for AI & HPC Devices

Overcoming the Limits of Monolithic PCBs

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DIS Tech

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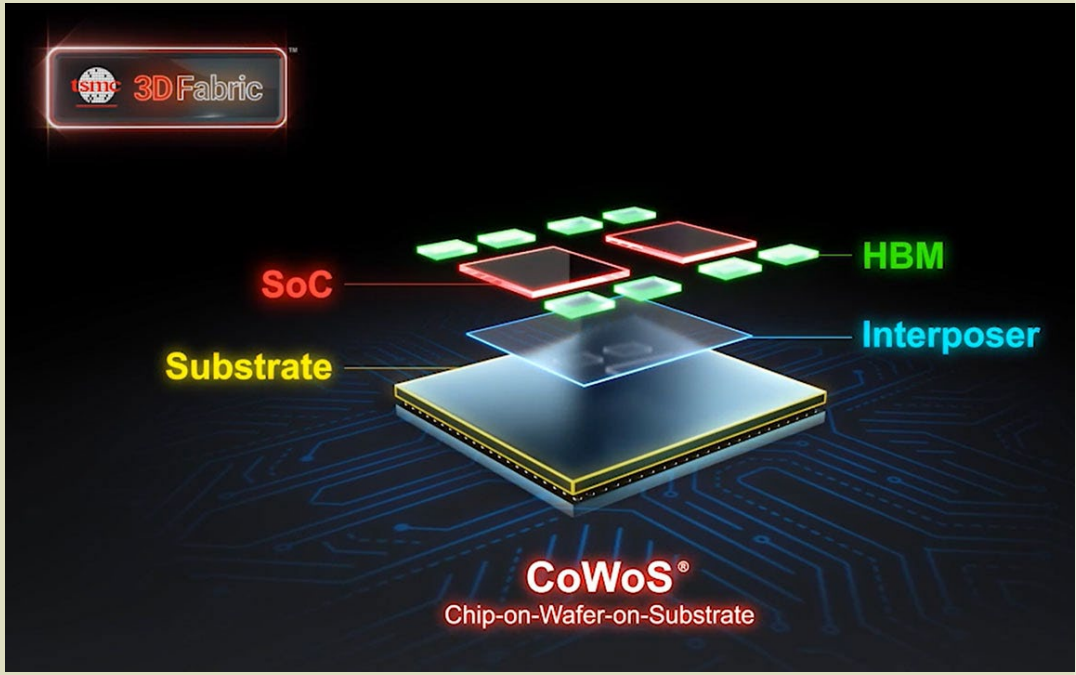
Advanced Packaging Enabling AI & HPC Growth

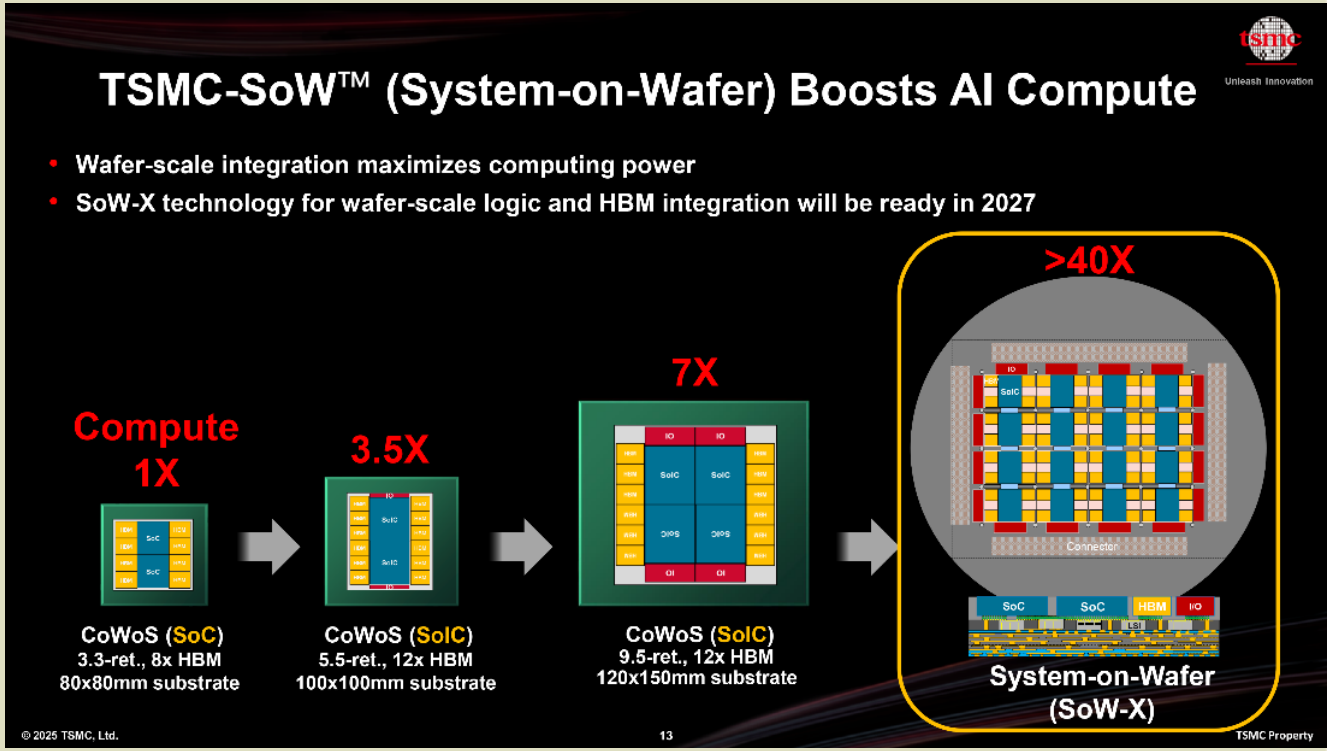
- More SoC + HBM integration in single package
  - AI & HPC devices continue to push the integration limits to accelerate up the performance curve
- Peak current at final test can be 2x – 10x probe
  - >2 KA with today's devices being tested, single-site
  - If a DIB can only deliver 1 KA, need twice as long to test
    - Plus, additional SLT insertion for loopback at speed



Source: https://www.tsmc.com/english/news-events/blog-article-20200803

Advanced Packaging Enabling AI & HPC Growth

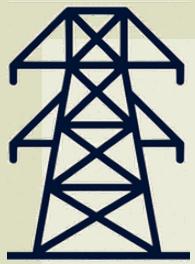
- Market trend is for higher integration and larger solutions
  - 2027 CoWoS substrates growing to support up to ~9x reticle size, vs. ~5x reticle size limit today
    - This will result in 2x increased power demand
  - Moving to CoPoS, CoWoP, SoW advanced packaging options in coming years will drive power density in modules even higher



Source: https://www.techspot.com/news/107695-tsmc-unveils-plans-giant-ai-chips-meet-surging.html

The Growing Test Challenge for AI & HPC

- AI & HPC devices aim to achieve higher performance more efficiently in every generation
  - Leading to lower voltages, higher peak current, smaller pitch

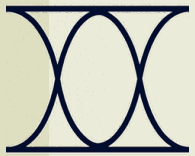


Bulk Power Delivery

- 2,000 A → 6,000 A peak current draw per DUT

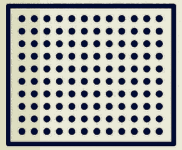
Power Integrity (PI)

- 5 – 20 mΩ impedance needed under full load



Signal Integrity (SI)

- >224 Gbps HSS I/O
- >100 lanes



Pin Density

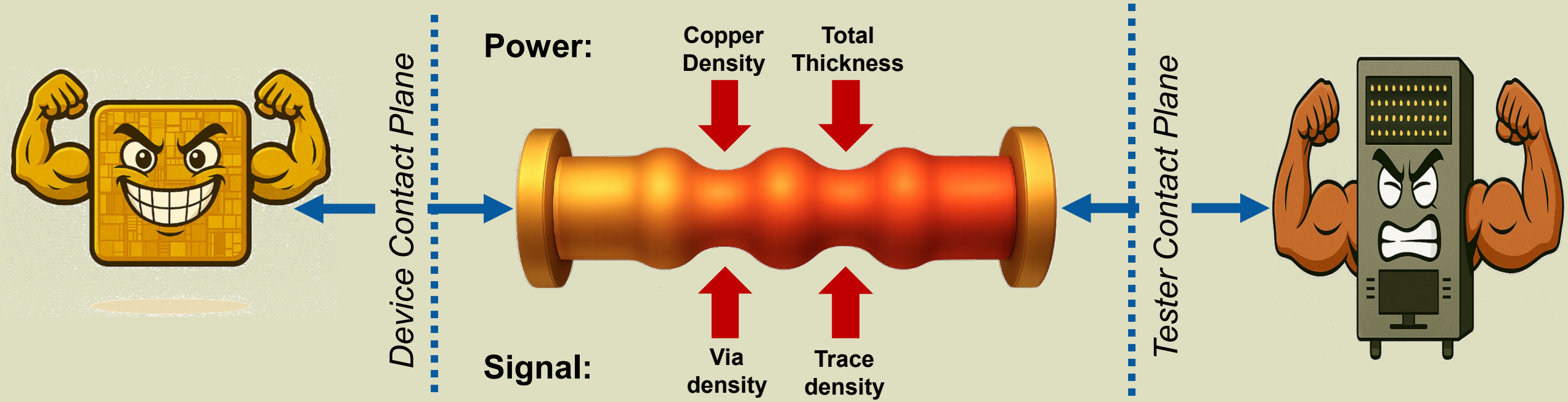
- Tens of thousands of pins per DUT at shrinking pitch

Interface Solutions are a Bottleneck for Testing

Device Capability
AI / HPC Processor

Interface HW Capability
PCB + Substrate

Tester Capability
ATE Instruments

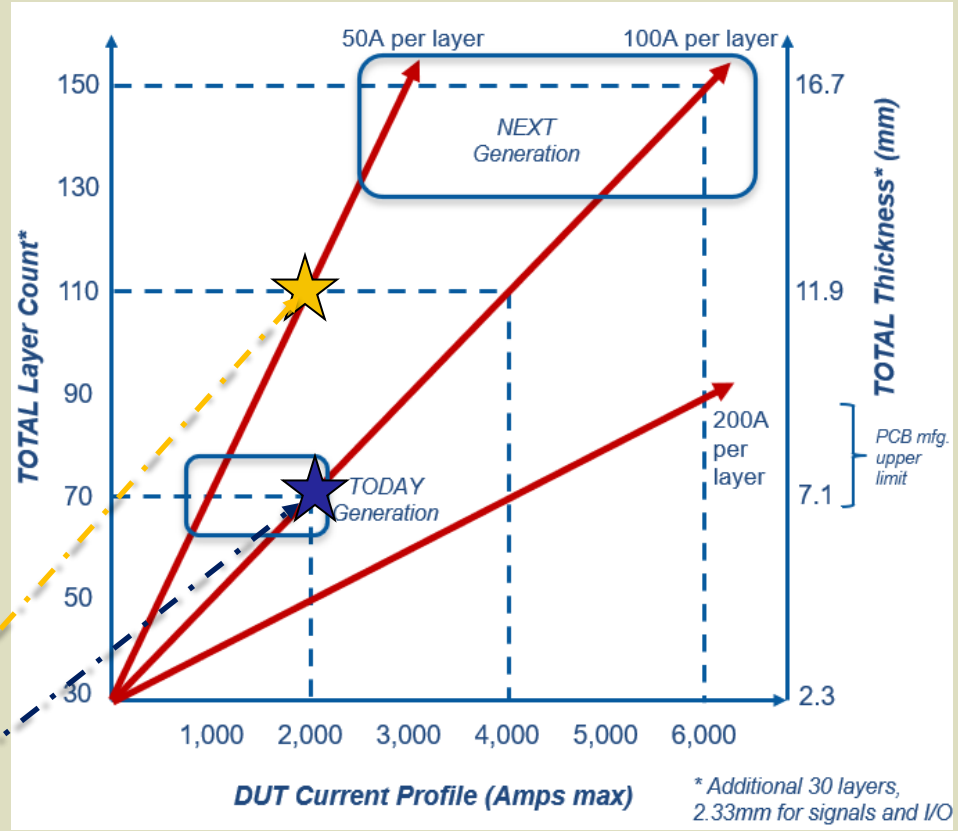


- Devices are demanding & Testers are supporting more power and signal speed than interface solutions can deliver

New PCB Metric for AI & HPC Solutions: “Ampacity”

- Total current a DIB can deliver:
  - CCC per layer * # of PWR+GND layers
- Conflicting factors for CCC per layer:
  - Via density, copper thickness (0.5 - 2.0 oz), trace congestion, backdrilling “swiss cheese” effect on PWR/GND planes
- To achieve Ampacity of 2,000A:

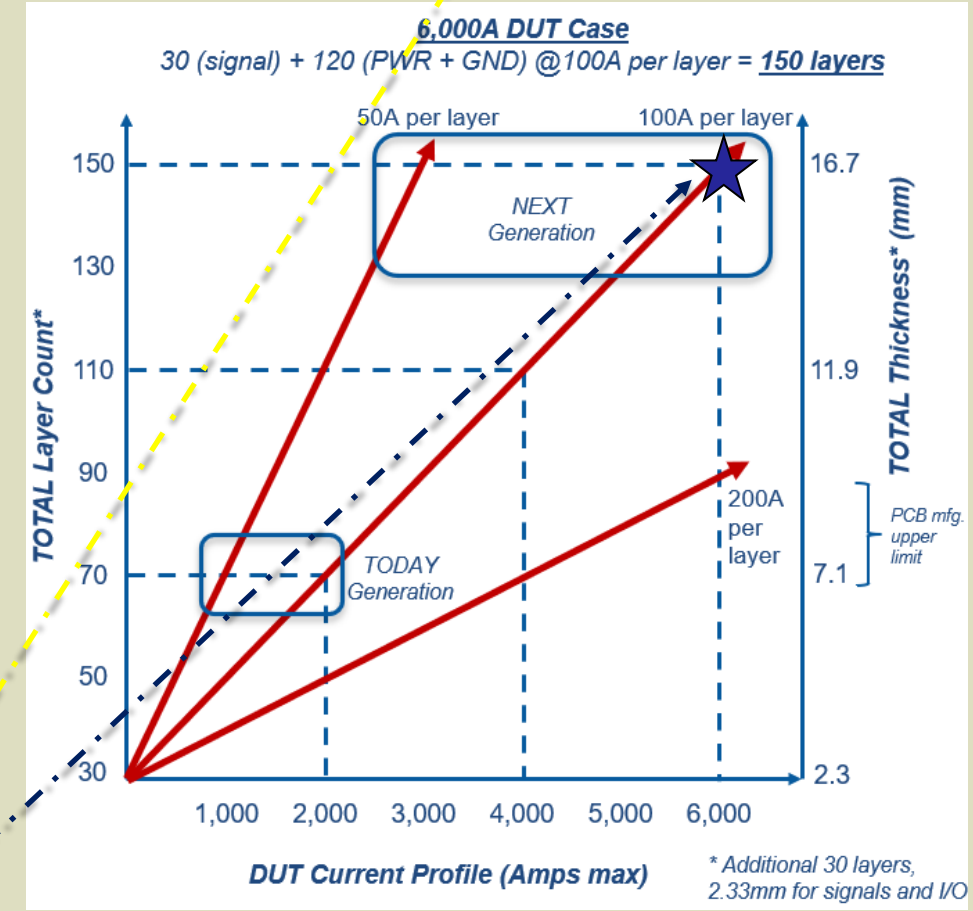
CCC per Layer	# of PWR + GND Layers	# of I/O Layers	Total Layers	PCB Thickness
★ 50A	40 + 40	30	110	11.9 mm
★ 100A	20 + 20	30	70	7.1 mm



>4,000A Requirements Drives New DIB Architectures

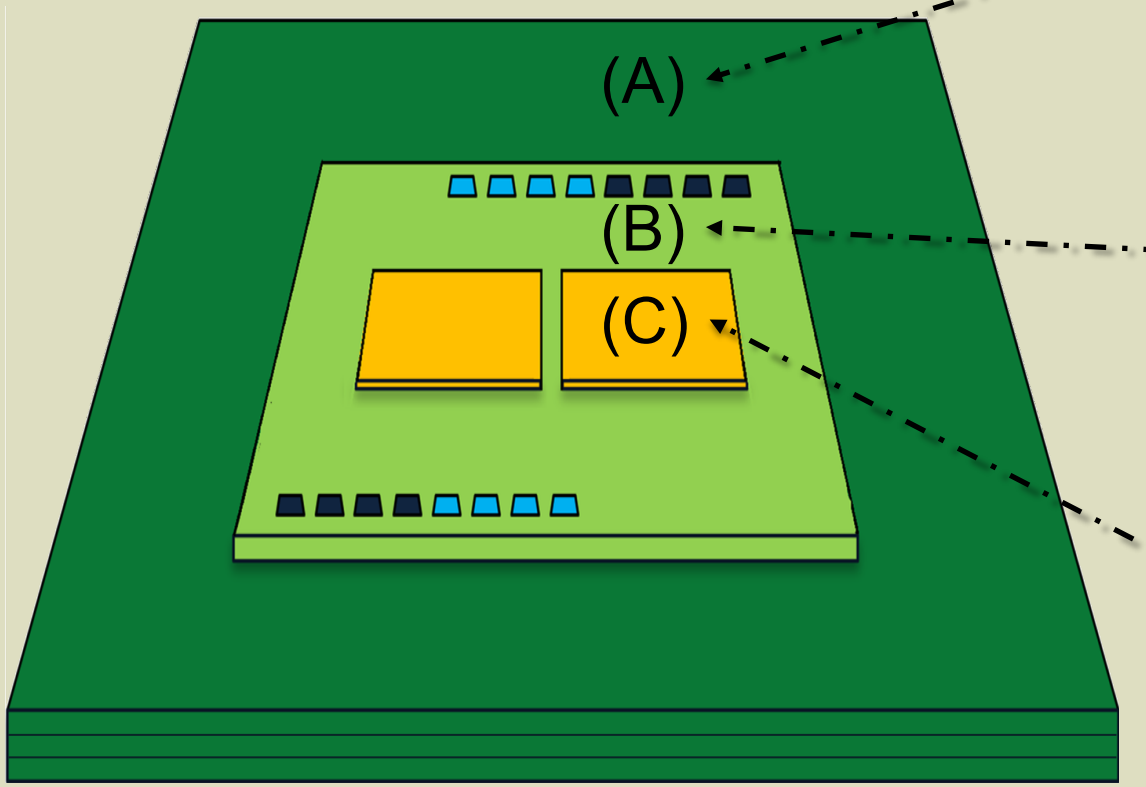
- Monolithic PCB capability is exceeded:
  - >100L of 2oz Cu = 10mm+ thickness & impossible drilling aspect ratios
- To achieve Ampacity of 6,000A:
  - 50A / Layer CCC is not feasible @ 270 layers
  - 100A / Layer results in PCB thickness still well beyond traditional PCB manufacturing capabilities

CCC per Layer	# of PWR + GND Layers	# of I/O Layers	Total Layers	PCB Thickness
50A	120 + 120	30	270	31.1 mm
100A	60 + 60	30	150	16.7 mm



New Approach: Modular DIB Architecture

FUSIONLINK



Motherboard (A)

Optimized for broad connection to the tester

- Bulk power delivery and routing to the DUT area
- Capable of 150+ layers and 30K+ components
- PCB Pitch – down to 300µm

Primary Substrate (B)

Optimized for high performance DUT circuits

- High frequency signal and power integrity
- Any layer connect with stubless routing
- Fine pitch – down to 80µm

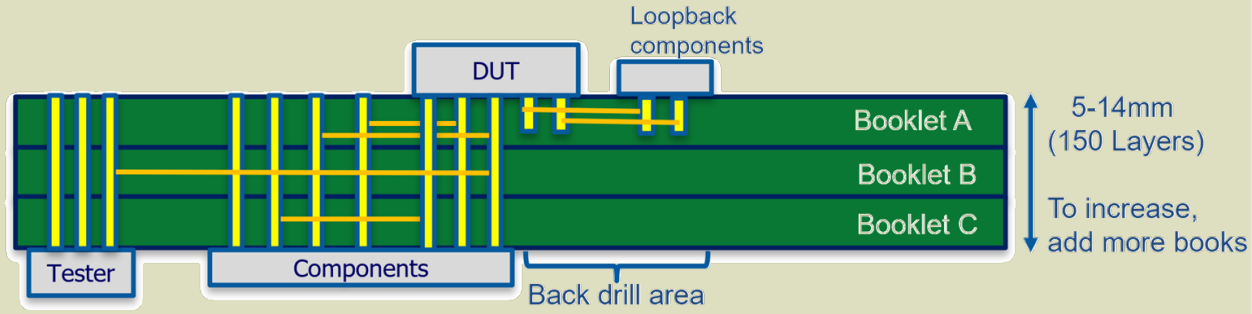
Advanced Substrate (C)

Optimized for probe needle contact

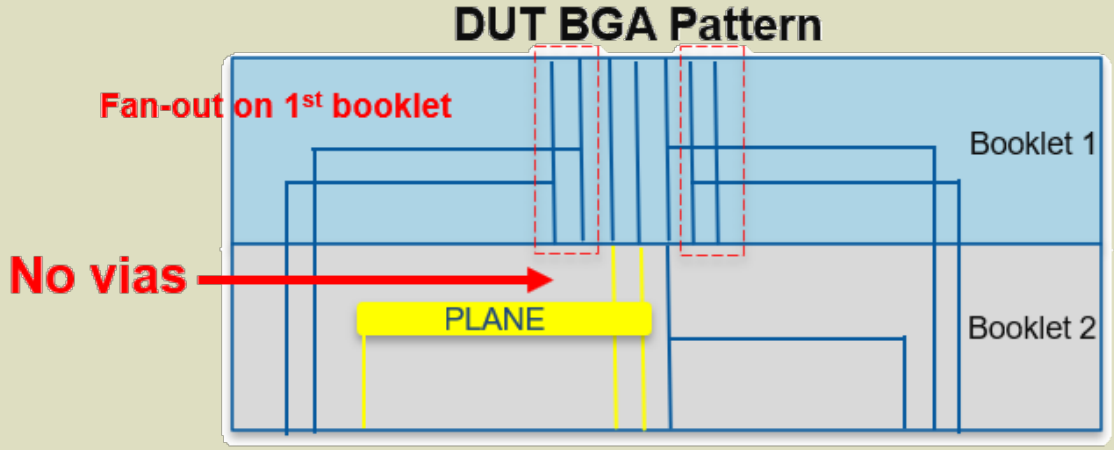
- Proprietary thin film materials and process
- Very fine pitch – down to 40µm, low CTE

Motherboard: Bulk Power Delivery

- Modular “booklet” design:
  - Each containing 30 - 50 layers
  - 150+ layers, 8 - 18 mm thick
    - 2 oz Cu for power, 0.5 oz Cu for I/O

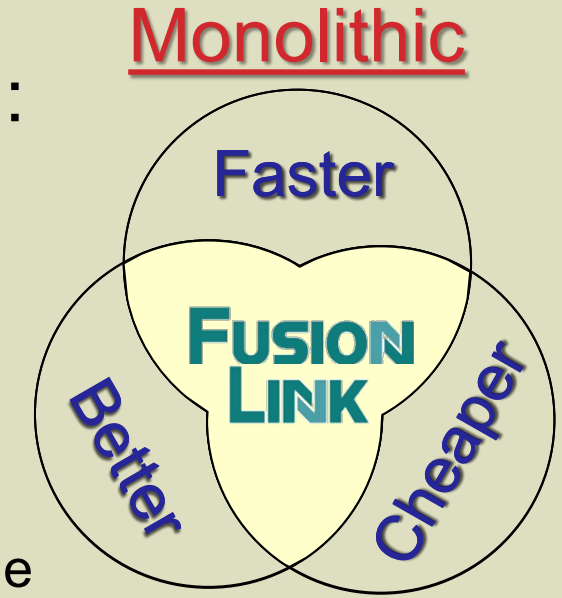


- Denser power planes = better PI
  - Backdrilling isolated to individual booklets eliminates the “swiss cheese” effect on power & ground caused by many vias
    - Maximize CCC per layer



Modular DIB Architecture Benefits vs. Monolithic PCBs

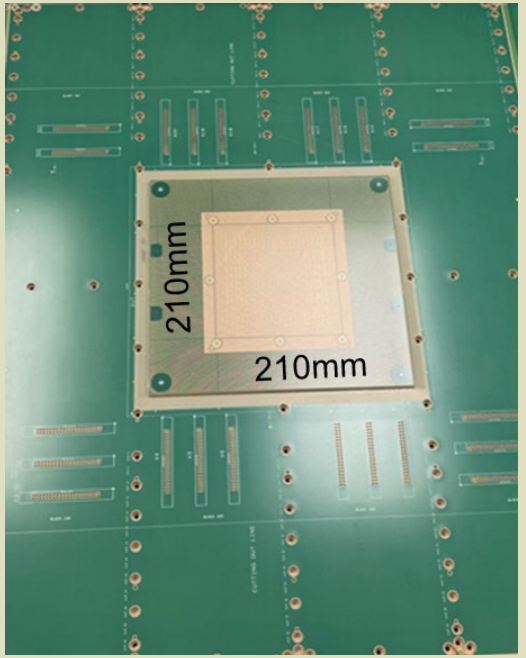
- The benefits of sequential lamination without the pain:
  - **Lead Time**: Faster
    - Build booklets in parallel, combine in a single step
  - **Cost & Yield**: Cheaper
    - Simplified booklet fabrication, smaller aspect ratios
  - **Performance & Reliability**: Better
    - Shorter and fewer stubs on individual booklets, more layers available



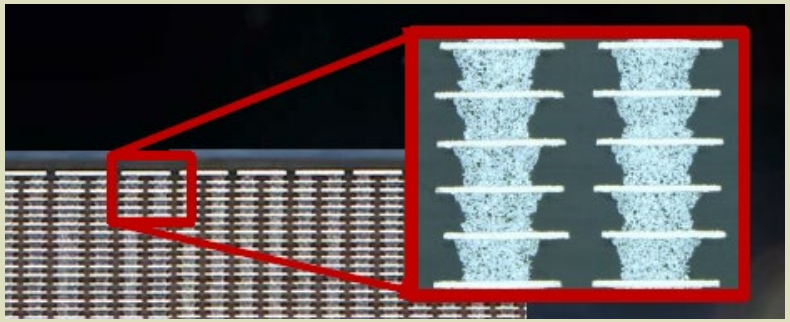
Monolithic PCB Problems	FusionLink Resolution
Drill bit damage from high layer count of 2 oz Cu	Lower aspect ratio drilling in thinner booklets
Long via stubs affecting high-frequency performance	Shorter/fewer stubs due to booklet segmentation
Limited fan-out space for DUTs	More stubless routing options available with multiple booklets
Poor manufacturing yields & cycle times	Simplified booklet fabrication & higher first-pass success rates

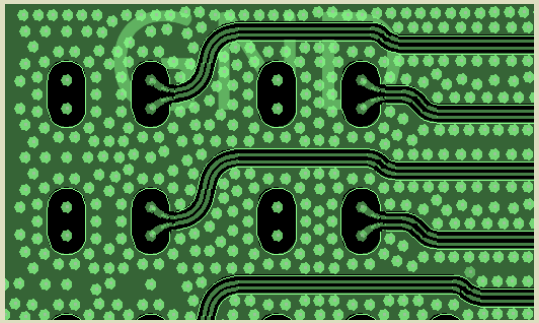
Primary Substrate: High-Speed Signal Integrity

- Up to 60 layers and 300mm size
  - Able to rotate gerbers during fabrication
    - Eliminates high-frequency “glass weave” effect on SI performance
  - Use materials optimized for high speed I/O



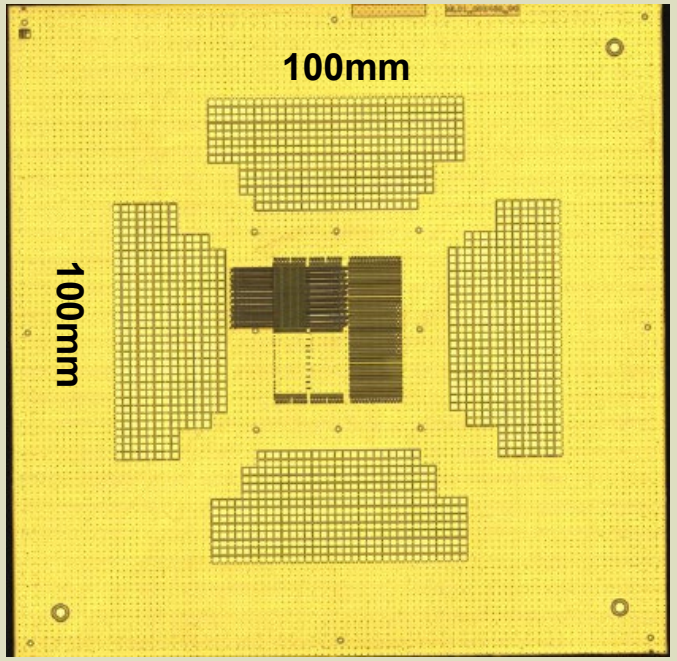
- Any-Layer Connect construction
  - Stubless routing
  - Dense GND stitching
  - Precise line width control

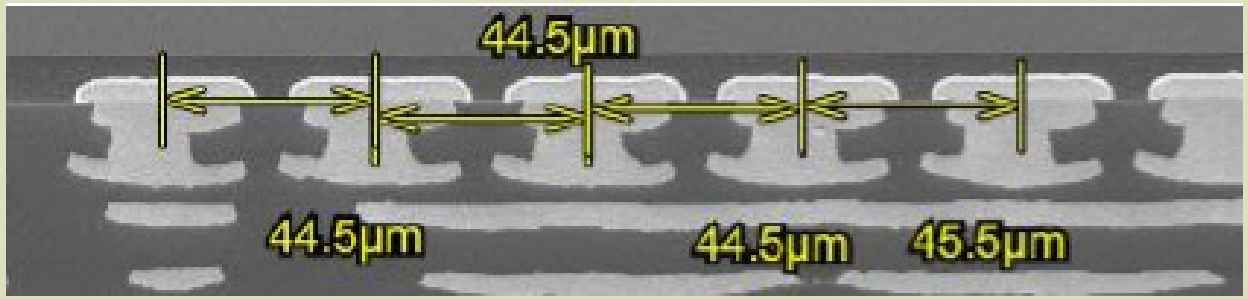




Advanced Substrate: Ultrafine-Pitch Contact & Routing

- Semiconductor fabrication process
  - Up to 20 layers & 100mm size
- Any-Layer Connect construction
  - Optimized socket/device fan-out with precise line width control for high-frequency SI performance
- 40µm pad pitch capability
  - Down to 5µm L/S for dense I/O routing





Advanced Substrate Benefits vs. Monolithic PCBs

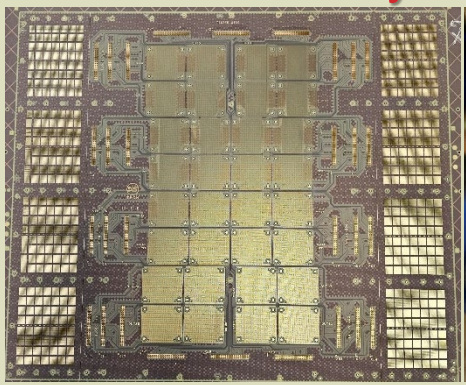
- Fine-pitch application area is self-contained on substrates
  - Fan-out of DUT area accomplished without impacting PCB stack-up
  - Allows for PCB pitch requirement and distance from center to remain manageable
  - Application circuit able to be located closer to the DUT
  - High-cost materials for high-speed limited to smaller substrates
  - Tiling of multiple substrates possible and ensures site-to-site matching

Traditional Substrate Problems	FusionLink Resolution
Stubs affecting high-frequency performance	Any-Layer Connect for stubless manufacturing
Size and pitch requirements in a single substrate are difficult to yield	Using larger base substrate and smaller ultra-fine-pitch contact advanced substrate improves yield & performance
Long lead time for high layer count	Parallel manufacturing of simpler tiers that can be stacked

Real World Results

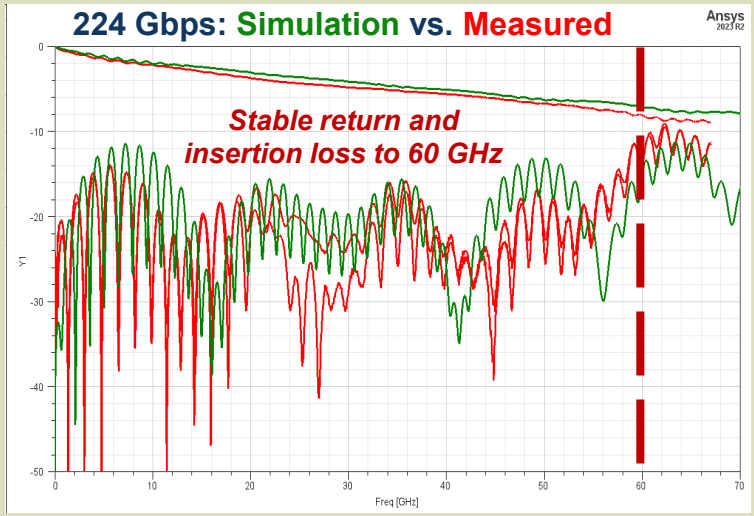
- Power Delivery: >2 KA solutions delivered in 120+ layers
  - ex) 84L Motherboard + 30L Substrate + 20L Advanced Substrate
- Manufacturability: Able to consistently yield previously “impossible” stack-ups
  - Predictable yields result in on-time-delivery
  - Consistent delivery able to scale to high volume
- Signal Integrity: Stable return/insertion loss to 60GHz, 224 Gbps, 500+ lanes
  - >15% wider eye openings on loopbacks with no stubs vs previous monolithic solution
  - Customer able to perform external loopback at speed and with minimal cross-talk

152-Layer PCB



34.4 lbs (15.6 Kg) in-panel
26 lbs (11.8 Kg) out of panel

0.616” thick
(15.6mm)



Conclusion & Outlook

- Breaking away from traditional monolithic DIBs will allow measurable improvements in:
  - Power Delivery
  - Power & Signal Integrity
  - Manufacturability

- What the future holds:
  - Interface HW solutions able to meet the growing demands of AI & HPC
  - Fully-functional DIBs able to be delivered in volume on-time & on-budget

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