TWENTY-SEVENTH ANNUAL

TestConX™

Archive

DoubleTree by Hilton
Mesa, Arizona
March 1-4, 2026

Turning Disruption into Advantage
A Socket Supplier's Perspective

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Mesa, Arizona • March 1-4, 2026

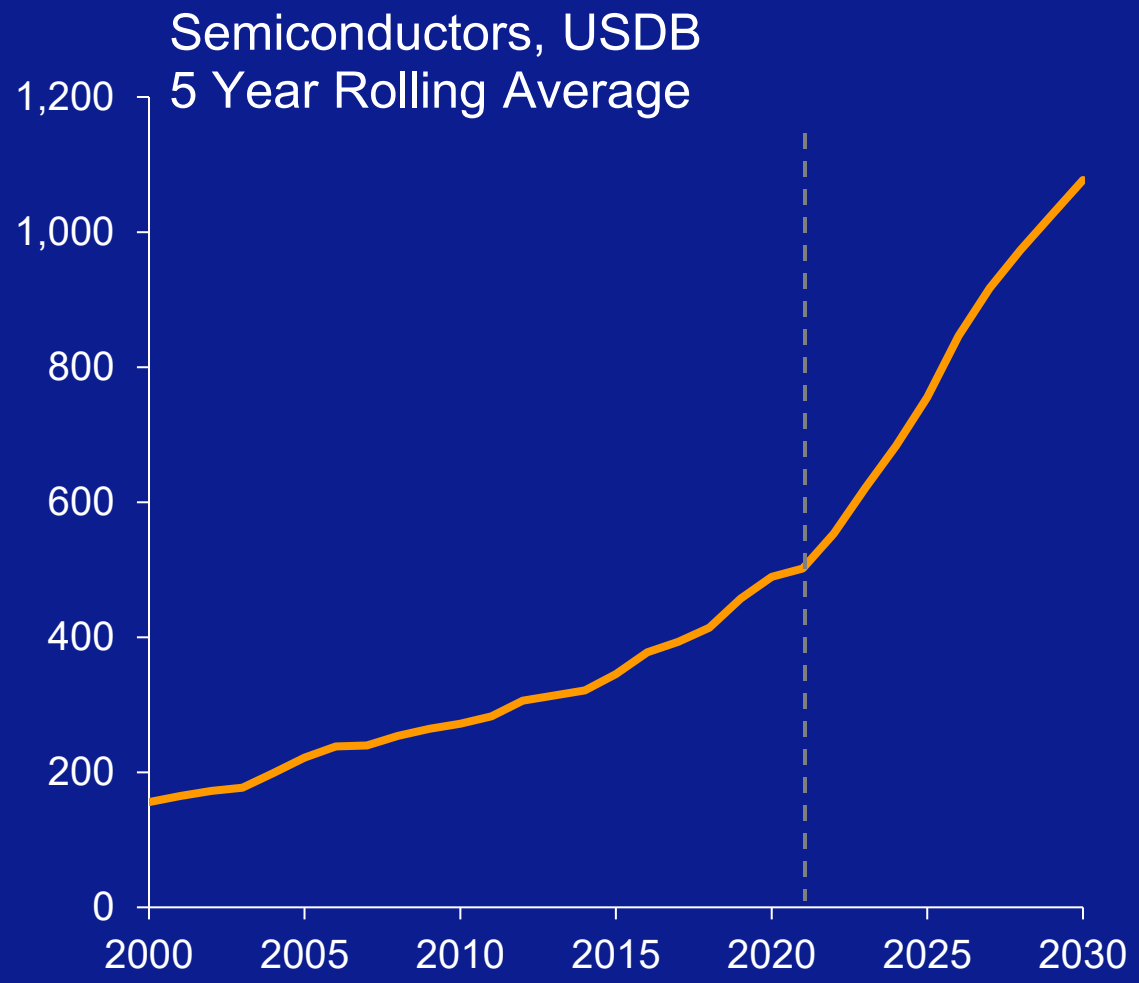
Disruptive forces driving new market landscapes

The rise of the fabless chipmakers

Innovations in Advanced Packaging

Geopolitics

High performance packaging is enabling the AI revolution



Point of inflection in 2021-2022 coincides with the ramp up of AI related chips

There are 2 markets currently in play:

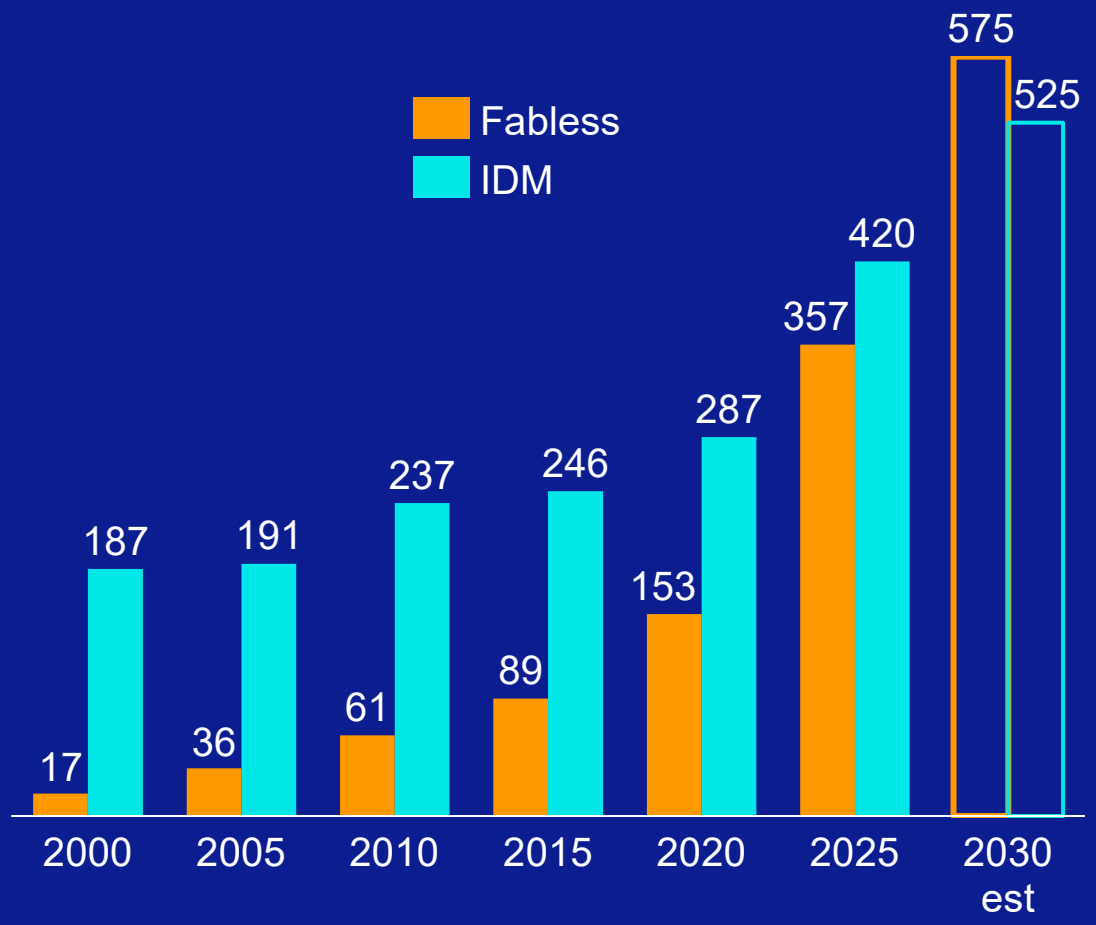
- AI related chips….
- …and there's everything else.

This new wave of growth is a "high performance package" story

Who's making all the money, and what are they doing with it?

Fabless chipmakers on track to overtake IDMs

Semiconductor Revenues by Supplier Type, USDB



Long-term growth rates 2025 - 2030:

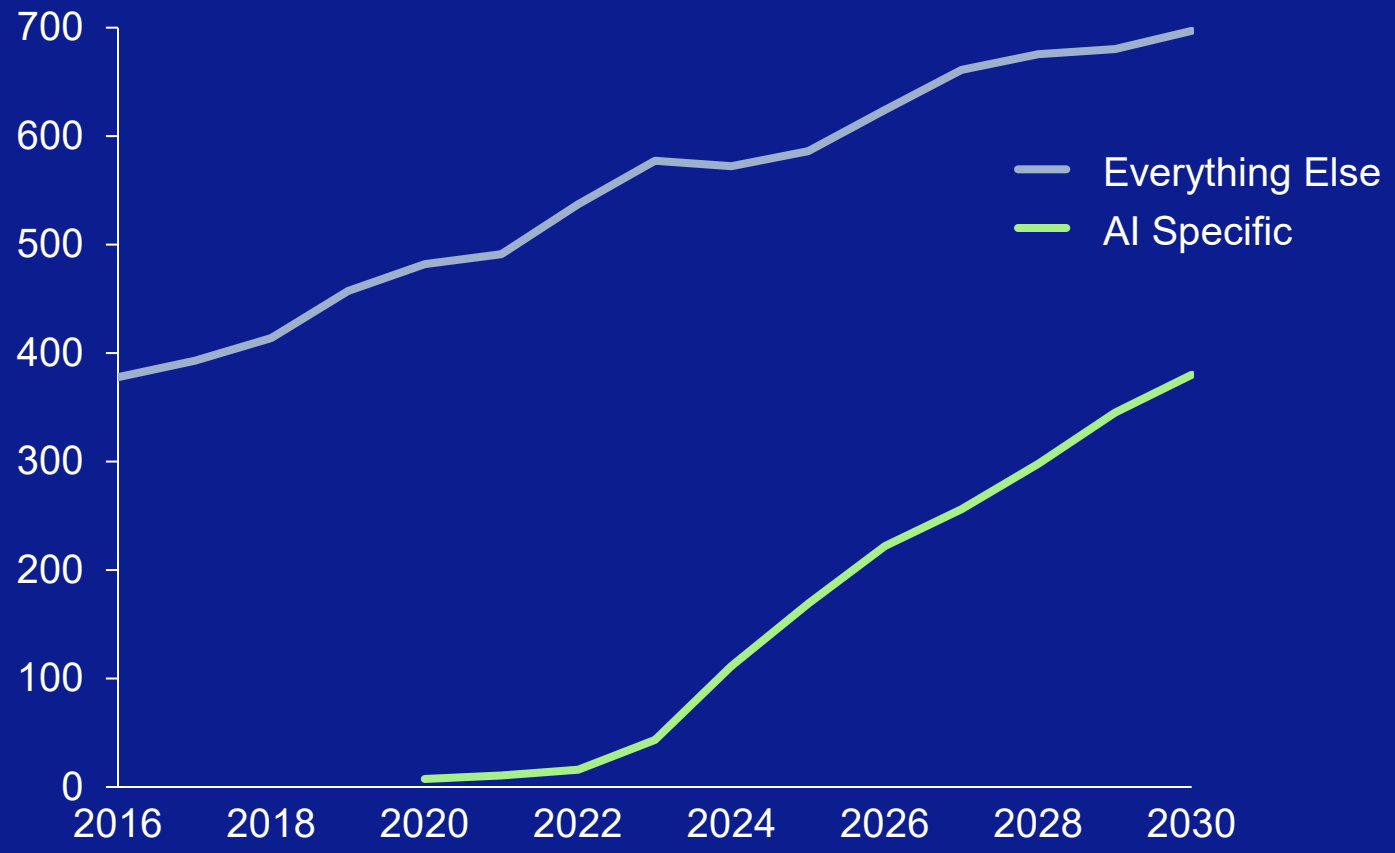
- Fabless 10.0%
- IDM 4.6%
- Total 7.2%

The fabless/foundry business model is beating the Integrated Device Manufacturer (IDM) model.

Going forward, chip designers and their foundry partners will be the ones shaping the direction of the industry

There are AI specific chips, and then there's everything else

Semiconductor Revenues, USDB



Long-term growth rates 2025 - 2030:

- AI Specific 10.0%
- Everything Else 4.6%

AI specific chips currently generate around 22% of semiconductor industry revenues

But account for over 40% of total Capital Expenditures and over 50% of the test and burn-in socket market

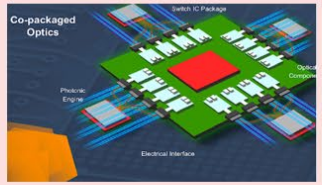
Introduction of EUV and the evolution of high-performance packaging are the key technology enablers for the AI boom

Advanced packaging creates value for high compute applications

Data center networking

Server – Cloud Computing

Switches – HPC



Co-packaged Optics

High-Performance Computing

Workstations

AI-powered Content

High-Performing Desktop/Laptop

Big-data AR/VR

Autonomous Vehicles

AI-enabled Passenger Cars

Robotaxi

Autonomous Driving

Packaging Families

ARCHITECTURE	Traditional Packaging	ADVANCED PACKAGING			
SUBSTRATE TYPE	WIRE BOND	FLIP CHIP	EMBEDDED DIE	2.5 D	3D	EMERGING
IC Substrate (Organic)	WB CSP WB BGA	FC BGA FC CSP FC SiP Metal Shielding Fan-Out on Substrate	Embedded Si Bridge Embedded Si Bridge + Si Interposers Embedded Die / Passives FOPLP Embedded Si Bridge in mold compound or RDL	Si Interposers	3DS TSV HBM TSV NAND TSV CBA DRAM Cu-Cu Hybrid Bonding – DoW	Hybrid Bonding - SoC on interposer Embedded Multi-Die / Passives Co-Packaged Optics
	BOC					
No Substrate	COB	Fan-Out PoP Fan-Out Fan-In (WLCSP)			Cu-Cu Hybrid Bonding – WoW TSV, after bonding – WoW	Hybrid Bonding - SoC in Fan-Out
Ceramic Substrate	LTCC HTCC					
Lead frame Substrate	DIP SOT/TSOP QFN QFP, LCC etc	FC QFN				

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High Performance Packaging

High-performance packaging – challenges and requirements

Challenge:
Integrate more chips

Requirements:
- Larger package size
- Larger interposer

Challenge:
Large interposer

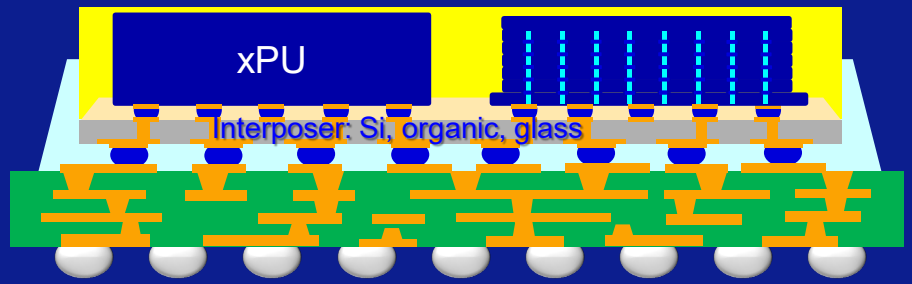
Requirements:
- Control warpage
- Higher reticle size of lithography process
- Adoption of glass material

Challenge:
Dense interconnections

Requirements:
- Low pitch and fine line & space interconnections
- Low parasitic and good signal integrity
- Embedded die option

Challenge:
Higher cost for more integration

Requirements:
- Low cost control
- Higher yield



Challenge:
IC substrate density

Requirements:
- Higher density IC substrate
- Smaller L/S
- More layers
- Larger substrate size – use glass core

Challenge:
Thermal management

Requirements:
- Control CTE of materials to reduce the package stress
- Control head generated due to more integration and during process steps
- High-performance Thermal Insulating Material (TIM) and package heat spreaders

Challenge:
Signal Integrity and high-speed performance

Requirements:
- More HBM stacking – with hybrid bonding
- Shorter interconnects
- Use optical interconnects

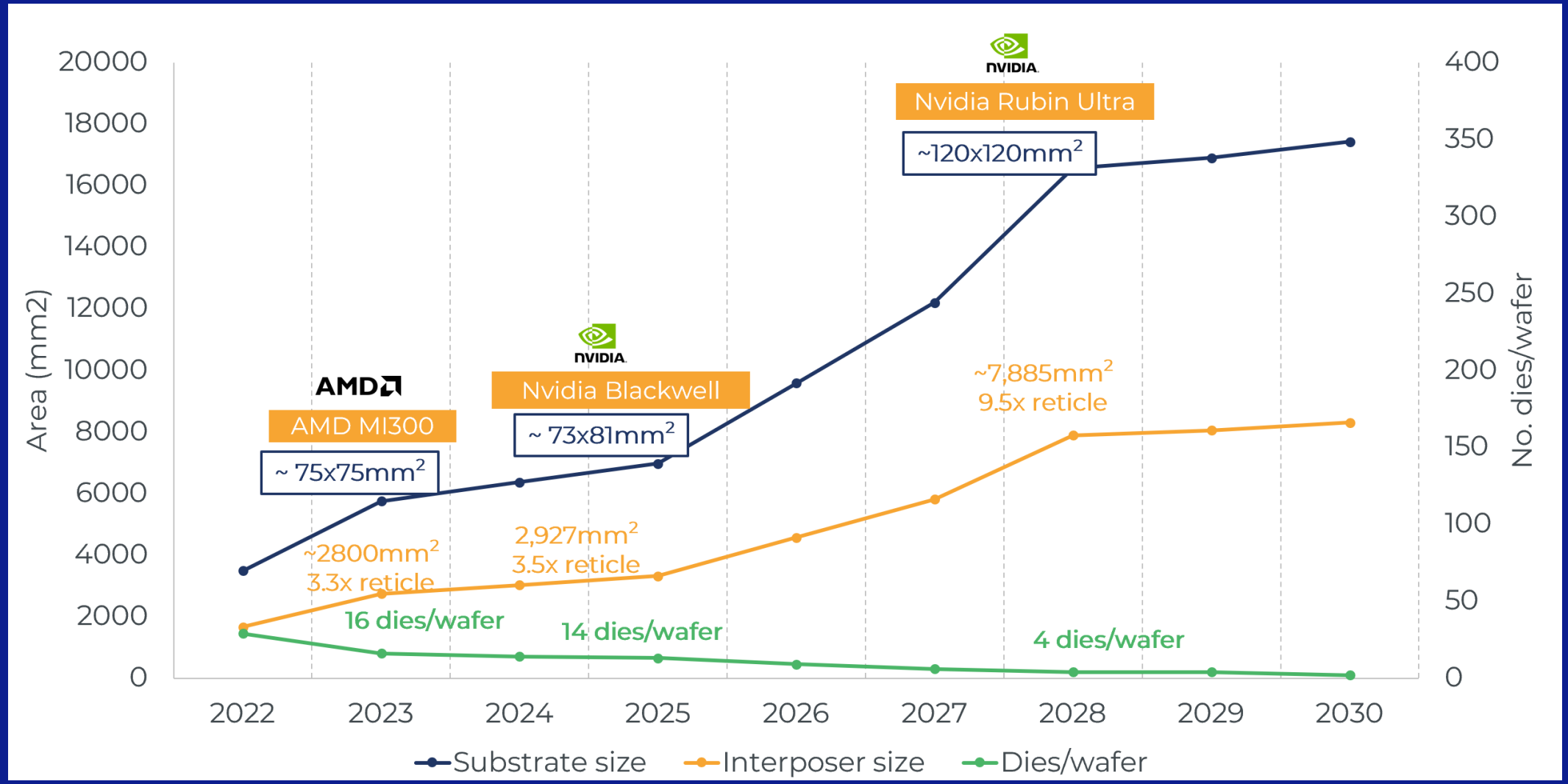
Challenge:
Power Delivery

Requirements:
- Integrate IVR, decoupling capacitor
- Back-side power delivery

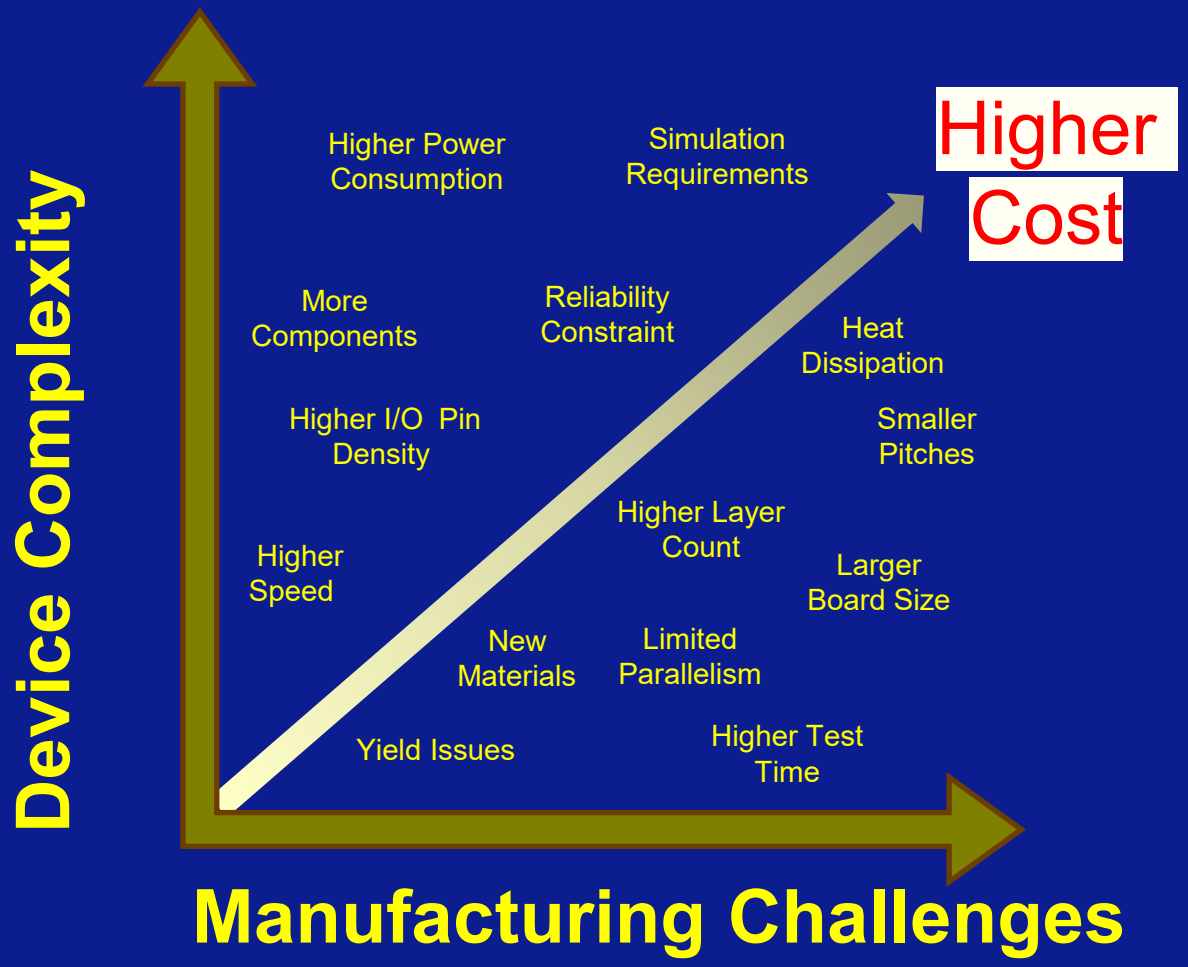
Key packaging technology trends

	Current	Future
Chiplet and HI	• Chiplet in PC/ server processor • HI in SiP, memory, processor, sensor, etc.	• Chiplet in mobile, consumer, automotive & other industry • More HI adoption in all market
2.5D Interposer	• Si Interposer • Organic Interposer (with RDL and bridge)	• More organic interposer; glass interposer • Photonic IC (PIC) interposer • Larger interposer to integrate more chips
2.5D Bridge	• Interconnect with C2/C4 or FO-RDL • Bridge with and without TSV	• Interconnect with Hybrid bond • More bridge with TSV
PLP	• Used for low-end FO/FI or high-density FO • More for small package size (<15mmx15mm)	• Adopt for 2.5D interposer • For large package size (> 50mm x 50mm) • Other packaging application, e.g., power module
3.0D Stacking	• W2W – Memory stacking, CIS • D2W –memory/IO + logic, face to back	• W2W- memory + logic • D2W – logic on logic, face to back and face to face
CPO Packaging	• OE and ASIC on different substrate • PIC and EIC side-by-side	• OE and ASIC on same substrate • Stack PIC and EIC
IC Substrate	• Organic Core Substrate • Substrate size ≤ 120mm x 120mm	• Glass Core Substrate • Substrate size >120mmx120mm

Advanced packaging moving towards larger package sizes



Device Complexity Drives Manufacturing Challenges and Higher Costs



Test solutions are available for most package types …

… but at what cost?

How motivated are test equipment and test consumables suppliers to develop new cost-effective solutions?

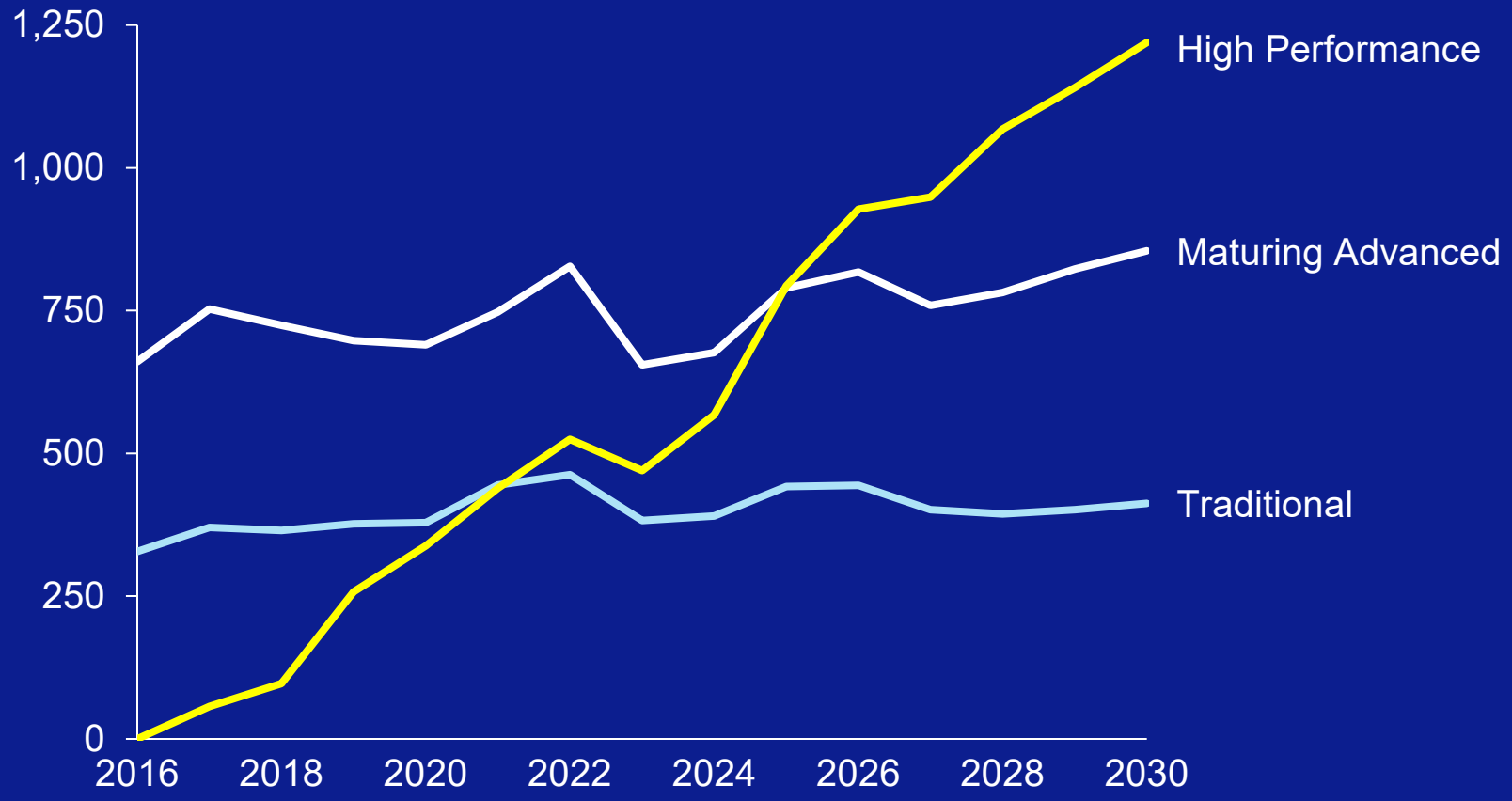
Should suppliers create their own intellectual property or co-develop with customers or partners?

What is the role of smaller test and burn-in socket suppliers?

What do these new test solutions look like?

High-performance packaging drives socket demand

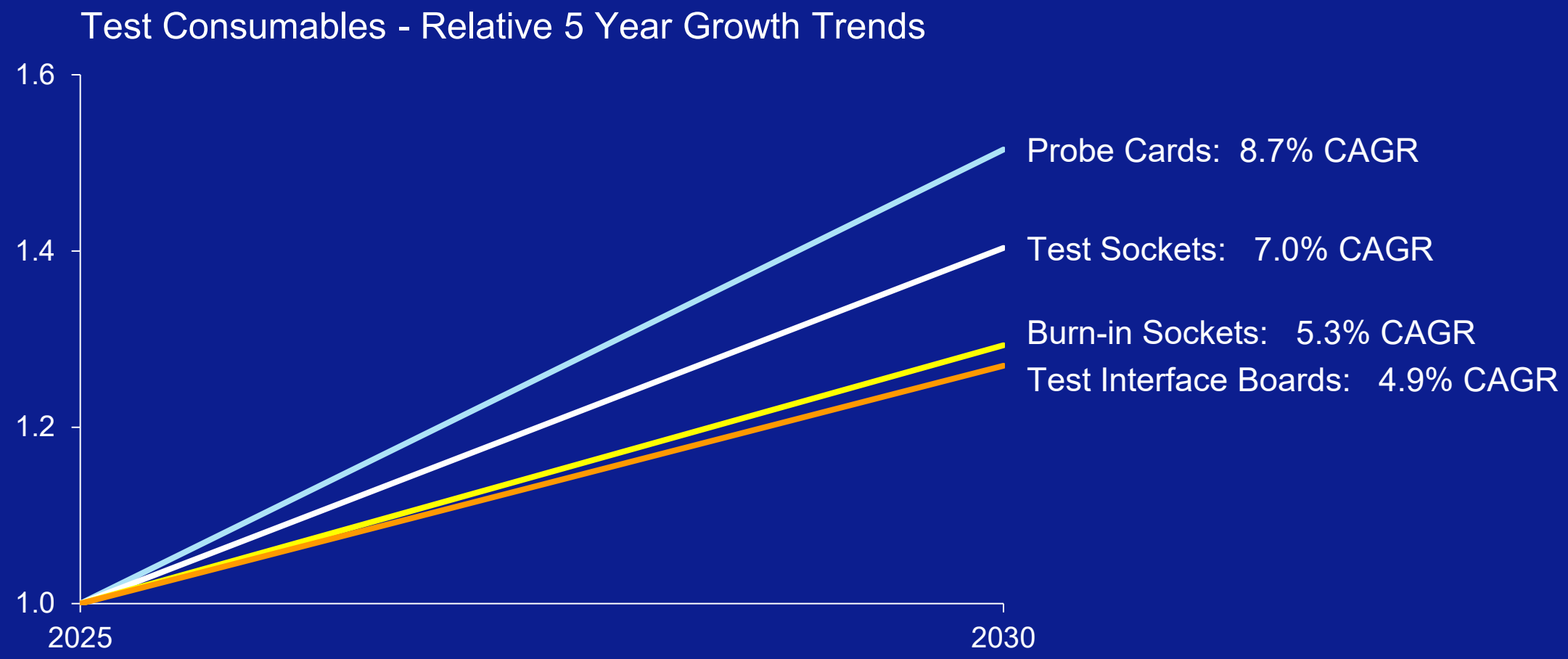
Test and Burn-in Socket Revenues by Package Family, USDM



Long-term growth rates 2025 - 2030:

- High-performance 9.0%
- Maturing Advanced 1.6%
- Traditional -1.2%

Wafer sort and system level test driving growth for test consumables



The semiconductor industry is now highly subsidised

Historically, for every $1 net profit made, chipmakers with manufacturing assets spent $1 on capital expenditure

From 2020 to 2025, the industry overspent by more than $300Bn on CapEx

This gap has been funded by:

- Cash
- Higher Debt
- Sale of Assets
- Equity Investors
- Government Subsidy

Government subsidy is estimated to represent more than 20% of capital expenditure over the past 6 years

What happens when the subsidies stop?

Final Thoughts

Fabless chipmakers, new advanced packaging technologies, and government intervention will have major impacts on the industry over the next five years

From a test and burn-in socket suppliers' perspective, these disruptors are "positive", and will lead to strong growth prospects.

Taking full advantage of these changes requires staying well informed and responding fast.

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