

TWENTY-SEVENTH ANNUAL



TestConX™

Archive

DoubleTree by Hilton
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Power Supply Sequencing and Monitoring

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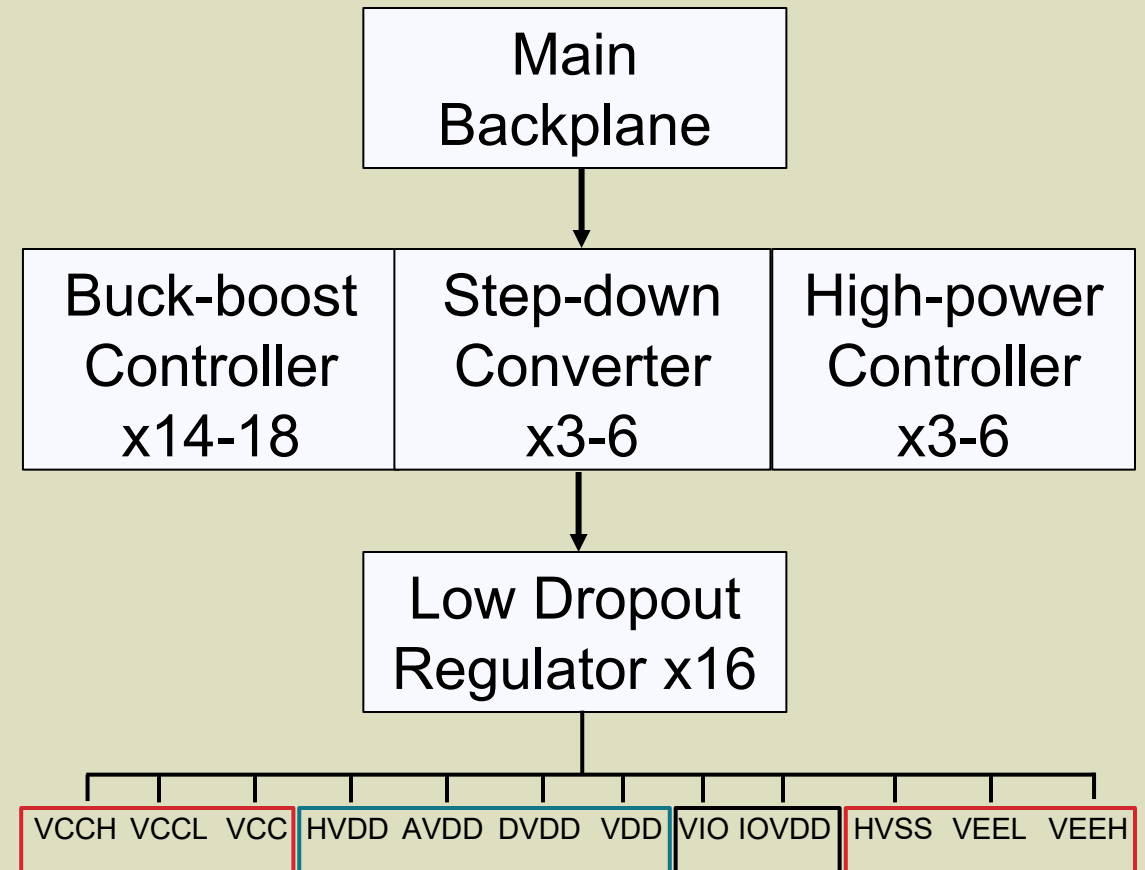
- Background
 - Review of 3 typical power trees for test equipment
 - Oscilloscope, source measurement unit (SMU), parametric measurement unit (PMU)
 - Summary of power supply types in test equipment development
- System specifications
 - Explain complexity of challenge (up/down) + error events
- Existing solutions and challenges
- Evaluation
 - Proposed solution experiment
 - Result

PMU Power Tree Example

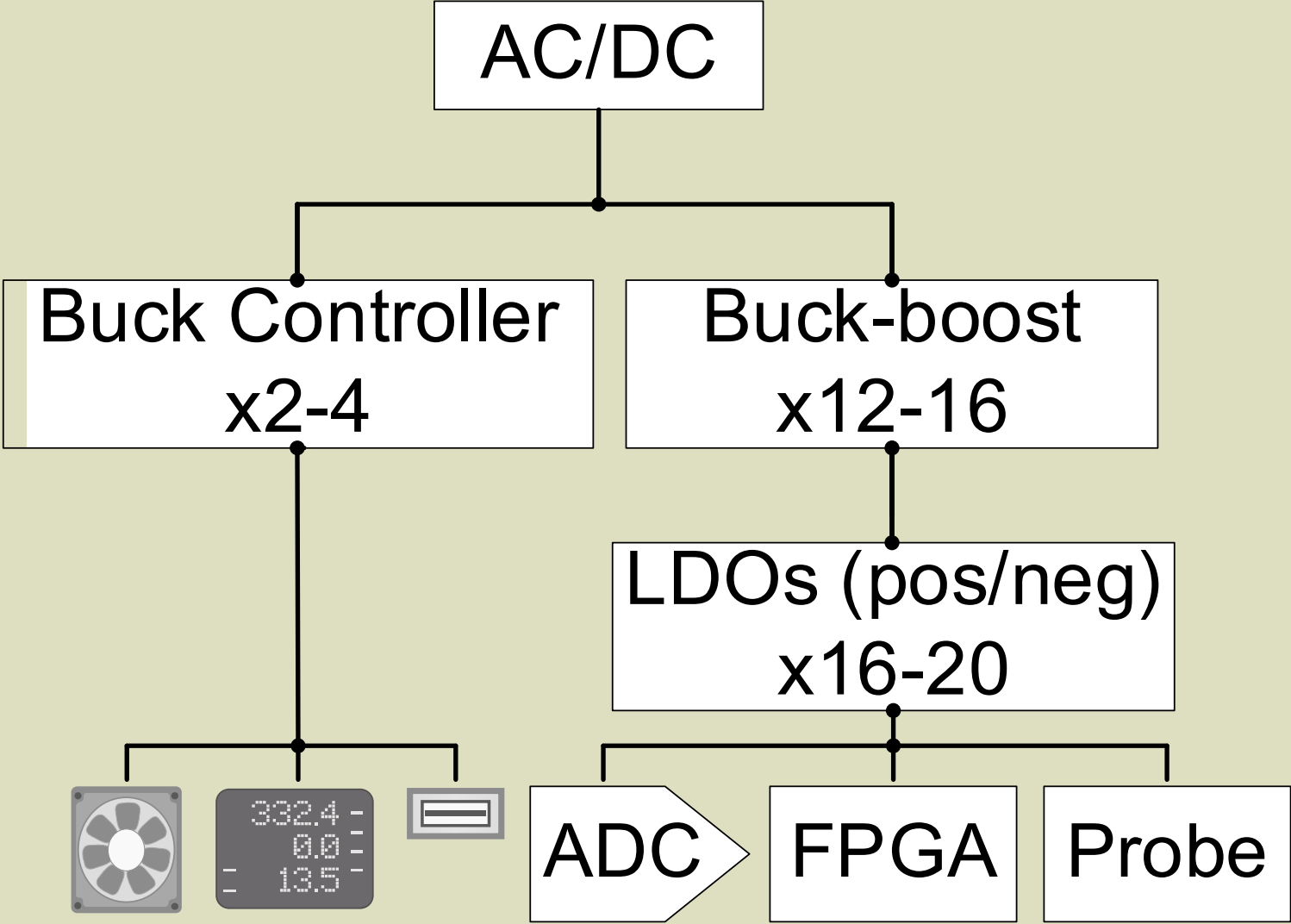
- Power (PWR) up/down sequence
- Interdependent sequence for each block
- Space limited

Power supply types:

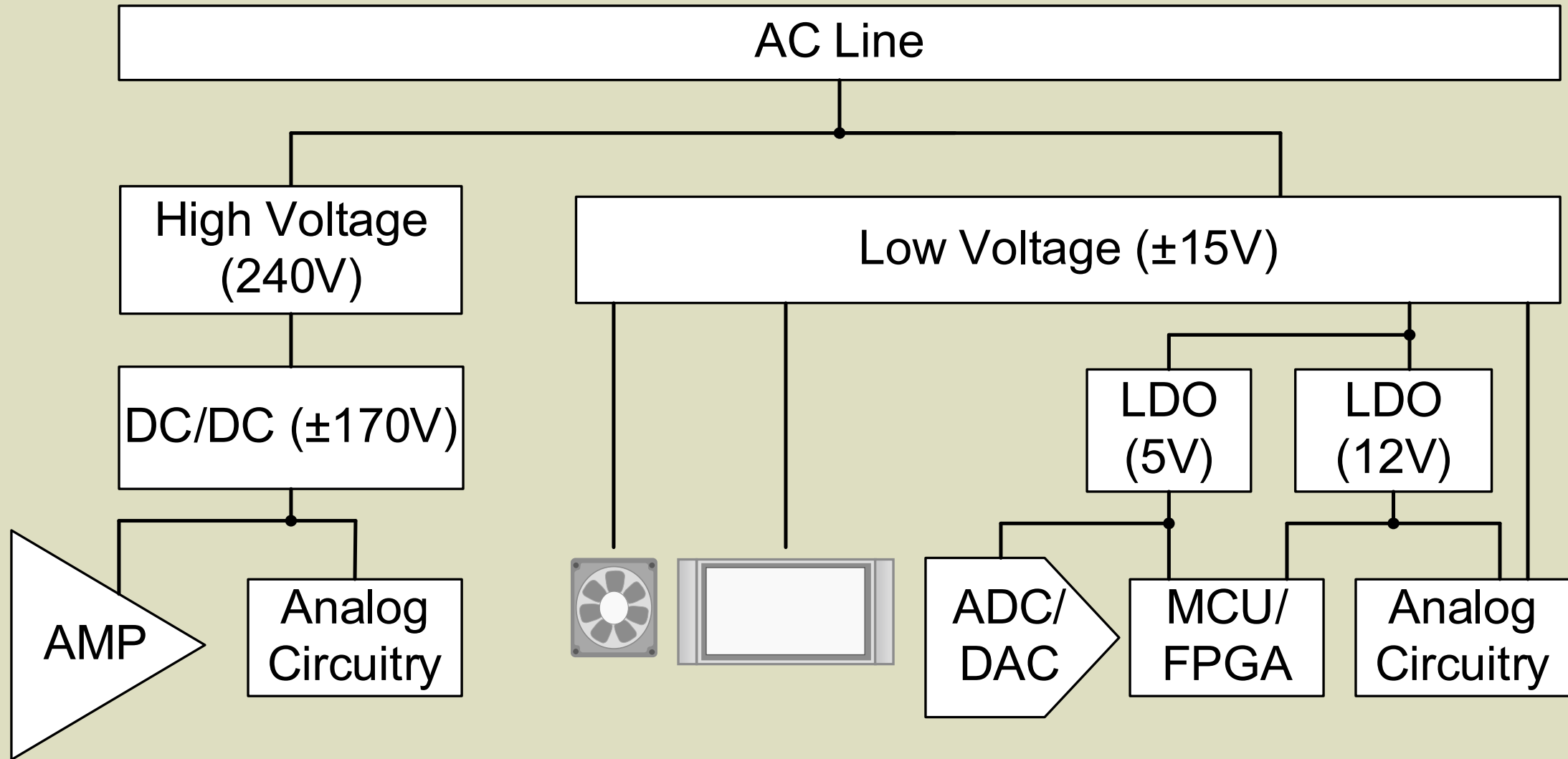
- Processor logic (0.8V to 1.8V)
- I/O (1.8V to 5V)
- Analog voltage ($\pm 24V$)
- High voltage for actuation biasing (up to 200V)



Oscilloscope Power Tree Example



SMU Power Tree Example



Background

Challenges:

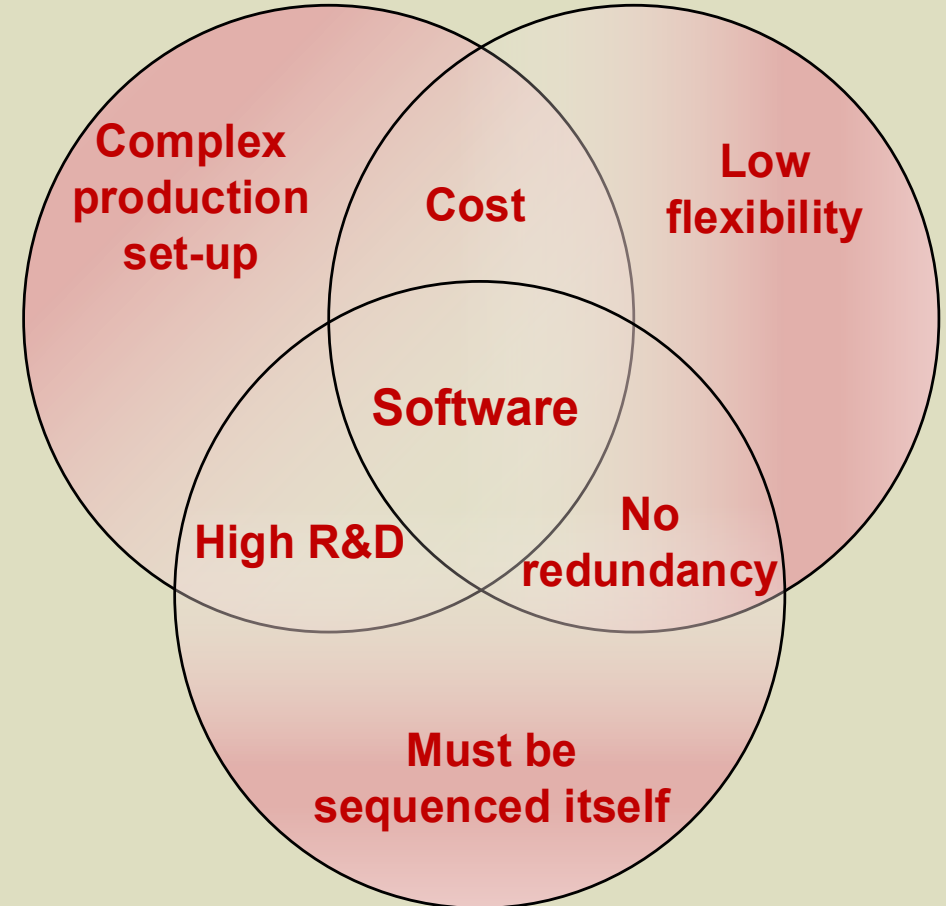
- Software
 - Writing FPGA/MCU code to properly ramp-up large amount of rails
 - Managing ramps of device under test (DUT) located remotely from the micro controller unit (MCU)
 - Continuous monitoring of supply rails
- Mismatch of rise times
 - Difference in load can alter the timing for a power rail
 - Specific ramp-up window (e.g. V_{CORE} must reach 0.5V within 5ms before V_{IO} starts rising)
- Fault management
 - What to do if power line is faulty?
 - How fast can software react to the fault and is it fast enough?

Dedicated sequencer

Scalable

Power management
integrated circuit

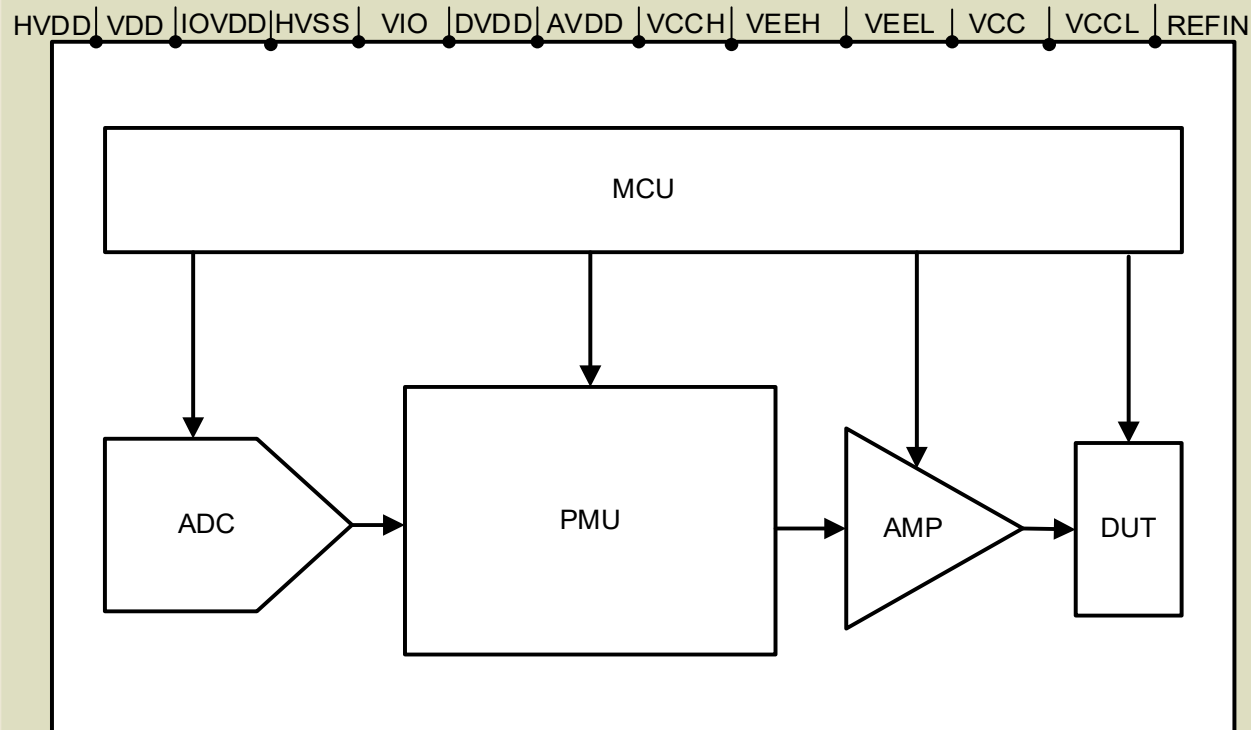
Advanced telemetry



MCU/FPGA

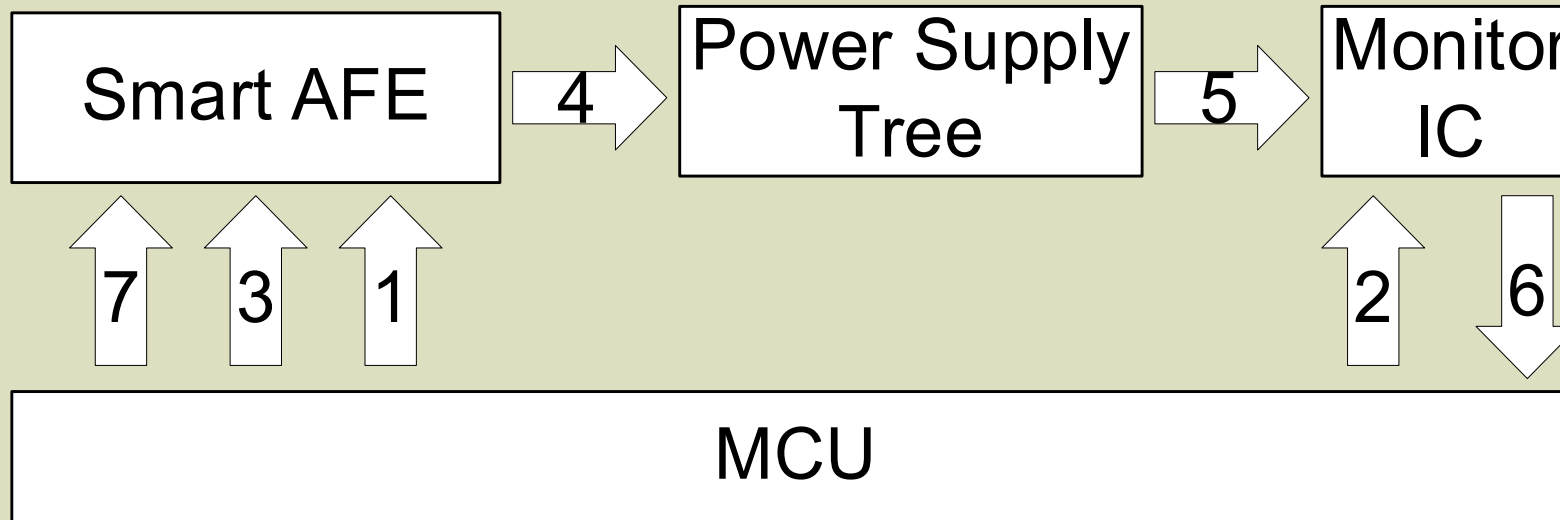
Flexibility

System Specification



ON Sequence	Function	PIN	Turn on Sequence								Turn off Sequence								Turn off Sequence	
			1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8		
1	MCU	IOVDD	[Waveform: rises at step 1, stays high]																	
2	MCU	VDD	[Waveform: rises at step 2, stays high]																	
1	AMP	HVSS	[Waveform: rises at step 1, stays high]																	
1	PMU	VIO	[Waveform: rises at step 1, stays high]								[Waveform: falls at step 8]								8	
2	PMU	DVDD	[Waveform: rises at step 2, stays high]								[Waveform: falls at step 7]								7	
3	PMU	AVDD	[Waveform: rises at step 3, stays high]								[Waveform: falls at step 6]								6	
4	AMP	PMU	VCCH	[Waveform: rises at step 4, stays high]								[Waveform: falls at step 5]								5
5	PMU	VEEH	[Waveform: rises at step 5, stays high]								[Waveform: falls at step 4]								4	
6	AMP	PMU	VEEL	[Waveform: rises at step 6, stays high]								[Waveform: falls at step 3]								3
7	PMU	VCC	[Waveform: rises at step 7, stays high]								[Waveform: falls at step 2]								2	
7	AMP	VCCL	[Waveform: rises at step 7, stays high]								[Waveform: falls at step 2]								2	
8	PMU	REFIN	[Waveform: rises at step 8, stays high]								[Waveform: falls at step 1]								1	
(any time)	ADC	HVDD	[Waveform: rises at any time, stays high]																	

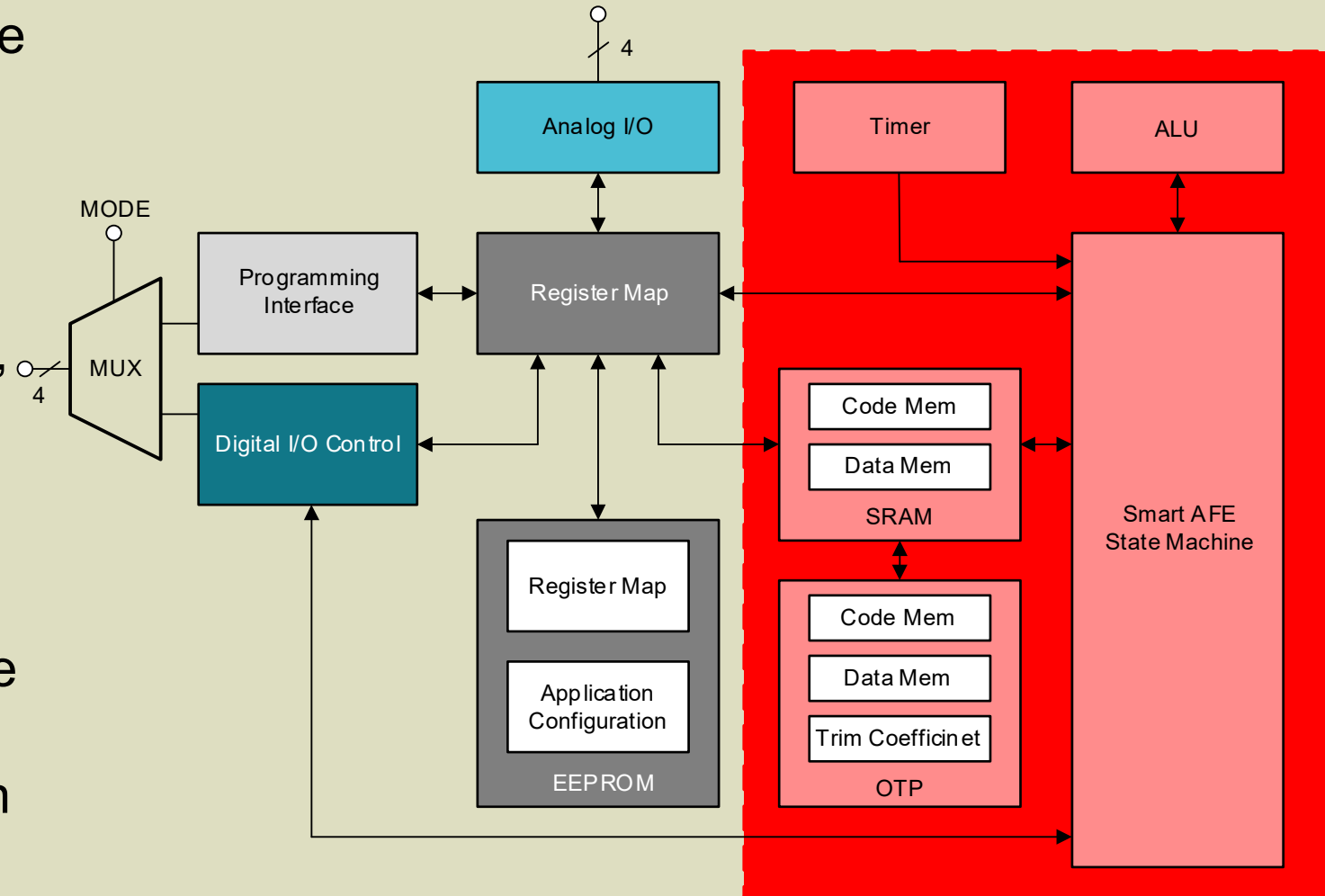
Solution



1. Sequence parameters write one-time (I²C/SPI)
2. Monitor parameters write every power-cycle (I²C/SPI)
3. Initiate power up/down sequence (GPIO)
4. Execute power up/down sequence (DAC/GPIO)
5. Continuous monitoring (ADC)
6. Send alarm if fault detected (GPIO)
7. Fault response command (GPIO)

What is Smart Analog Front-end (AFE)?

- State machine (SM) allows flexible and fast creation of custom parts without changing silicon
 - Control loop, GPIO, fault management
- SM supports multiple instructions, ALU, timer, and SRAM space for firmware
- SM logic is stored in the one-time programmable (OTP) memory
- Parameters to the SM, and device configurations are stored in the EEPROM and can be adjusted on the fly



State machine

Digital IO

Analog IO

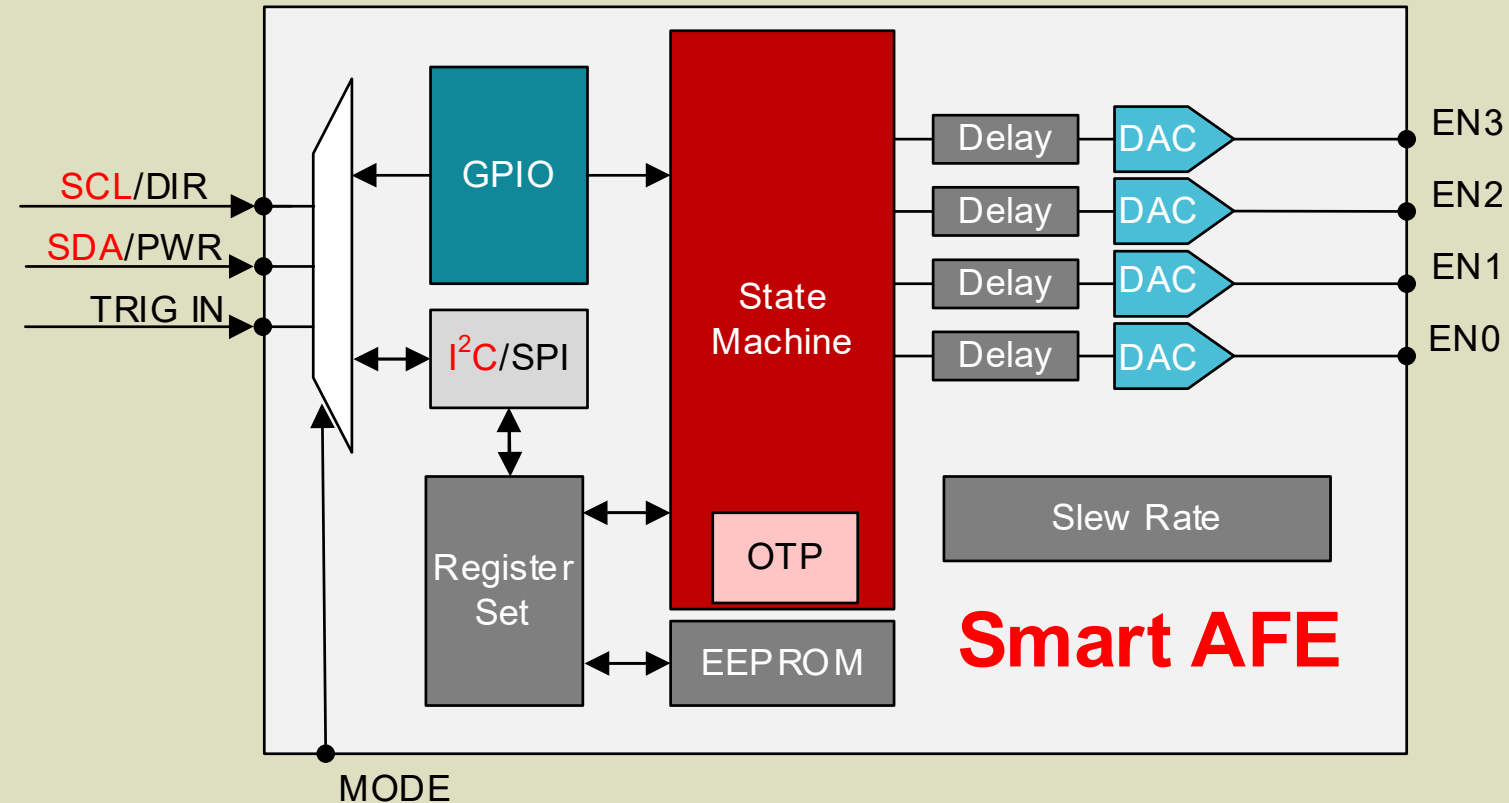
Features

Inaccessible

Power Supply Sequencing and Monitoring

Sequencing | Solution

- Independent configurable delay, and sequence for PWR UP and DWN
- PWR UP/DWN is selected by the DIR pin
- TRIG IN to initiate the sequence
- PWR pin to immediately disable all channels in case of fault
- Programmable slew rate per channel to control the speed of power supply ramp



State machine

Digital IO

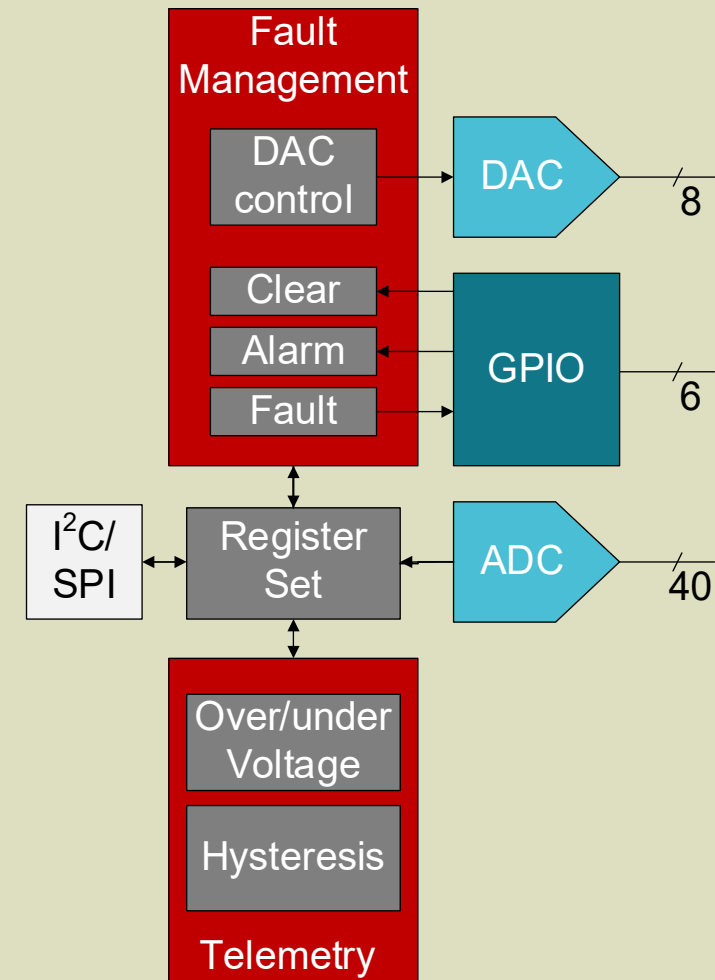
Analog IO

Features

Inaccessible

Monitoring | Introduction

- Guard logic:
 - Monitoring of each channel
 - Under voltage/over voltage
 - Programmable hysteresis
- Alarm:
 - Generate alarm when fault is detected
 - Control DAC outputs in the event of fault
- Configurable via internal registers



Guard logic

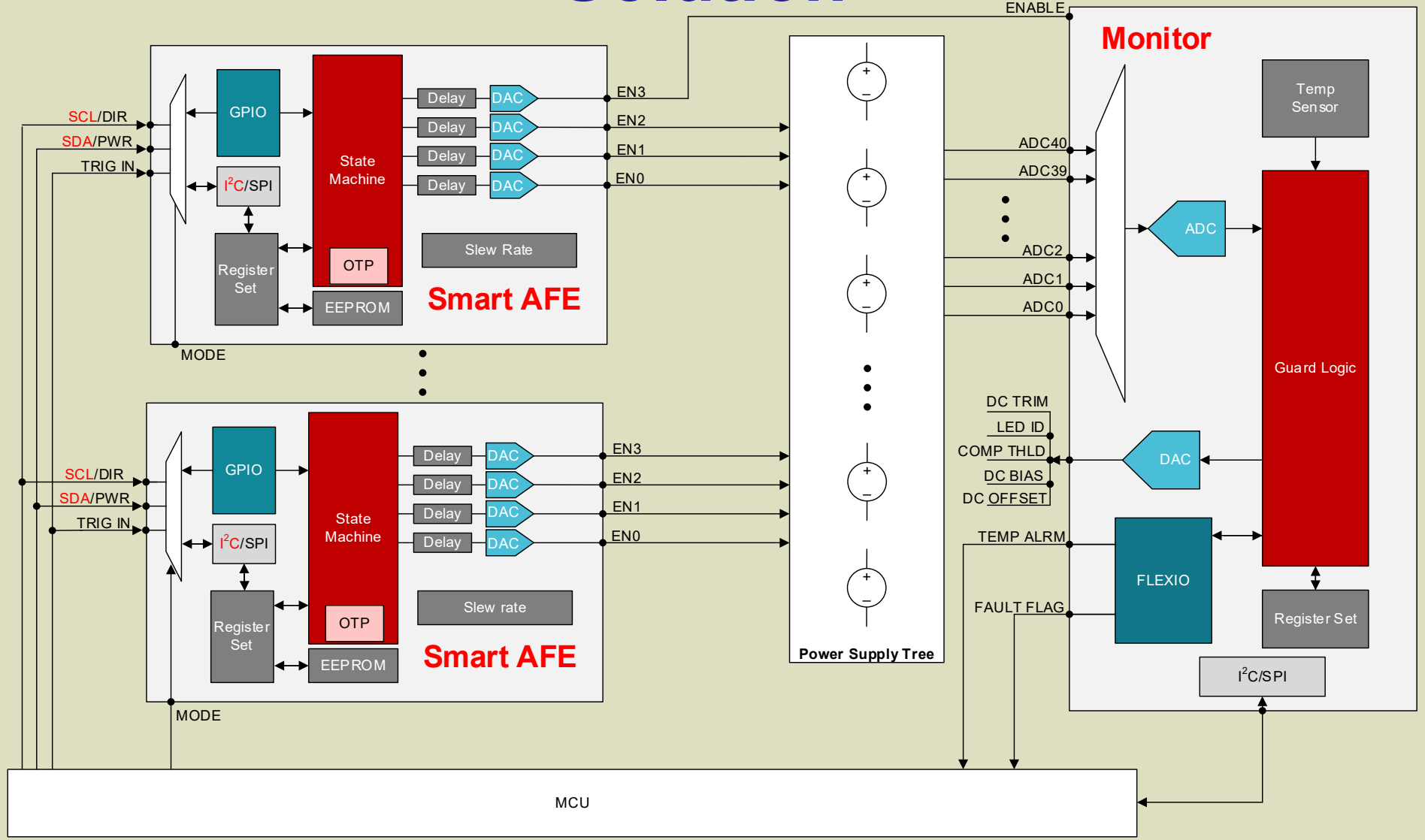
Digital IO

Analog IO

Features

Inaccessible

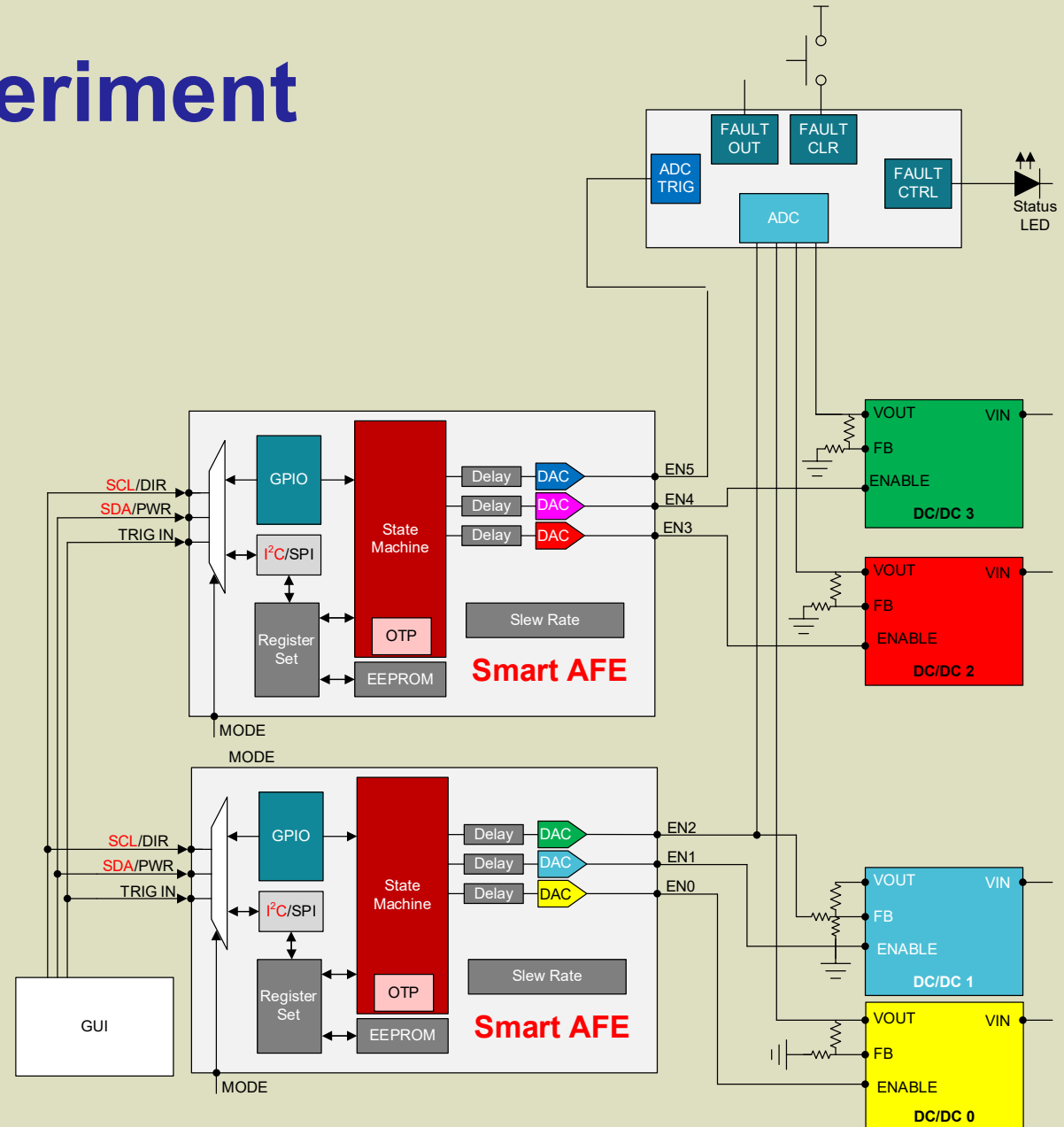
Solution



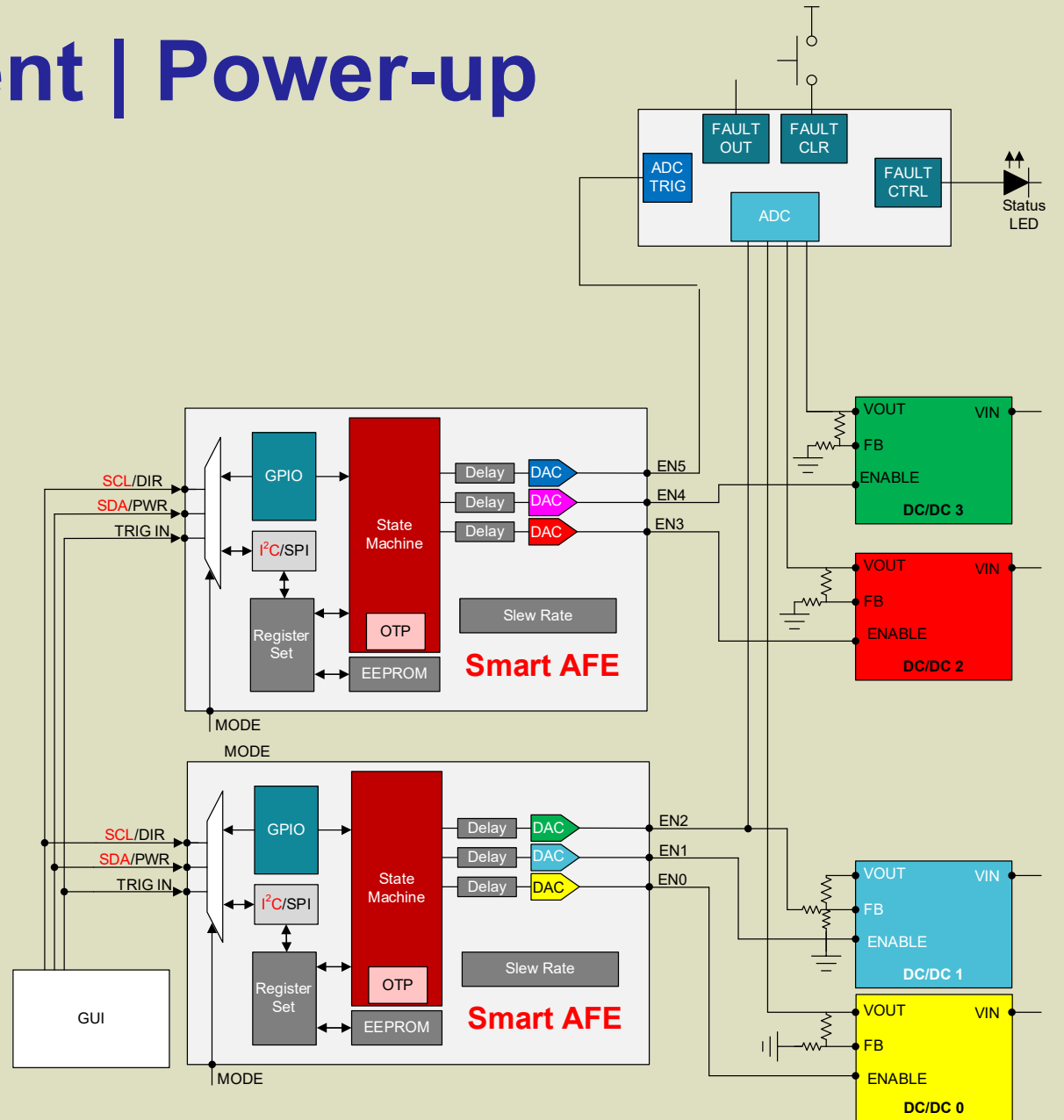
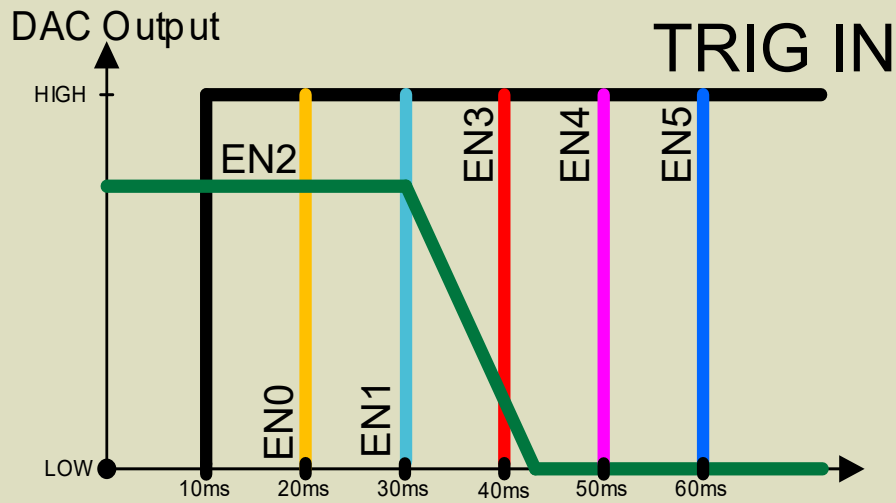
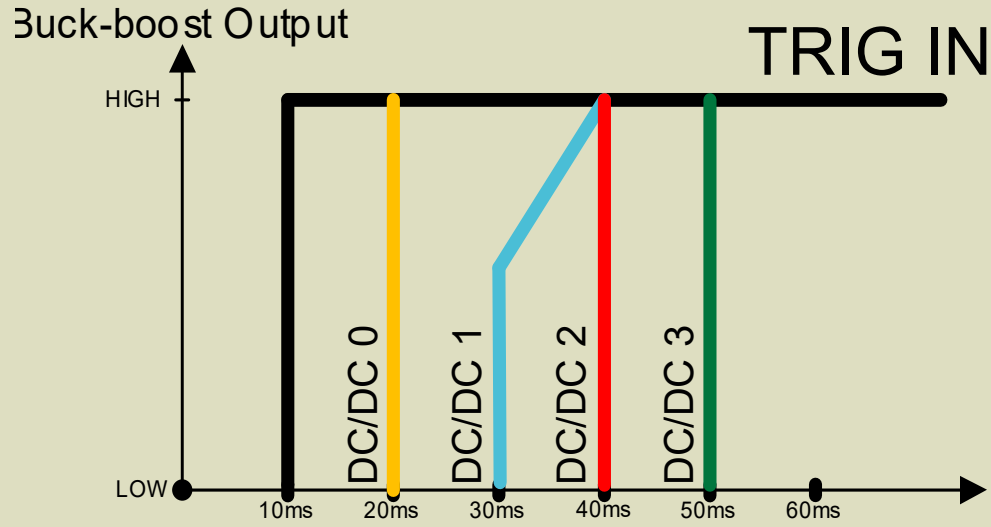
State machine/guard logic | Digital IO | Analog IO | Features | Inaccessible

Experiment

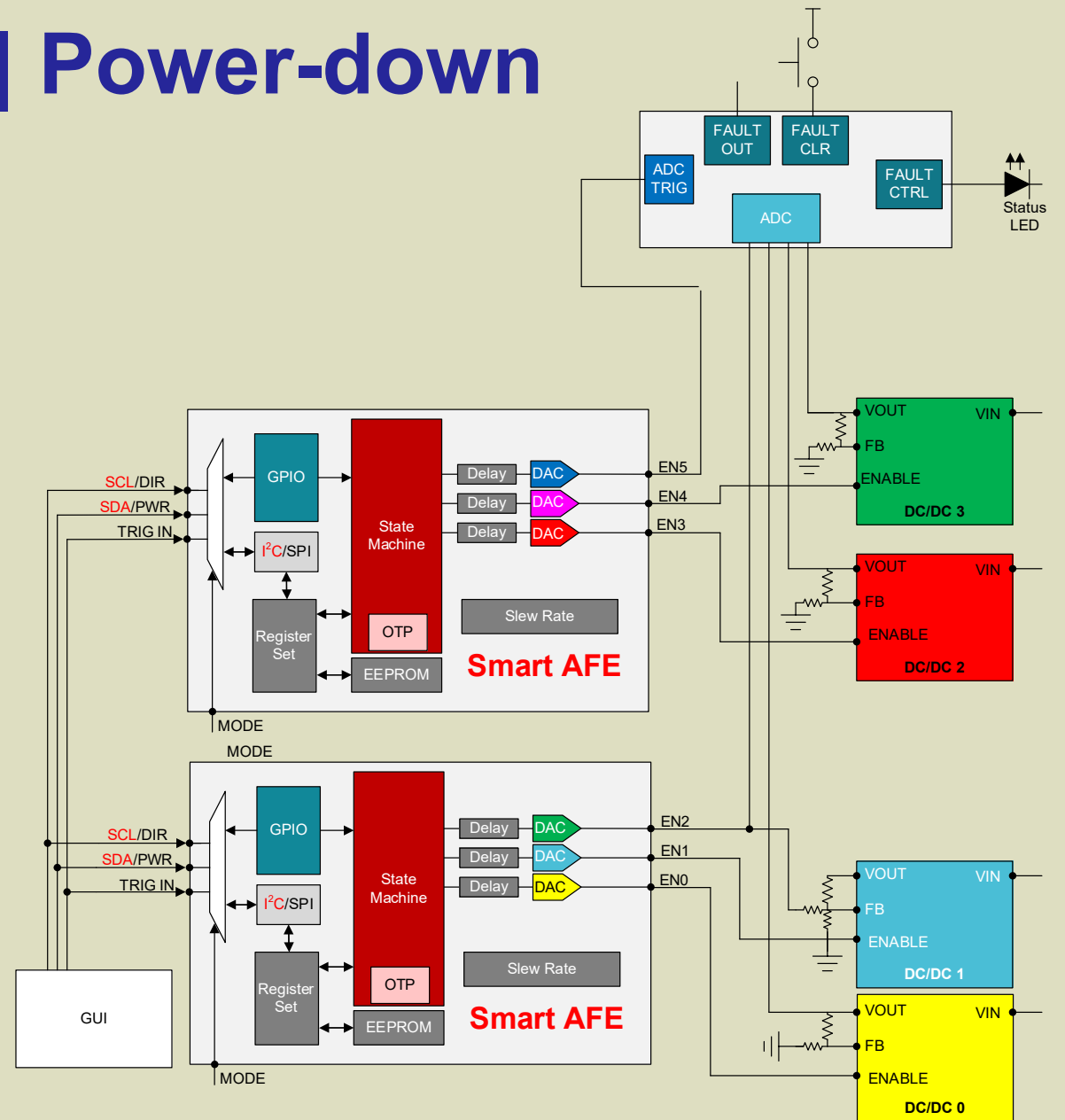
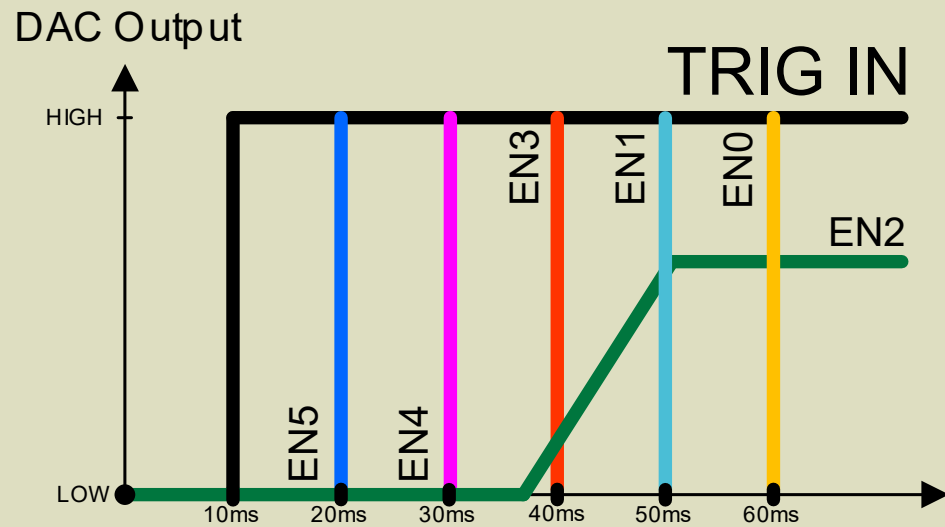
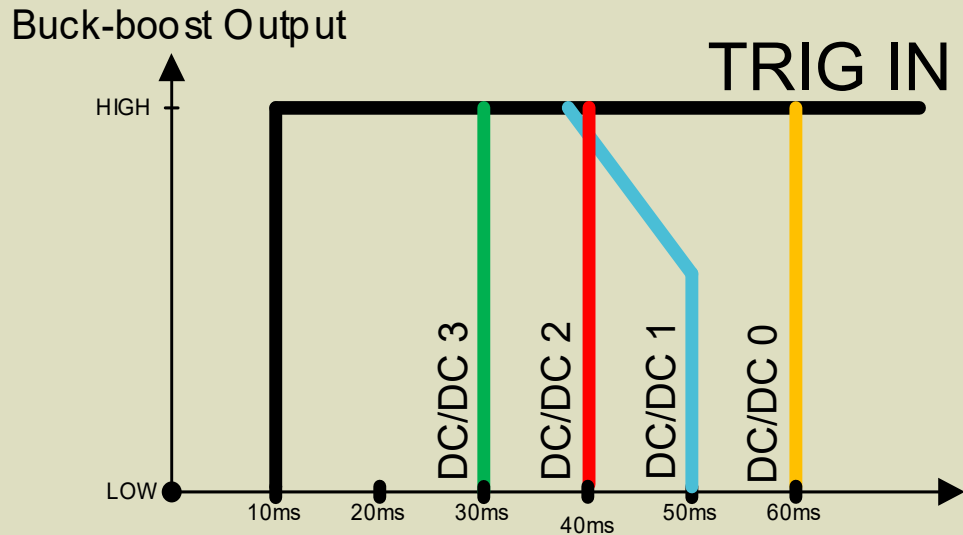
TRIG-IN	DIR	PWR	SYSTEM
0	X	1	Do nothing
1	1	1	Start power-up sequence
1	0	1	Start power-down sequence
X	X	0	Immediately shut off all channels. Latches until reset



Experiment | Power-up

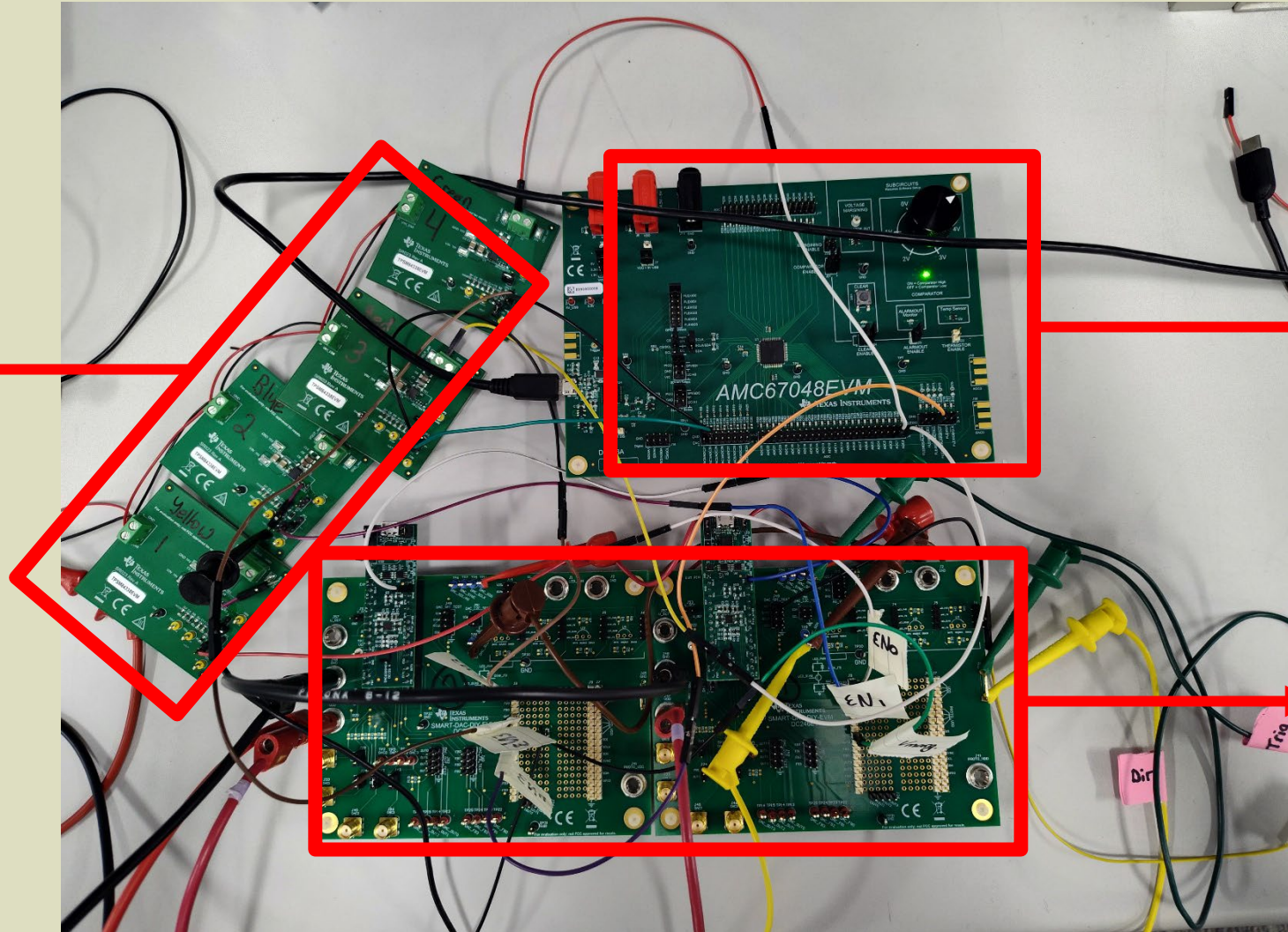


Experiment | Power-down



Results | Set-up

Power
Supply
Tree



Monitor

Smart AFE

Results | Software-free Controlled AFE Sequence

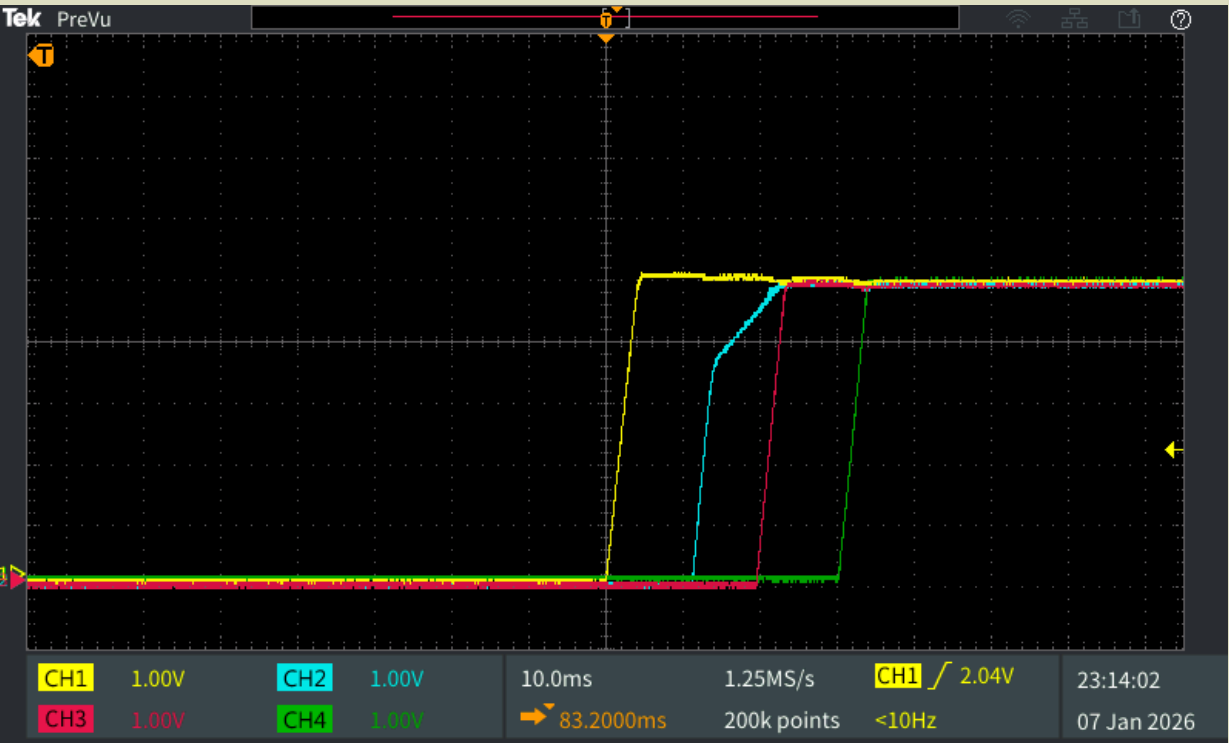
Power-up

Power-down

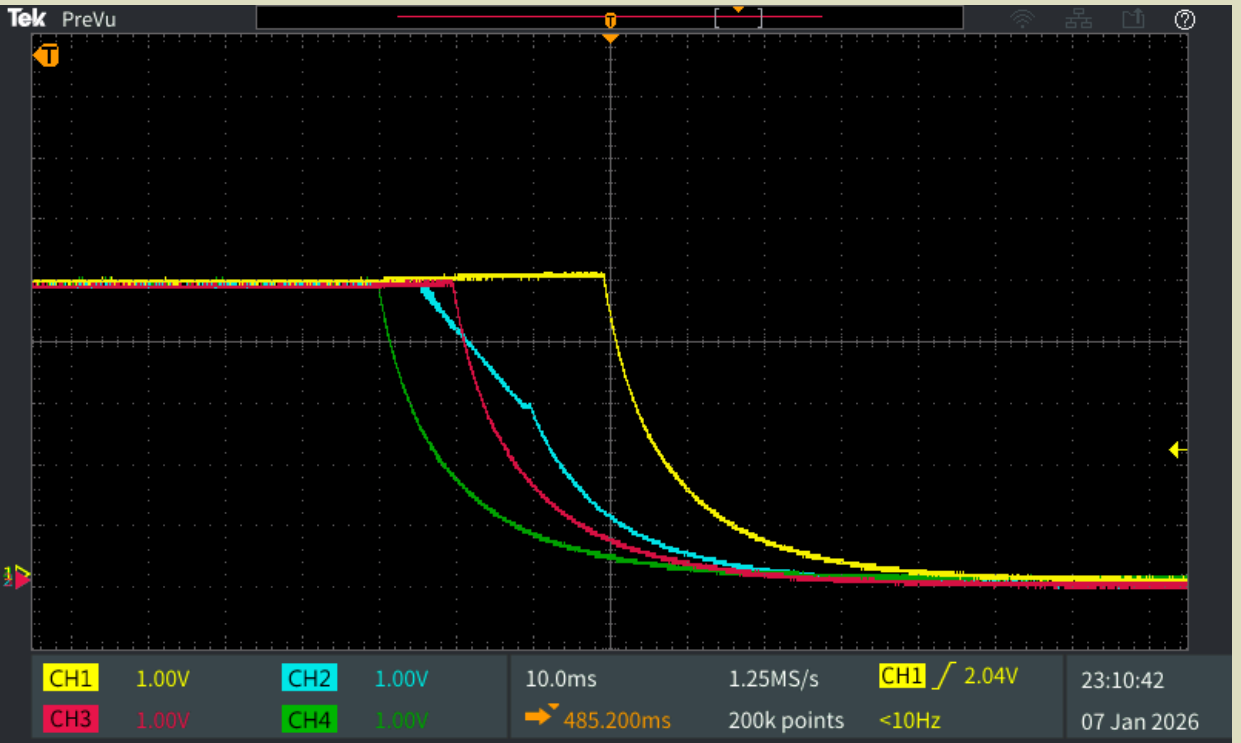


Results | DC/DC Controlled Power Sequence

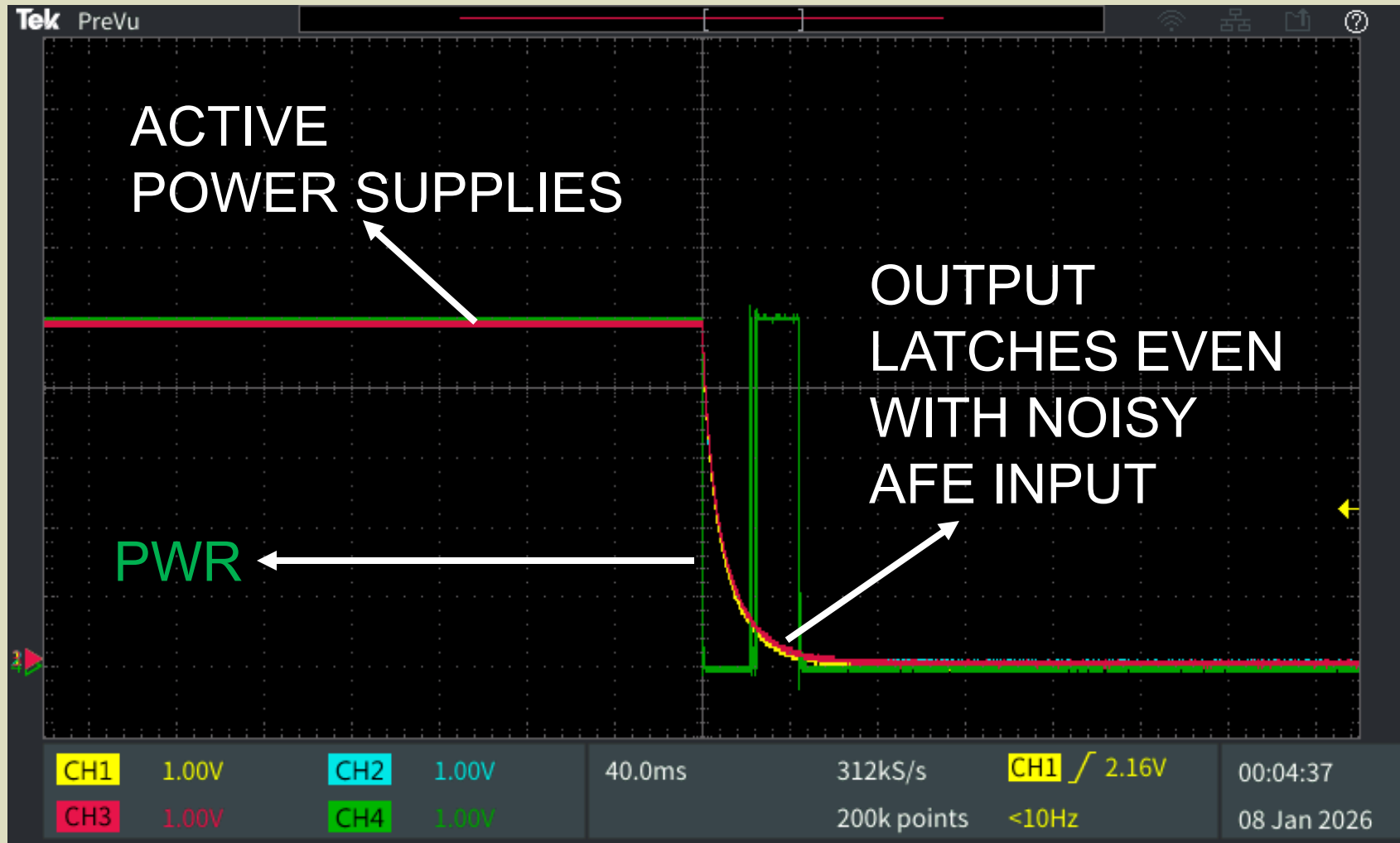
Power-up



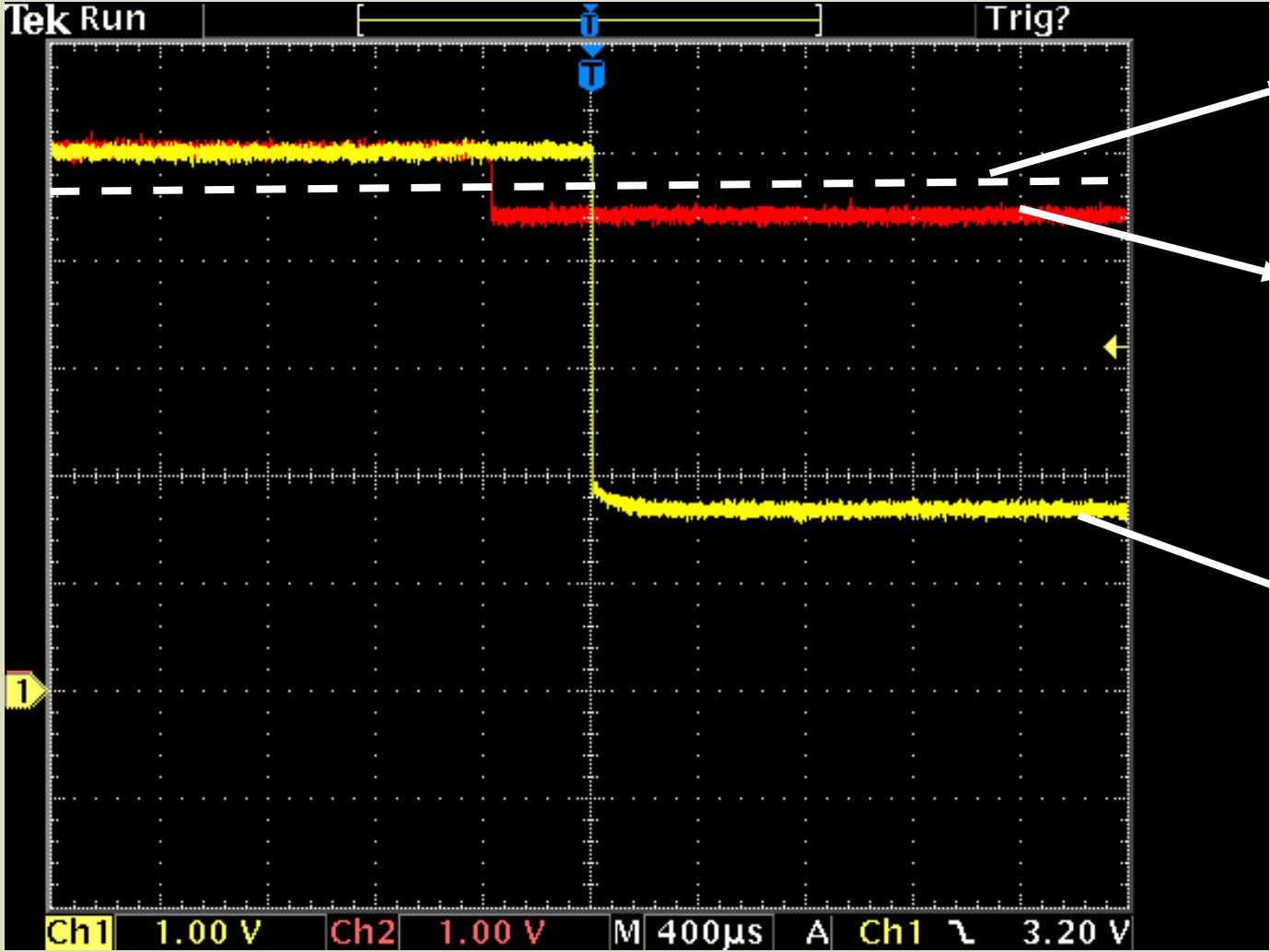
Power-down



Results | AFE Shut Down Command Response



Results | Monitor IC Power Rail Fault Response



FAULT THRESHOLD

POWER

ALARMOUT (active LOW)

In Summary

- Power management in tester equipment requires extensive R&D
 - Some systems require over 40 channels of dynamic power supply control
 - Software/hardware development
 - Trade off between common sequencing and power management solutions
- Flexible solution with minimal software
 - State machine configured for the sequencing and power supply ramp control
 - Adjustment of timing on the fly via internal registers
 - High channel density monitoring
 - Predictable response

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