TWENTY-SEVENTH ANNUAL

TestConX™

Archive

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HPC Chip Complexity Drives Need for Integrated Test Cell Solutions for SLT

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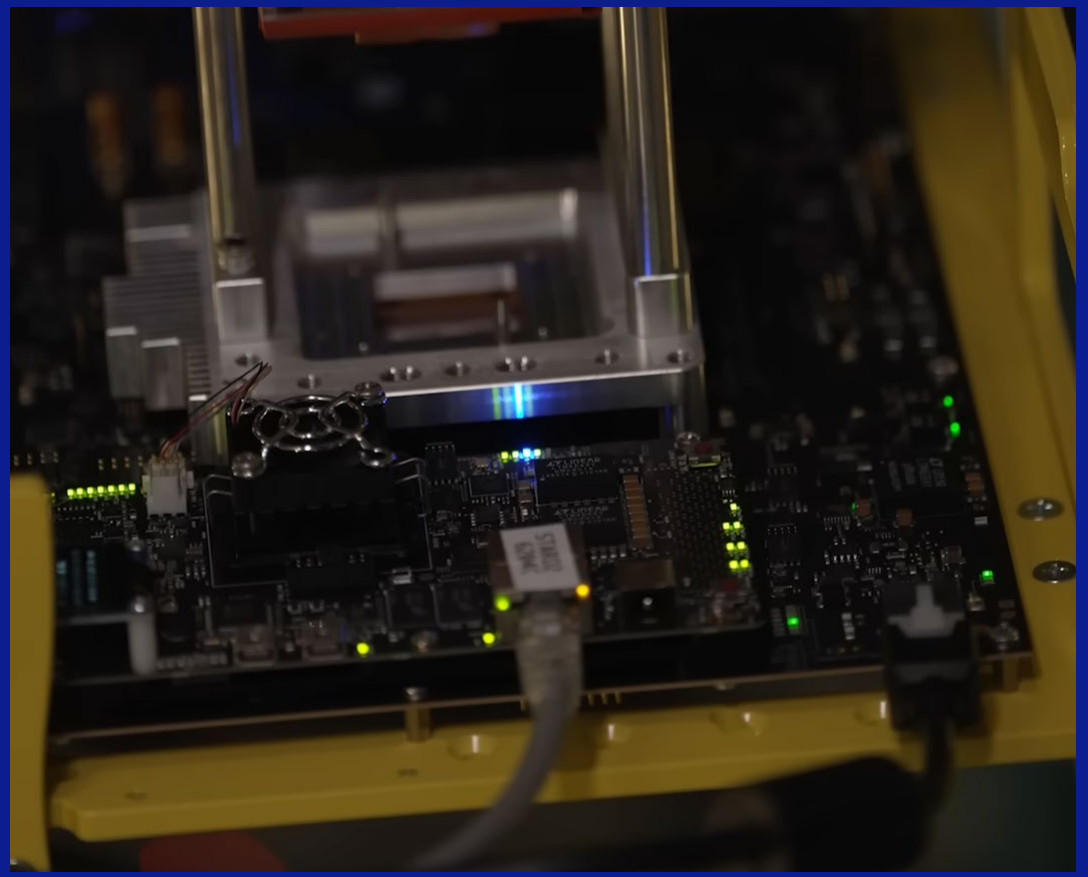
- What is System Level Test (SLT)?
- Challenges for SLT of High-Performance Compute (HPC) Devices
  - Volume Scale
  - Electrical Power & Signaling
  - Thermo-mechanical
  - Network & Software,
  - Actionable data for Machine Learning and Artificial Intelligence (ML/AI)
  - Automation
- Integrated Test Solution

What is SLT?

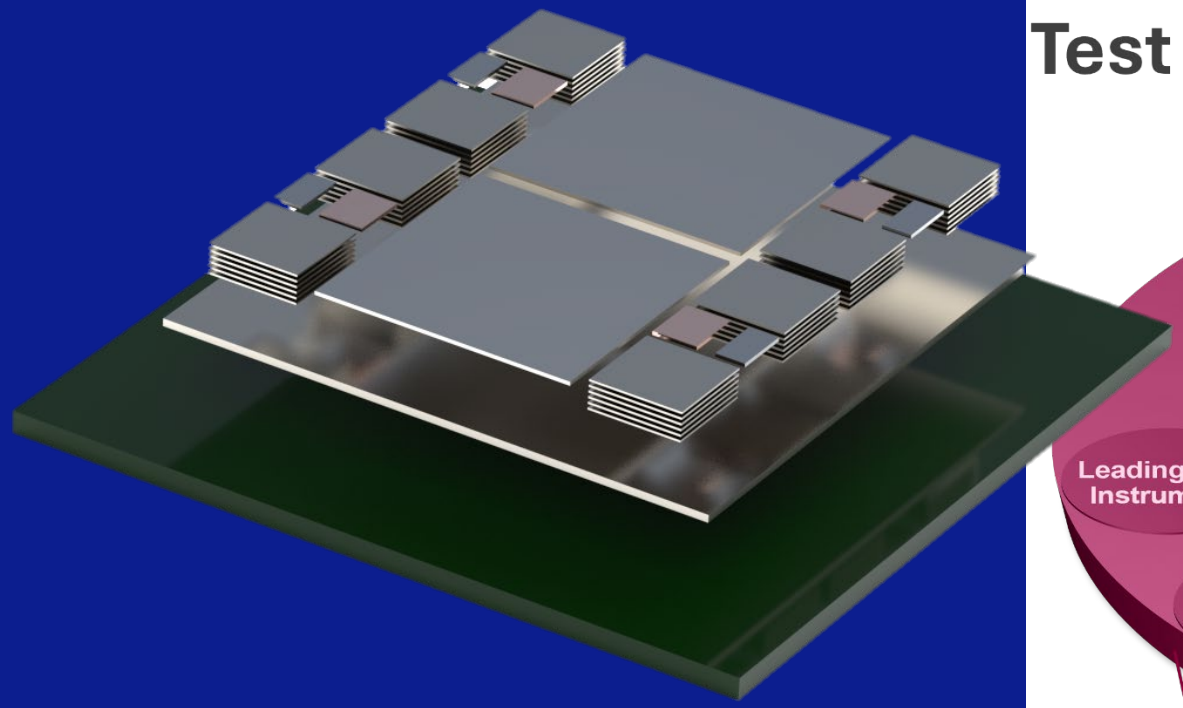
Test Coverage: Focus on critical test coverage items not covered by ATE

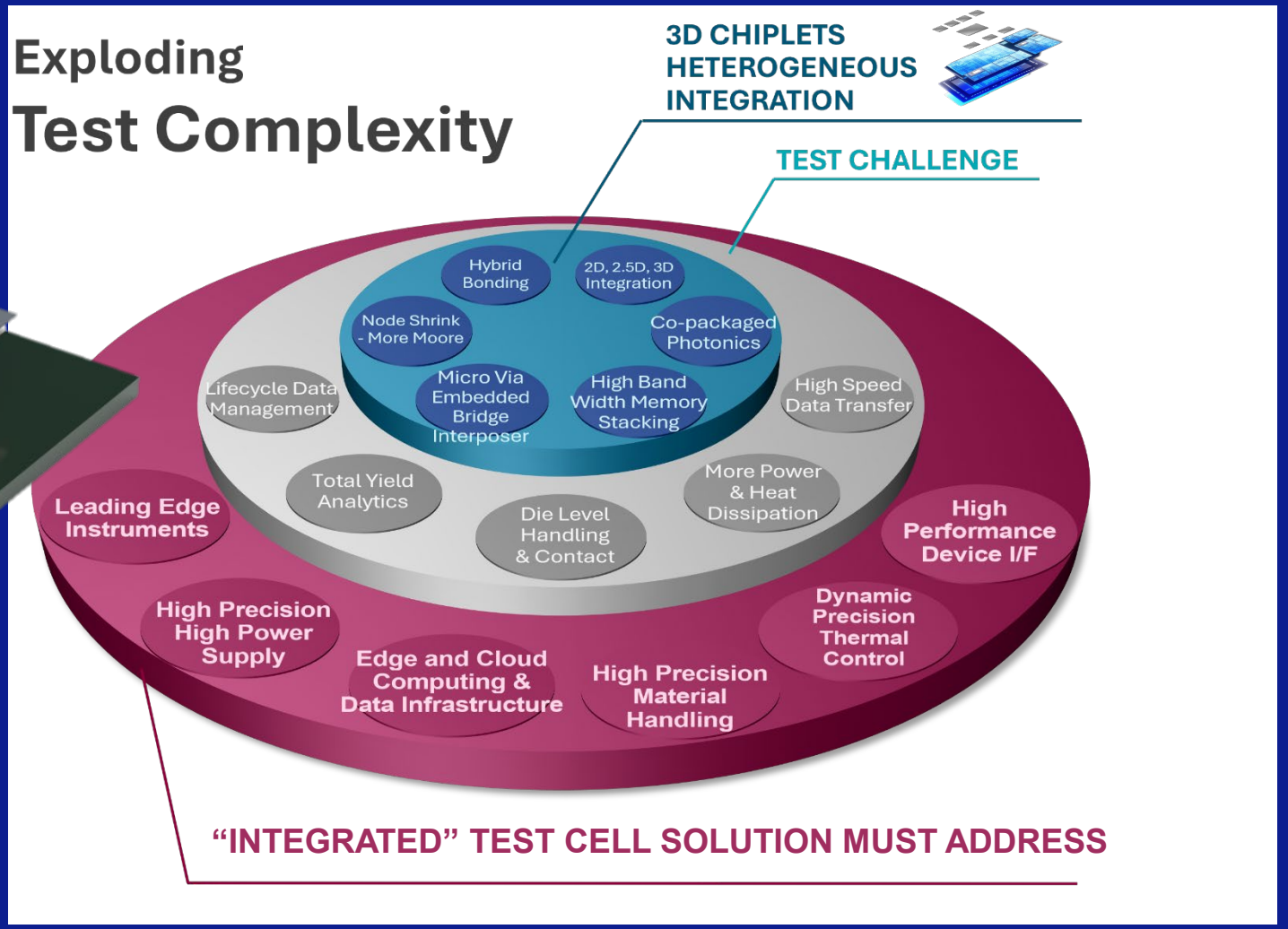
- DUTs are mostly processors
- Socketed applications board
- Test are software-centric
  - Boot OS
  - High-speed data traffic
  - Performance at temperature
  - Vmin and power checks
  - Reboot and repeat



Source: CNBC: https://youtu.be/UdhWvg5mycY

SLT in the Era of Complexity - Affordably





Relative Cost Comparison of Test Insertions for High-Performance Computing Processors

Long test times demand low costs while providing high performance and reliability

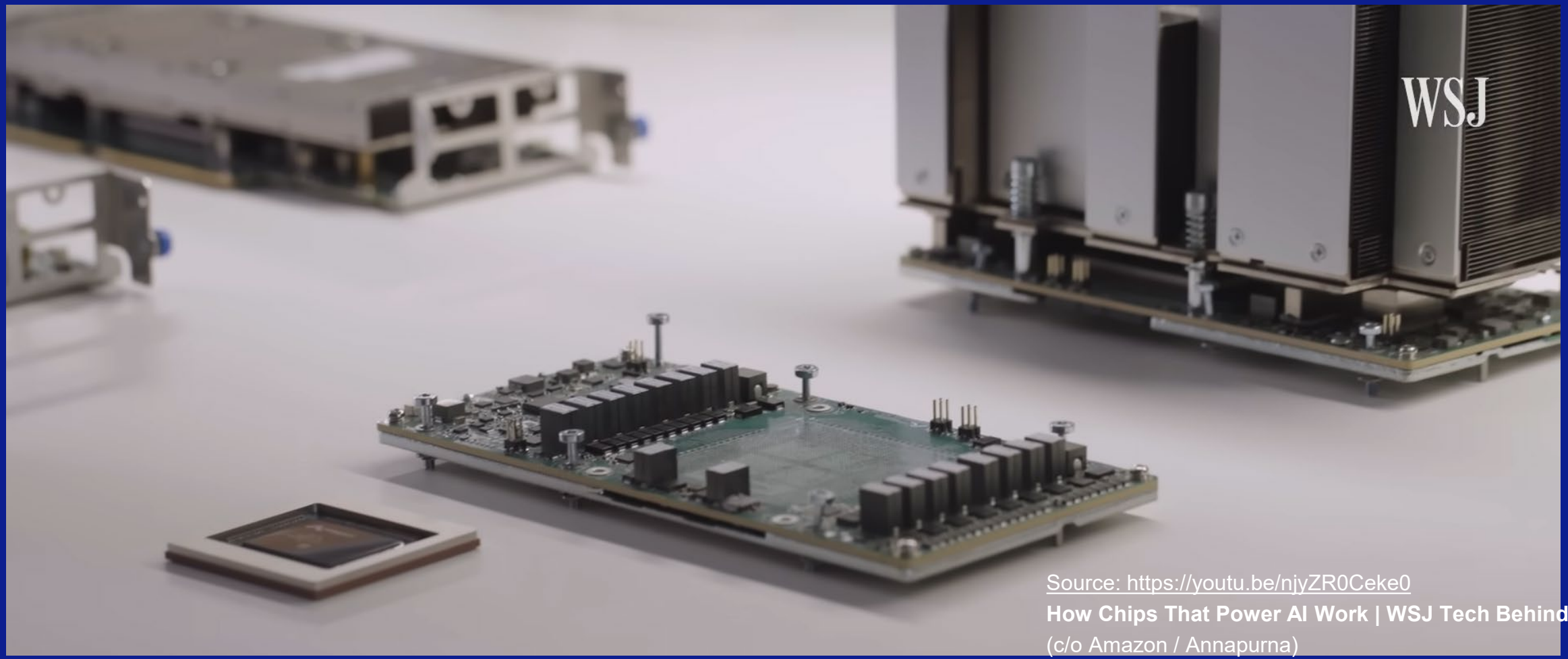
Wafer Sort	Final Test	System Level Tester	Burn-in
Mid pin count ATE + prober	High pin count/ high power ATE + Tri-Temp handler	Integrated handler, thermal, test electronics	Non-automated oven, thermal, electronics
1 site in parallel	1 site in parallel	~6 to 132 sites in parallel	112 sites in oven
$$$$ / site	$$$$ / site	$$ / site	$ / Site
~<2 min TT	~<5 min TT	~30-120 min TT	3-8 hr HVM TT (HTOL = 1000 hrs)*

Relative Example Only – prices and site count vary tremendously based on performance

*HTOL – High Temperature Operating Life is typically used to qualify a process, not 100% production test insertion, but it often uses similar burn-in equipment

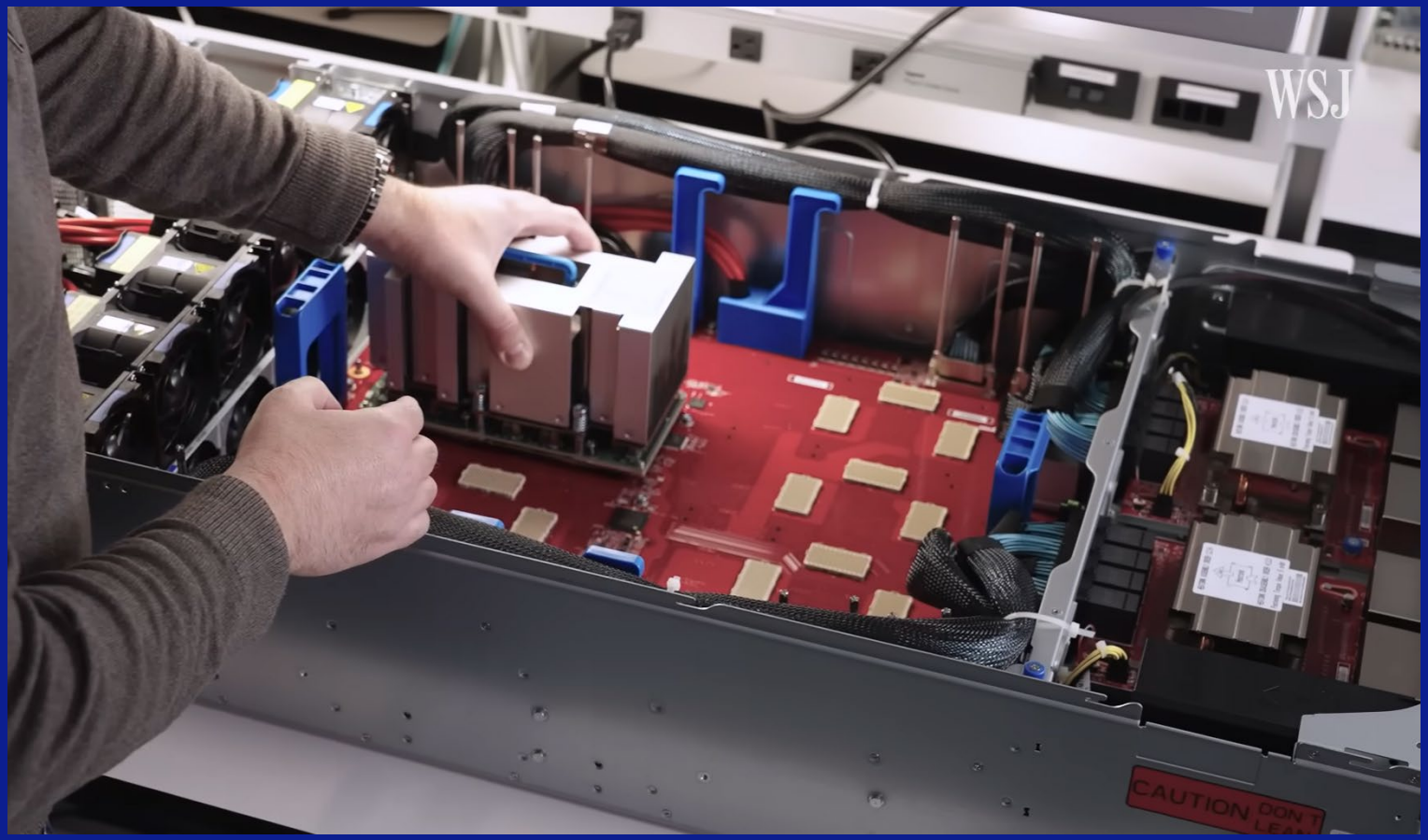
Budgetary Simple Test Site Calculator	
Annual Unit Volume	1,000,000
Weekly Unit Volume	19,230.77
Avg Daily Volume	2747
AVG Hourly Volume	114
Expected Test Time (min)	45
Ideal /perfect test sites:	86
Efficiency (Retest, Indexing, Maint & Test Ops)	75%
Planned Test Sites	**114**

Example Challenge - Stack-up of Socketed SLT Board for Electrical & Thermal



Source: https://youtu.be/njyZR0Ceke0
How Chips That Power AI Work | WSJ Tech Behind
(c/o Amazon / Annapurna)

Example Challenge Continued



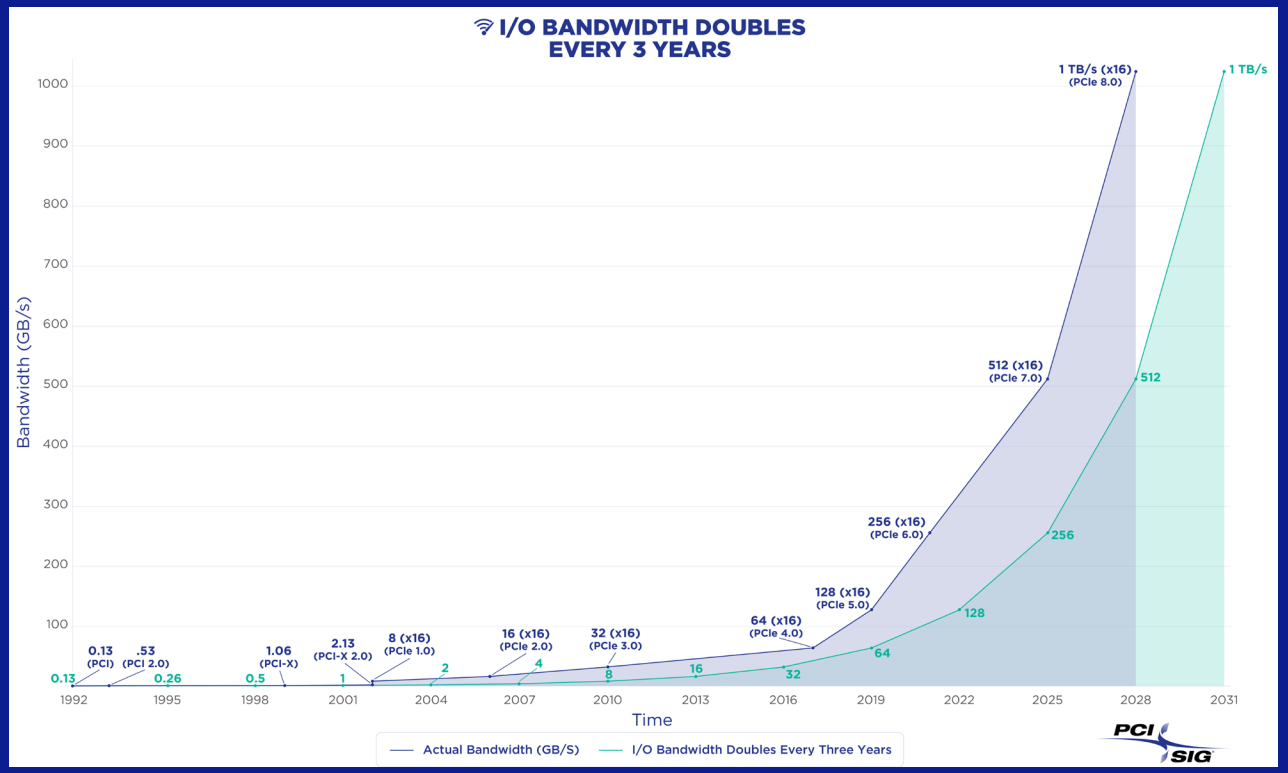
Source: Wall Street Journal, “How Chips That Power AI Work”
https://www.youtube.com/watch?v=njyZR0Ceke0

High Volume Mfg Test:

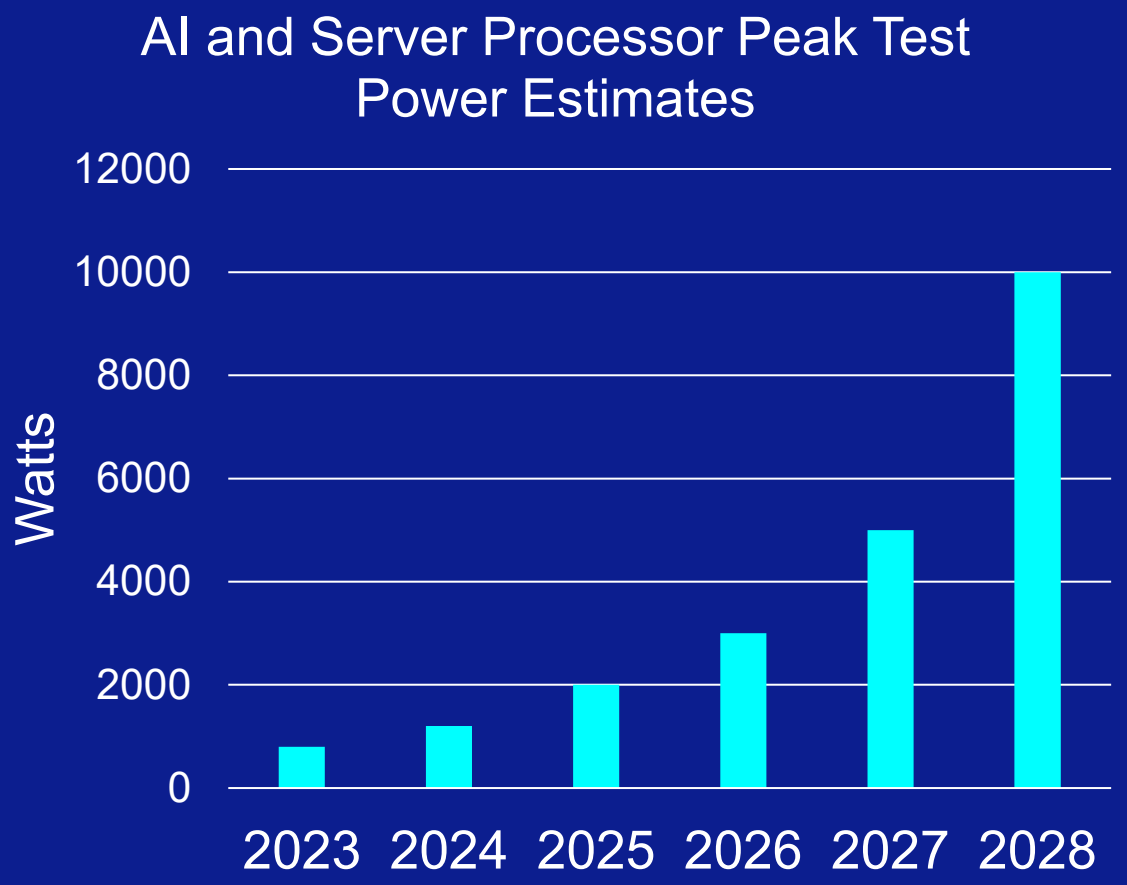
- Automate DUT placement
- Automate socket actuation
- Automate thermal engagement
- Provide electrical power and control
- Update SW in real-time
- Collect actionable data
- Minimize floor space

Electrical Challenge: TB/s Data Rates & KW of Power

HPC system-level testers must support the leading-edge chip technology

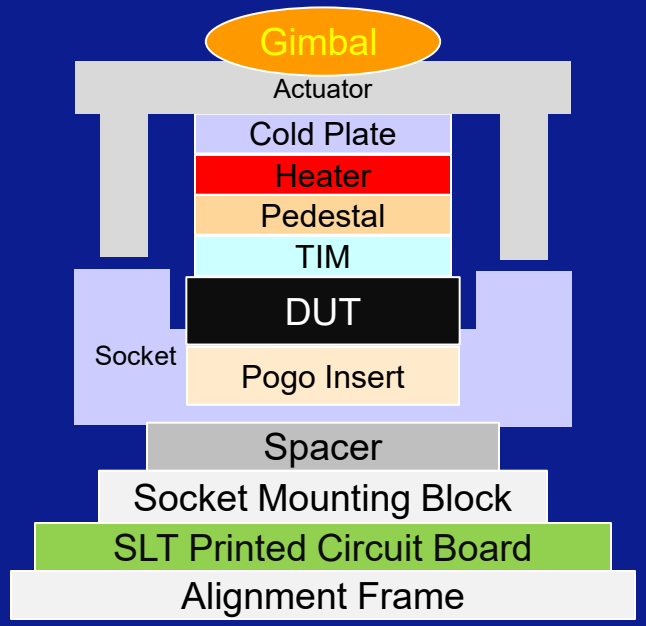


https://www.businesswire.com/news/home/20250805675479/en/PCI-SIG-Announces-PCI-Express-8.0-Specification-to-Reach-256.0-GTs



Mechanical Challenge: Socket Actuation

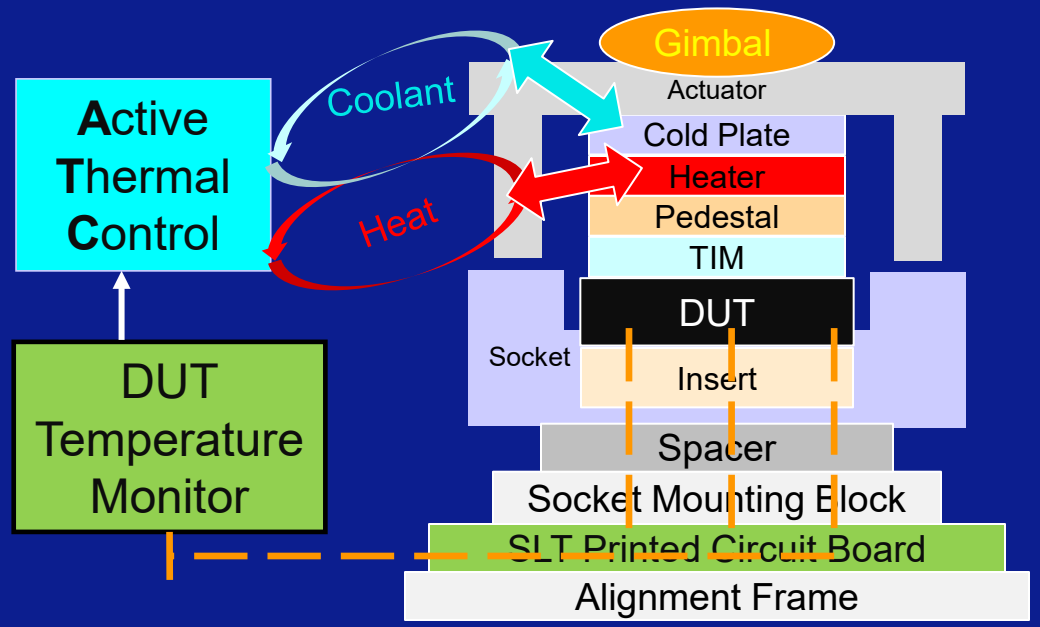
- Move out of the way so handler can drop the part in the socket
- Align perfectly every time
- Supply 100s of Kg of force
- Evenly compress non-coplanar surfaces to make good electrical contact with pogos
- Provide thermal control / heat & cool
- Repeat every ~30-60 minutes reliably



Thermal Challenge: Control Loop Feedback

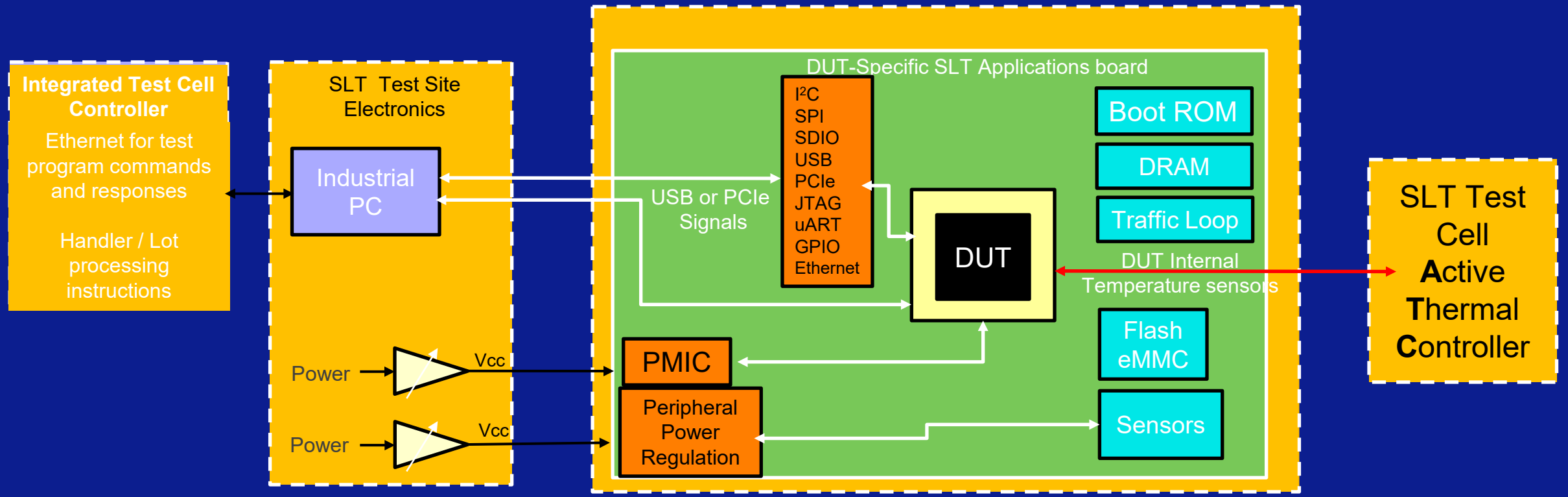
- Customer* chip Tj sensors
- Customer SLT PCB
- Multiple hot spots
- Customer algorithm for aggregating multiple temperature sensors
- Test cell vendor ATC algorithm
- Available multi-zone control

*“Customer” is chip designer



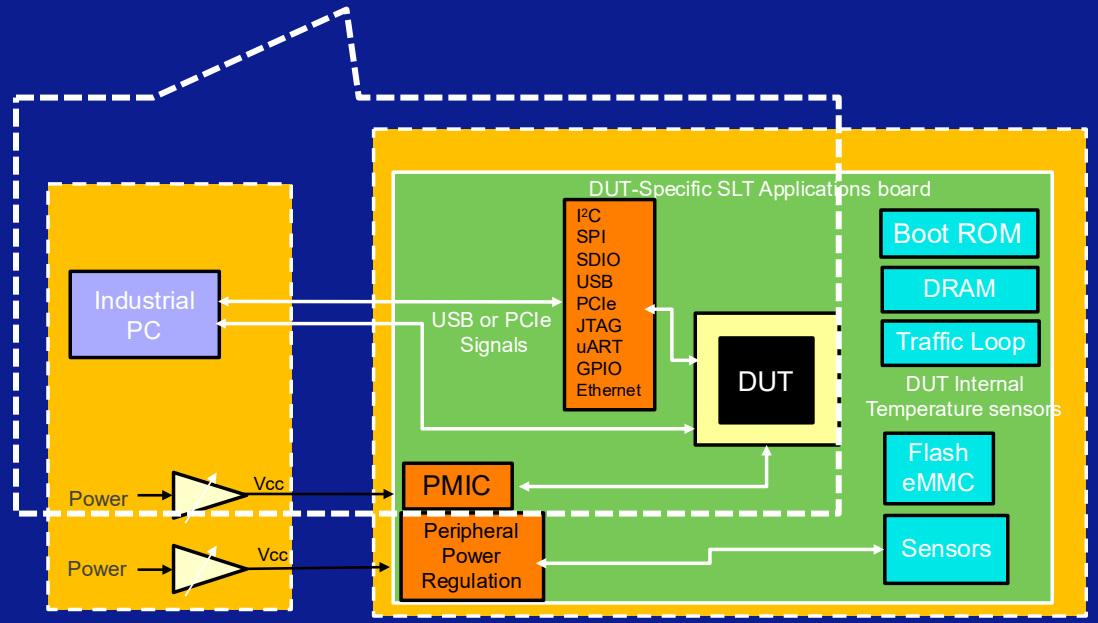
Integrated Test Cell Solution: Typical Electrical Test Interfaces for SLT

Test Cell Infrastructure: Power, communications, automation, thermal, SW, network

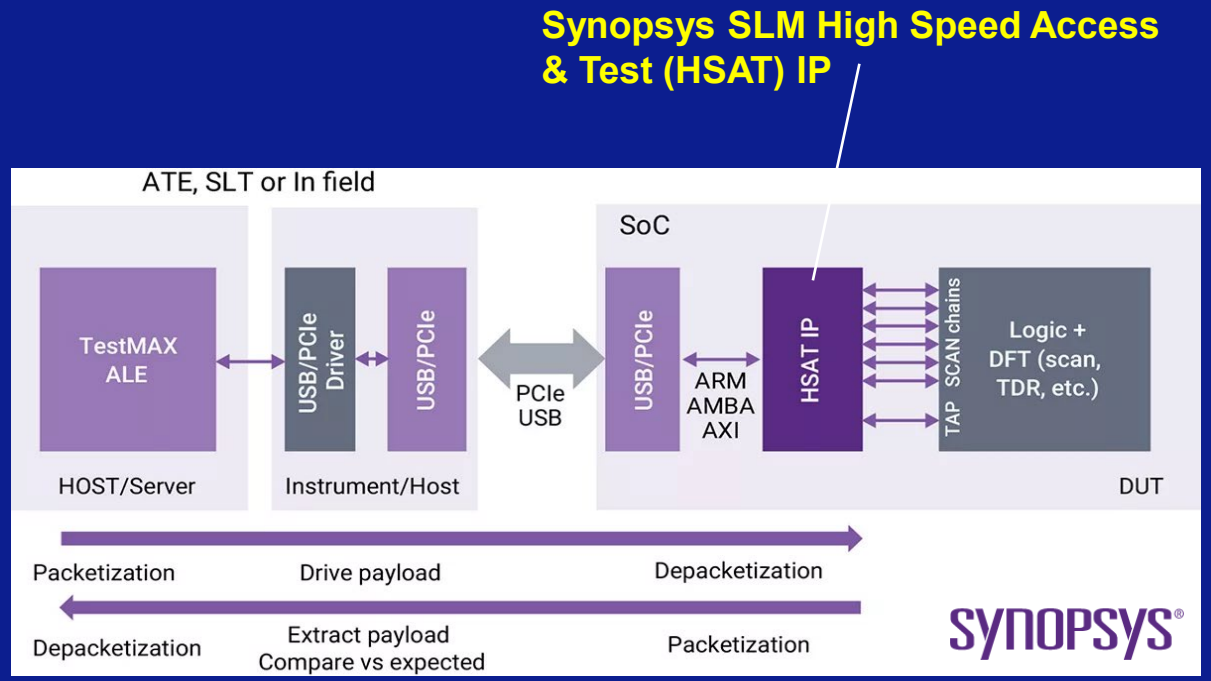


Migration of Test: Scan-over-PCIe or USB
New DFT Techniques for Structural Test Coverage at SLT

SLT has cost-effective infrastructure enabling structural test over high-speed serial ports



Example from Synopsys: High-speed access & test IP acts as a subordinate on AXI bus, serving as a bridge between HSIO and DFT network

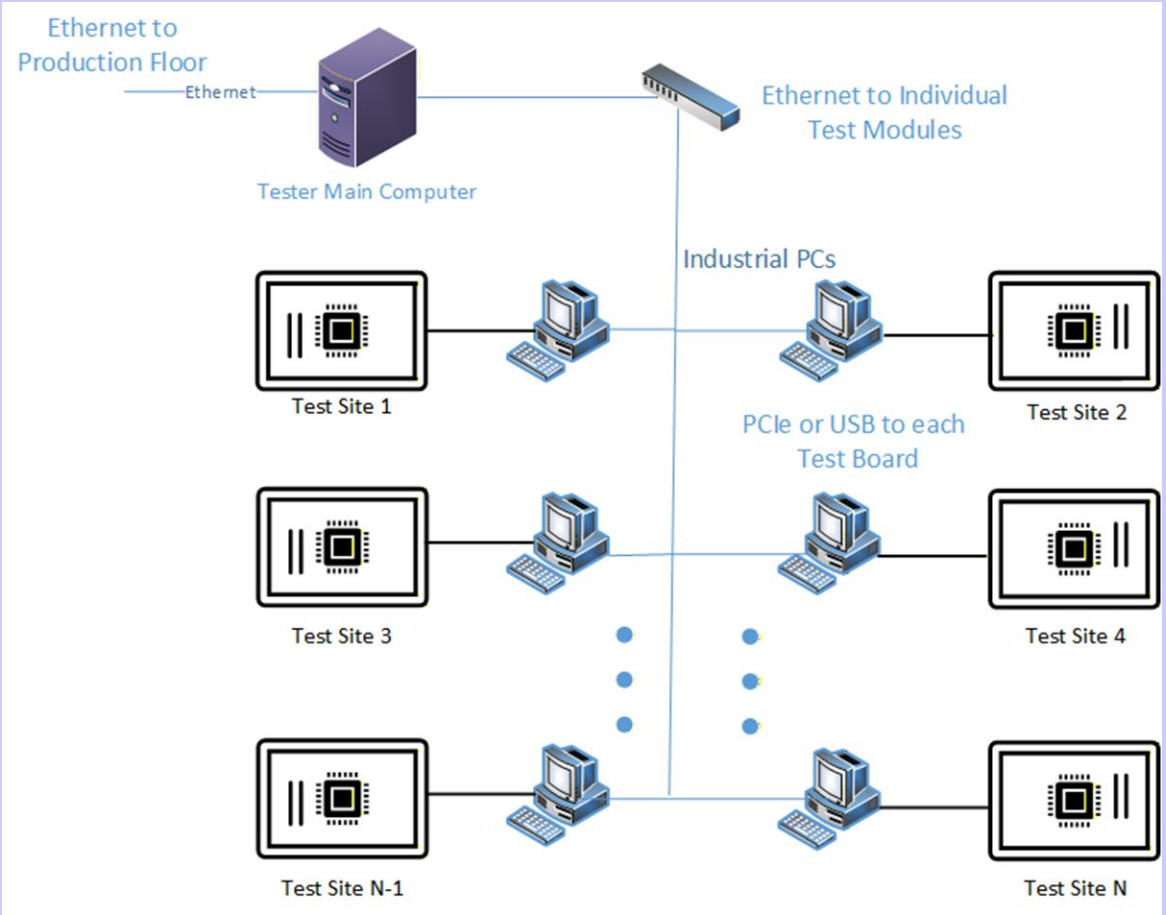


Networked for Test Site Control and Data Collection

Scaled for very high test site count

- Ethernet distributed to every supervisory controller for control & data collection
- Site controllers communicate via PCIe, USB, and other digital protocols to DUT
- Test computer interfacing to factory network and cloud-accessible AI/ML tools

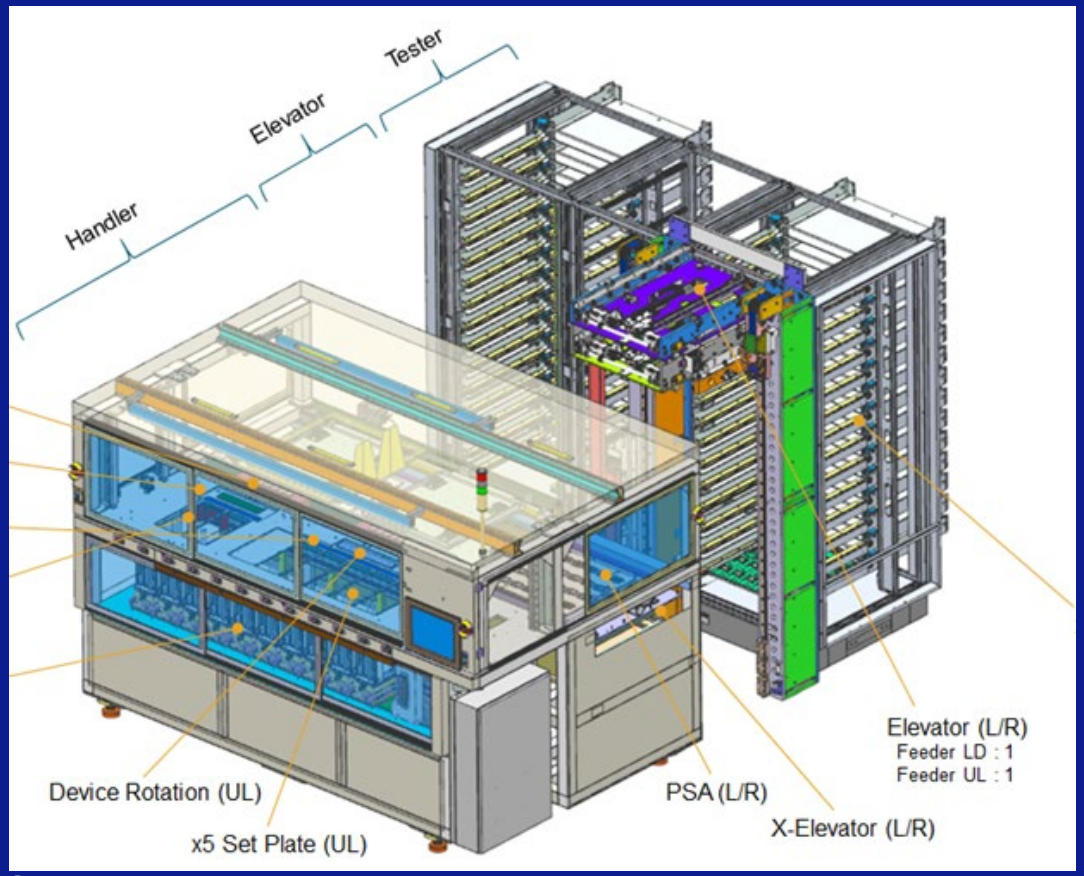
Internal Network Infrastructure



Automation for high test site count

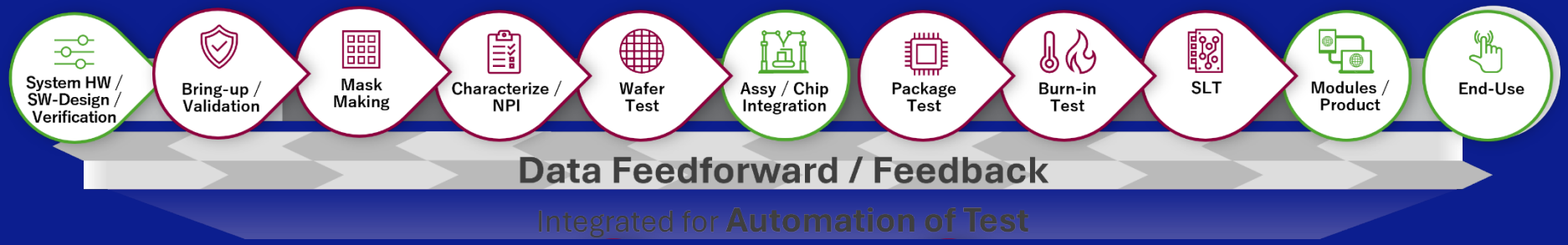
HVM Considerations:

- Long test times, so share handler
- Site count is high – go vertical to reduce floor space using elevators
- Socket force cancellation techniques
- Minimize indexing time
- Integrate with production floor tools/manufacturing execution systems



Source:
https://www.advantest.com/en/products/component-test-system/system-level-test-systems/7038/

Integrated Software Tools for the SLT Test Cell



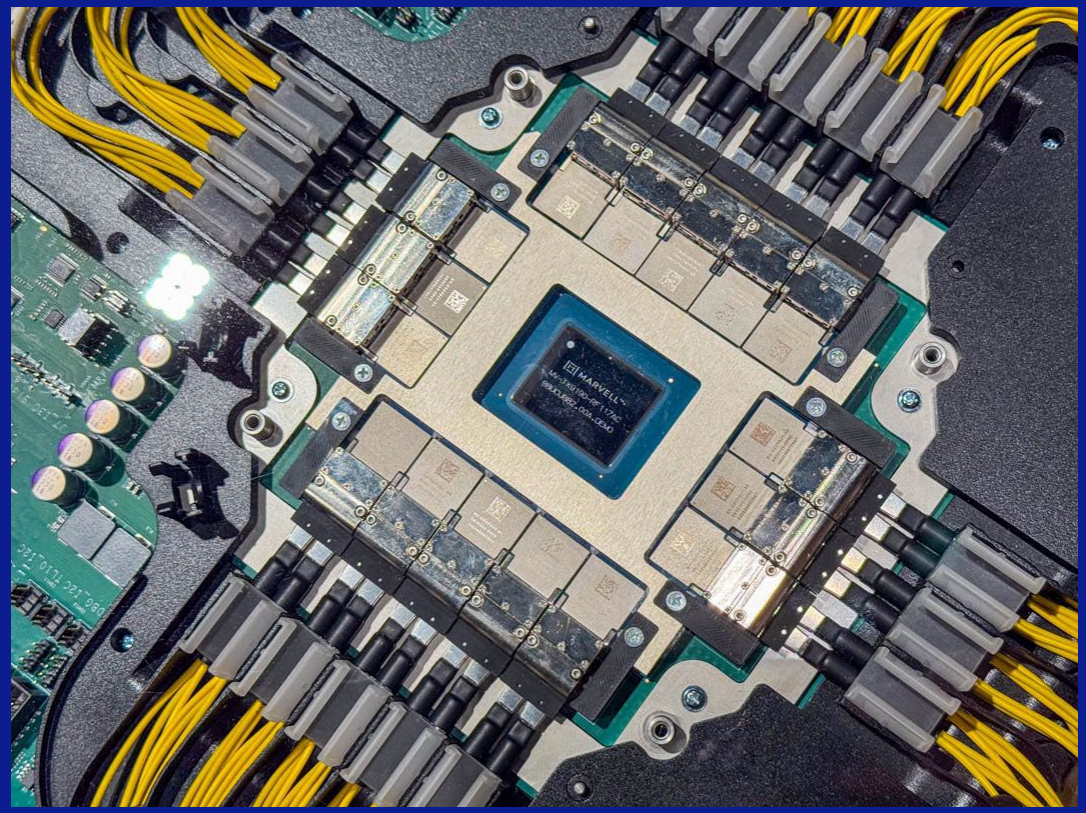
Device360	Studio360	Cell360	Facility360
DUT	Tester	Test Cell	Facility
Device Roundtrip Test Content SCAN Patterns	Test Program Hardware/Software Drivers High Parallelism	Distributed Lots Operator Instructions Handler + N Testers Thermal	Central Database/PCS Data Pipeline to ACS Tool Data & Device Data
SBC or COM-HPC	Tester PC	Cell PC	OSAT or ACS Server

ActivATE360™ Messaging Cluster | Integrated, Distributed & HPC | Handler | Hardware | Thermal

Advantest ACS

Upcoming Challenges

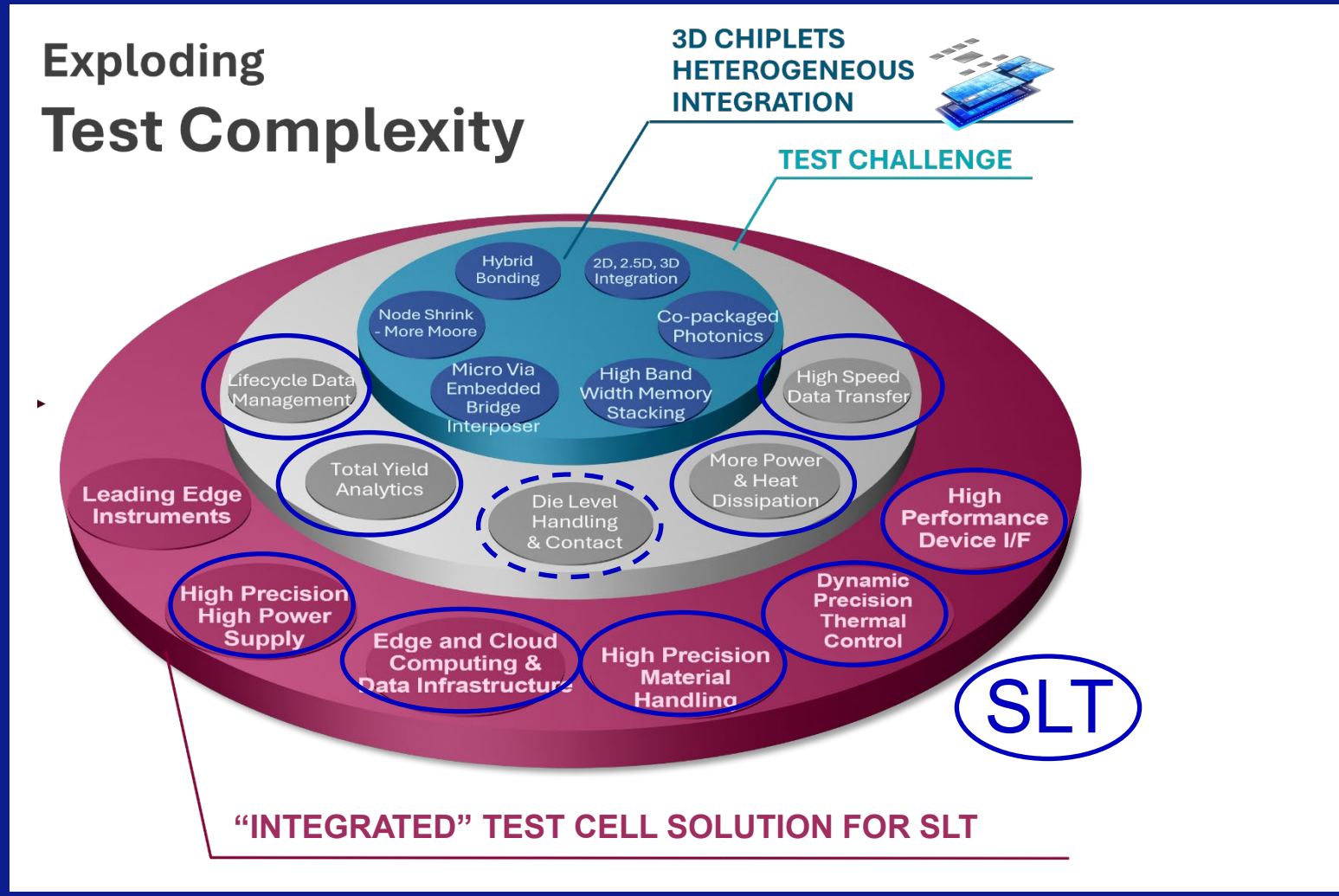
- Co-Packaged Optics
- Devices exceeding JEDEC tray standard dimension
- Power distribution to the test floor facility



Source: Marvel; TX9190 Switch at OCP 2025
https://www.servethehome.com/marvell-tx9190-liquid-cooled-cpo-switch-at-ocp-2025/

Conclusion: SLT in the Era of Complexity

- Multi-disciplinary challenges met
- Integrated test solutions
- Cost-Optimized
- Connected and ready for AI



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