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TestConX™

Archive

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Human touch versus AI: A simplified approach to PCB launch optimizations

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Problem

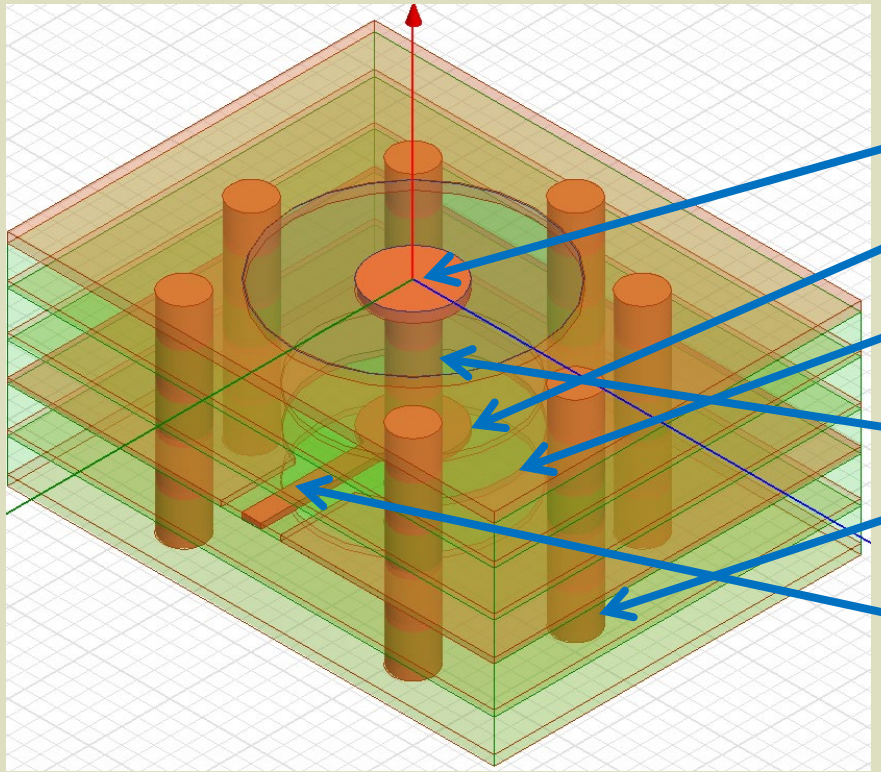
- Optimization of PCB parameters for a given interconnect between outside world and traces inside the PCB generally requires 3D FEA simulation and optimization to achieve the best results.

- Computations are repetitive and time consuming, tying up expensive resources and manpower for a configuration that is rather similar and not very complicated from case to case, yet has to be performed over-and-over-again.

- Therefore, a simple ‘pushbutton’ solution is proposed to quickly and simply arrive at a near optimal solution.

Problem geometry

- **Connector to PCB interface**

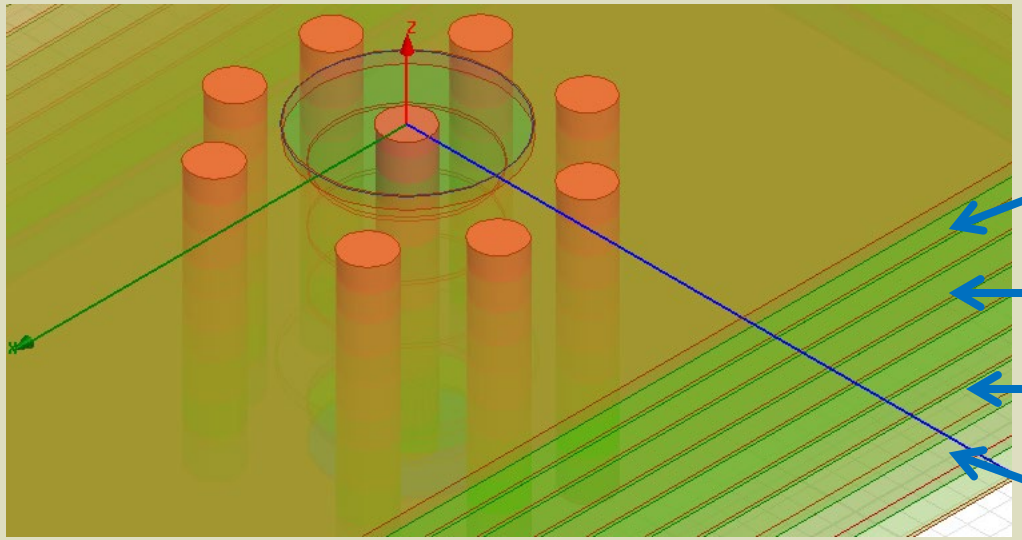


» Contact pad
» Capture pad
» Antipads
» Signal via
» Ground vias
» Signal trace

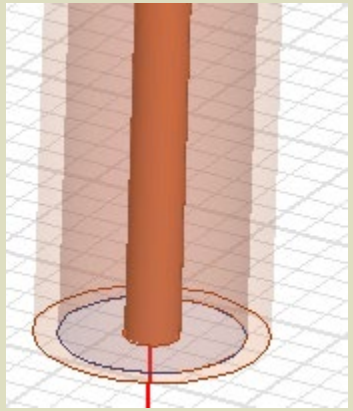
To be determined for optimization:
- Antipad diameter
- Ground via bolt circle diameter

Examination of PCB construction

- PCB stack:



This is essentially a coaxial configuration akin to that of a cable:



Difference in PCB stack:
Fields will be ‘bulging outward’ between ground plane layers around signal via.

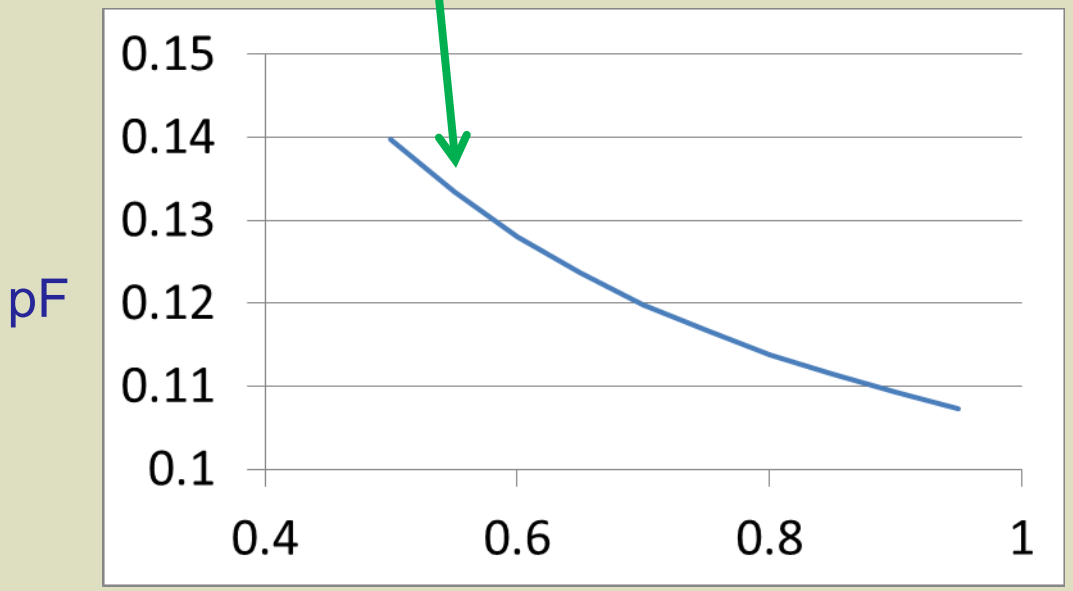
Therefore, unfortunately, it will not be possible to simply use coaxial cable impedance equations as a solution.

Previously discussed….

- Use of SPICE circuit simulator for optimization (see next slide from 2024 presentation)
- Still requires some software and an operator that understands FEA as well as circuit simulation
- The above-mentioned approach, presented at the 2024 TestConX Workshop, is geared toward speeding up the search and fine tuning an optimal performance solution.

From 2024 - ‘Repetitive’ 3D FEA

- Basic problem is relatively simple, yet we must compute a full 3D FEA run for each individual curve/solution over and over again.

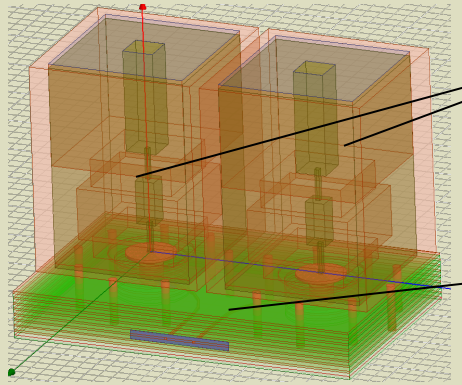


Example: Capacitance as a function of antipad diameter for a single pad/antipad combo (select dielectric constant)

It seems as though it should be possible to operate from ‘lookup tables’ instead.

From 2024 - Potential solution: SPICE simulation

- Establish a SPICE equivalent circuit for the chosen architecture.



Coaxial cable* to PCB connector

PCB with ***stripline**** on inner layers

- Identify parameters of interest, e.g. various L,C components.
- Define possible range of these parameters.
- Establish SPICE equivalent circuit for chosen architecture.
- ***Run Monte Carlo*** analysis and inspect results.

****analytical solutions are available, no 3D FEA required***

Current approach vs. Envisioned

Currently used: FEA

- Very competent solution
- Expensive
  - Initial acquisition
  - Annual maintenance
  - Optimization option
  - Hardware requirements
  - Operator qualifications
- Slow
  - CPU/RAM
  - Occasional non-convergence

Envisioned:

Spreadsheet or similar software

- Affordable
  - Acquisition
  - Basic EE understanding
  - Low/no maintenance
  - No special hardware necessary even for complex problems
- Fast
  - Low CPU requirements
  - Low RAM needs

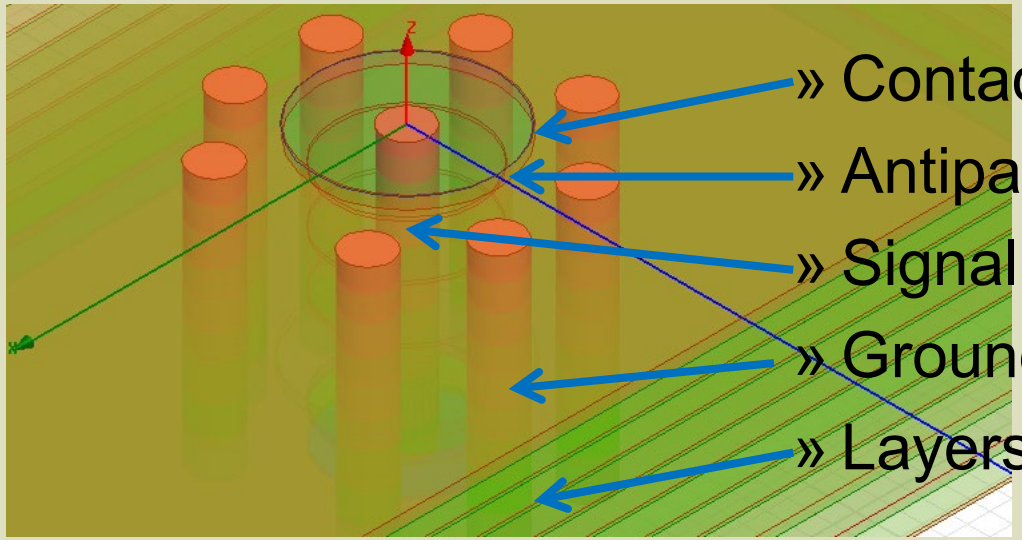
Next steps

- Develop datasets that span anticipated parameter value ranges
  - Parameters to be varied are Dk and dielectric layer thicknesses
- Determine upper and lower limits for these parameters

- Run 3D FEA optimizations (one each) to identify optimal antipad size for selected parameters
- Set up spreadsheet database for parameter ranges
- Develop macros and interpolations that automatically determine proper antipad sizes for a given customer supplied PCB stack data input.

Lookup table creation from 3D FEA models

- PCB stack:

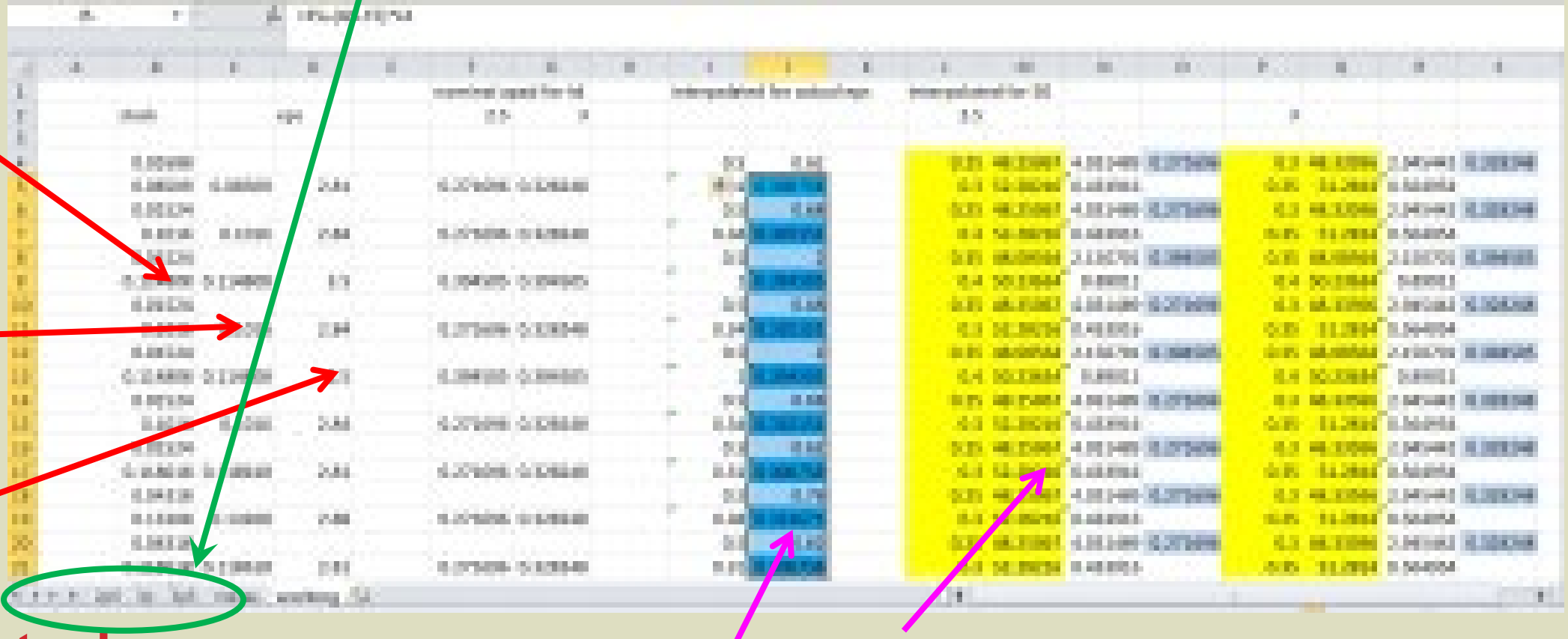


To be extracted:

- Antipad sizes for desired stack impedance

- Antipad sizes should be determined for each individual layer for optimal results.
- If the stack is reasonably uniform it becomes possible to model this as one piece (i.e.one pad size).

Lookup table reward: Spreadsheet output

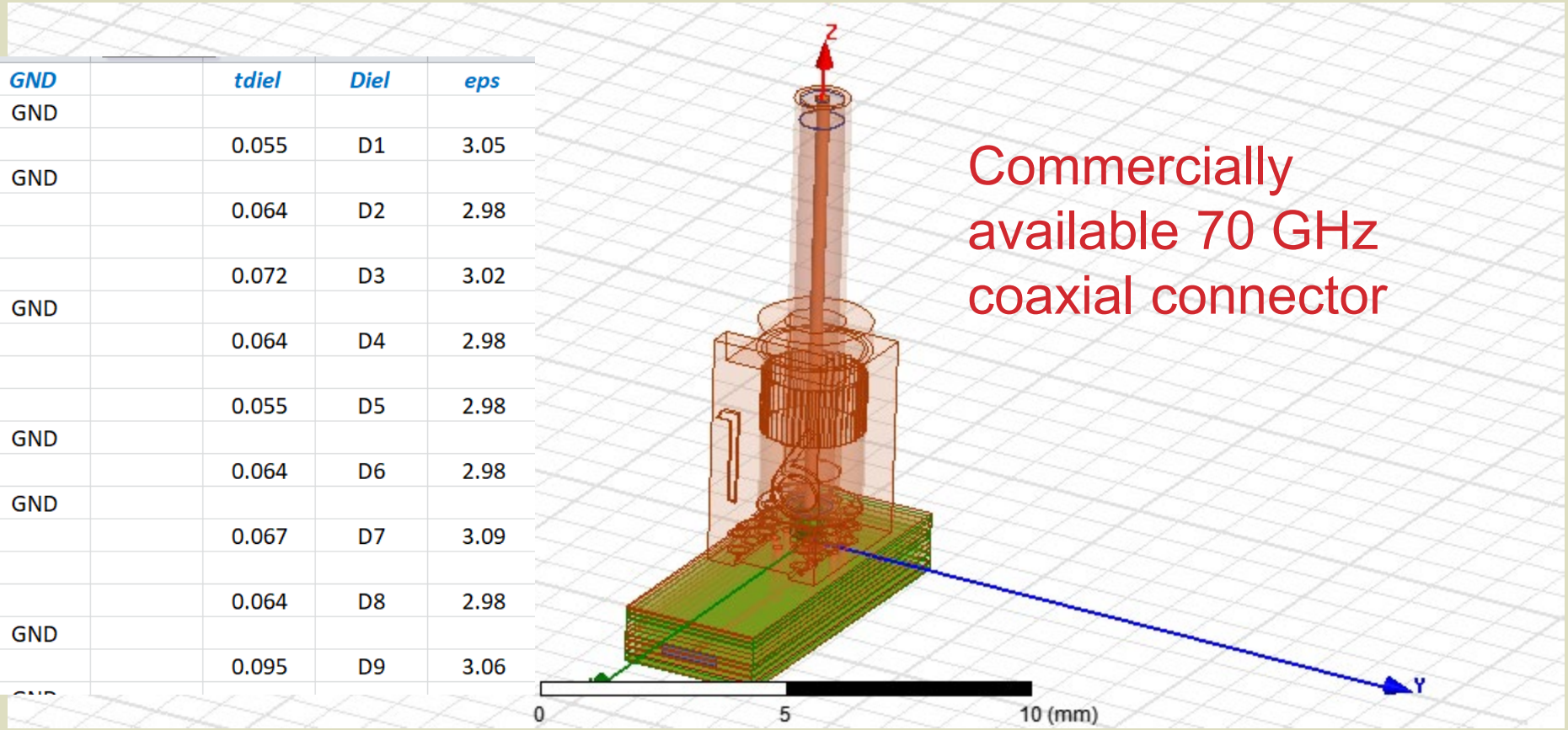


PCB stackup:
Customer provided input

Processing of input data generates a set of antipad recommendations

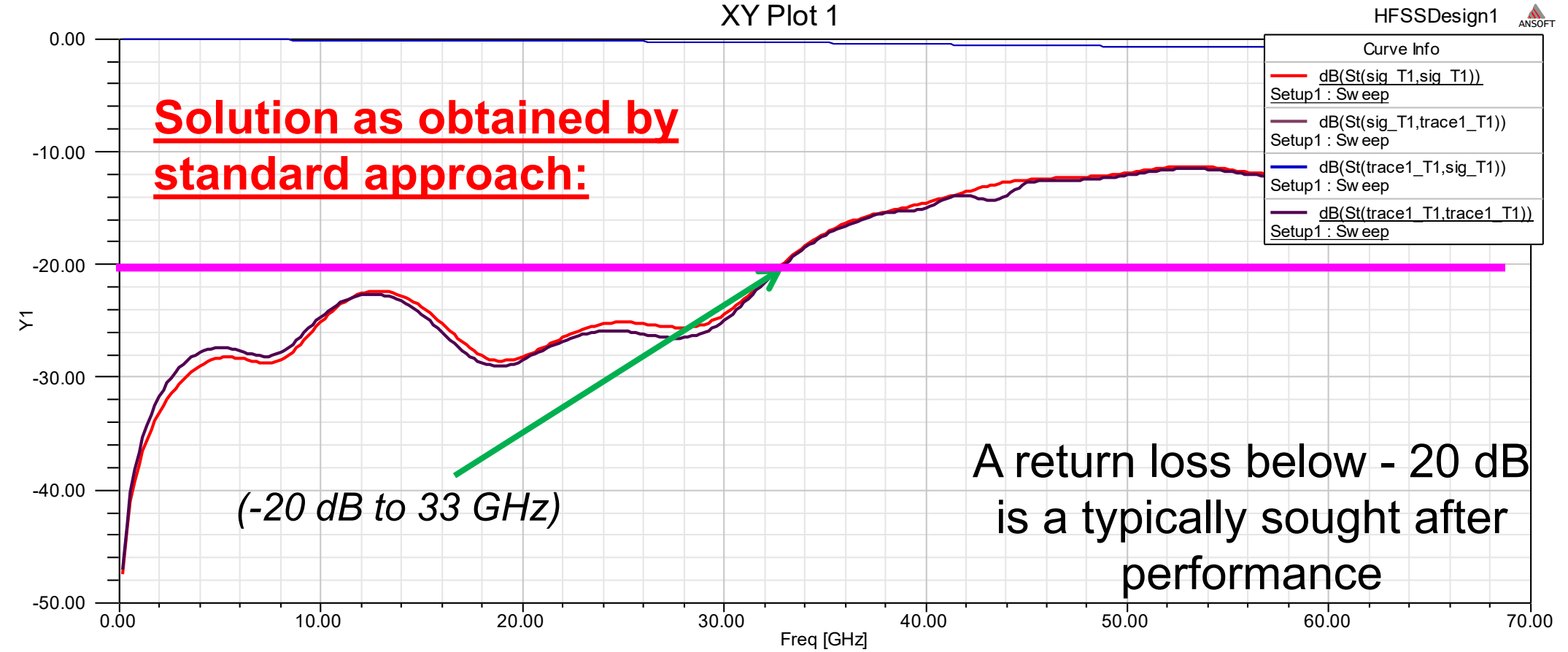
Example

tmet	Cu	sig	GND		tdiel	Diel	eps
0.061	L1		GND				
					0.055	D1	3.05
0.014	L2		GND				
					0.064	D2	2.98
0.030	L3	sig					
					0.072	D3	3.02
0.014	L4		GND				
					0.064	D4	2.98
0.014	L5	sig					
					0.055	D5	2.98
0.014	L6		GND				
					0.064	D6	2.98
0.014	L7		GND				
					0.067	D7	3.09
0.030	L8	sig					
					0.064	D8	2.98
0.061	L9		GND				
					0.095	D9	3.06

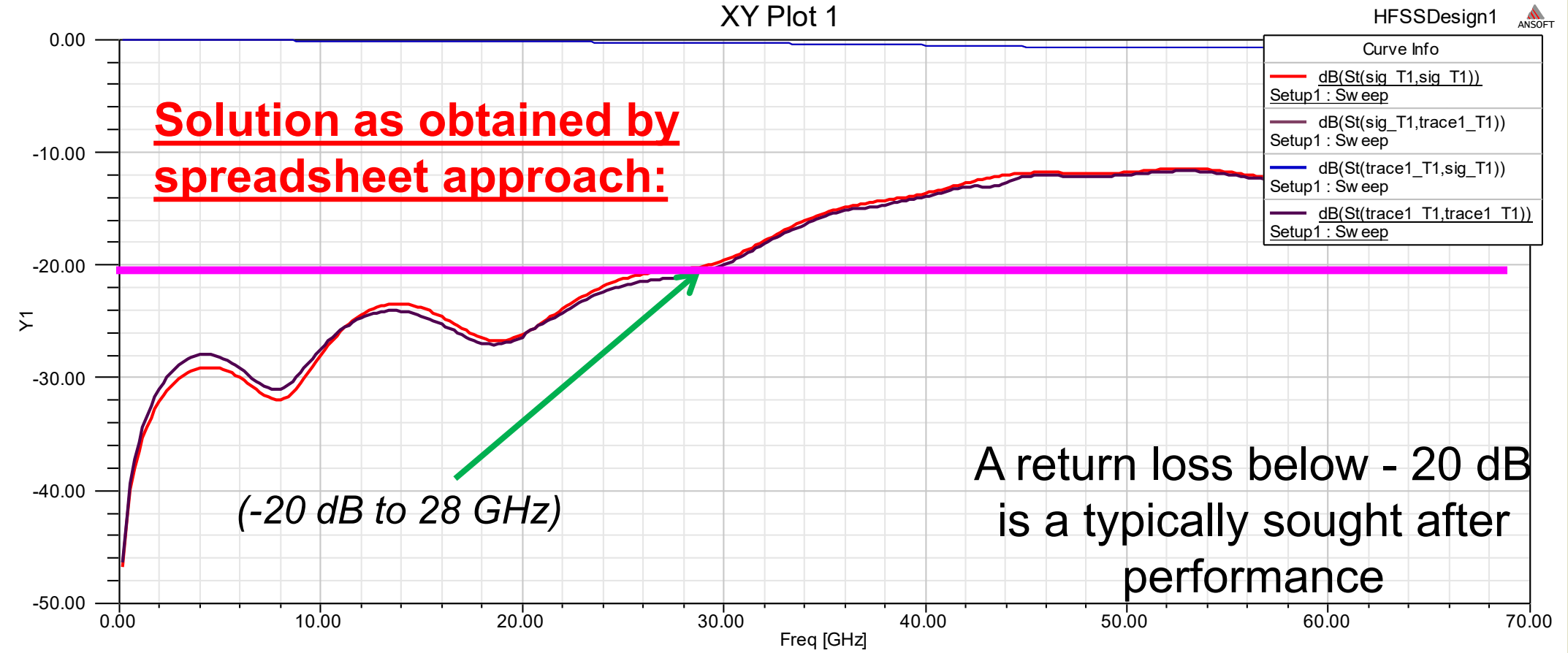


Commercially available 70 GHz coaxial connector

Return loss S11

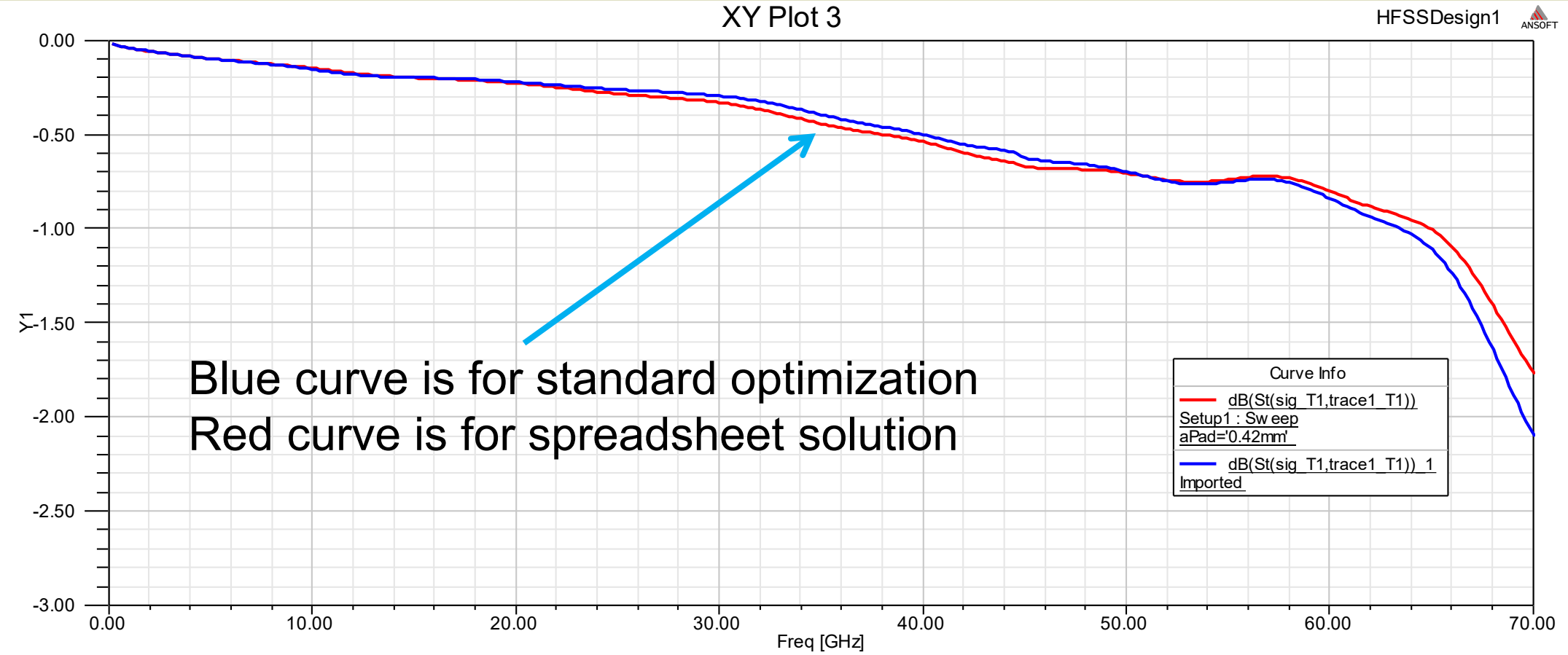


Return loss S11



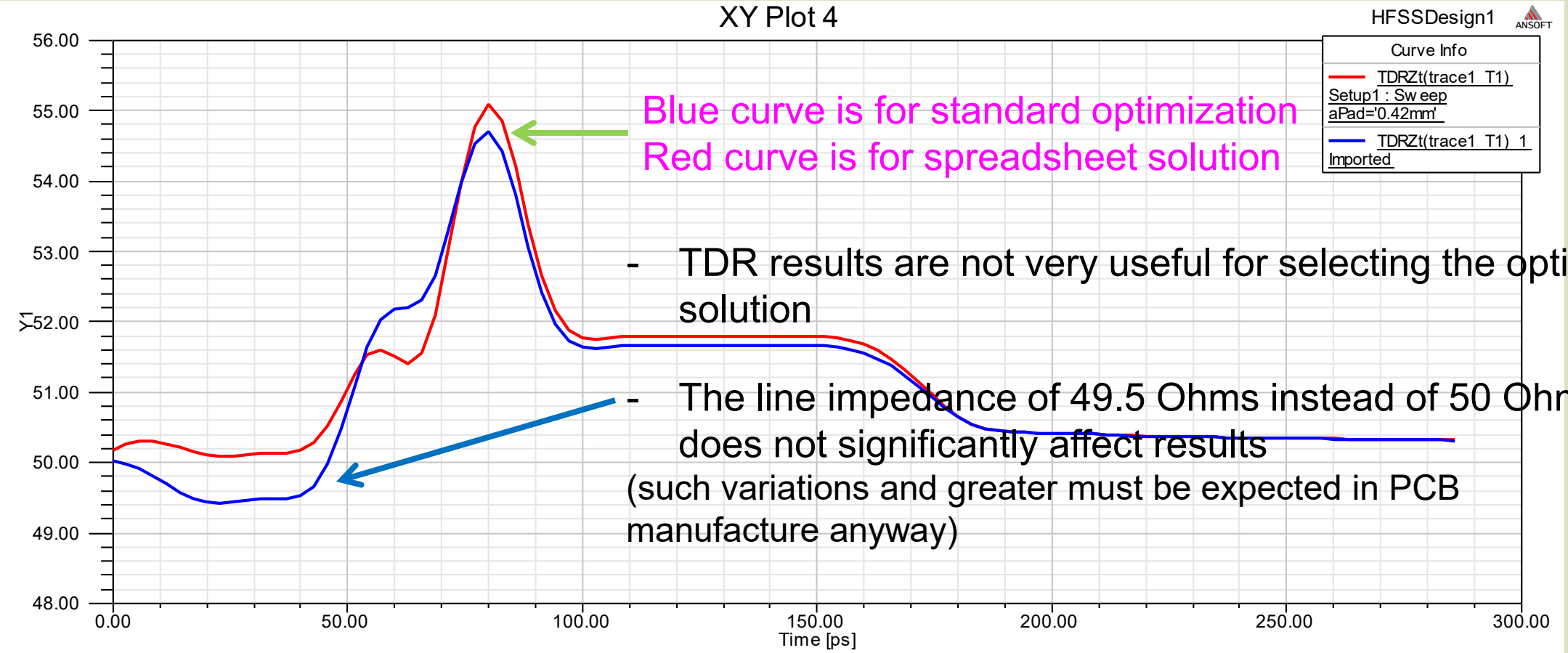
Insertion loss S21

Corresponding S21 sets to the S11 solution sets above



Time Domain Reflectometry

Corresponding time domain reflection measurement set to the S11 solution sets



Blue curve is for standard optimization
Red curve is for spreadsheet solution

- TDR results are not very useful for selecting the optimal solution
- The line impedance of 49.5 Ohms instead of 50 Ohms does not significantly affect results

(such variations and greater must be expected in PCB manufacture anyway)

Comments

- 3D FEA models for individual cases must be carefully set up in order to arrive at accurate data tables.
- Correlation between spreadsheet and full 3D FEA optimized models has been demonstrated on a limited case basis to date.
- Failure to execute the 3D element models properly will lead to failure of the spreadsheet method.

Pros and Cons

- Pros
  - Very fast generation of very large solution numbers
  - A large number of variable parameters may be specified
  - Random parameter selections offers good chances that a ‘near best’ or the best solution will be present in the output dataset
- Cons
  - Setup requires a good understanding of how to generate a valid equivalent circuit
  - A large number of a priori 3D simulations may be required to develop a comprehensive database that allows for quick parameter range selection

Conclusions

- Optimization of PCB parameters is mandatory to achieve good performance at high frequencies.
- Establishing lookup tables for antipad size selection via 2 1/2D or 3D FEA will allow for rapid selection of design parameters for near optimal launches into PCBs via interpolation from data tables.
- Experience with proper parameter selection and knowledge of their possible ranges will further enhance the design toward best case results.

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