TWENTY-SEVENTH ANNUAL

TestConX™

Archive

DoubleTree by Hilton
Mesa, Arizona
March 1-4, 2026

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Next generation Test Socket Evaluation, Mechanical, Thermal, Signal Integrity, and Device Performance Validation

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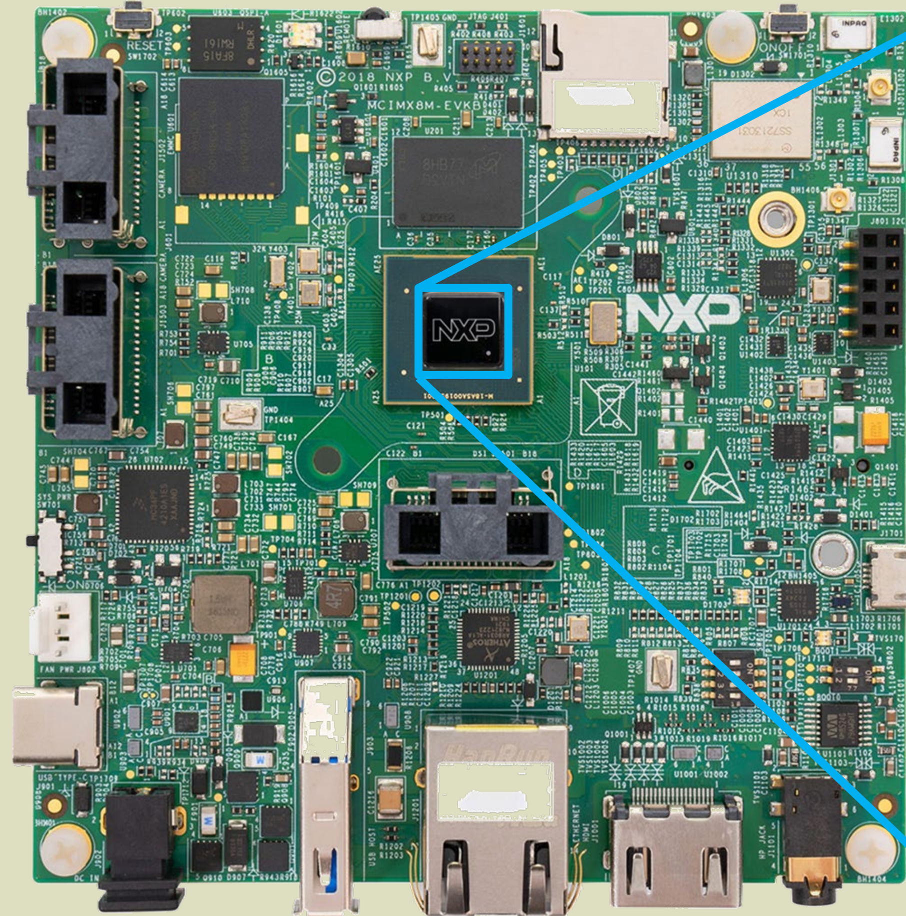
Mesa, Arizona • March 1–4, 2026

Example Micro-Processor and Environment



Core Complex 1
- 4 x ARM® Cortex®-A53 core
- 32 KB L1-I
- 32 KB L1-D
- 1 MB L2 with ECC

Core Complex 2
- 2 x Cortex-A72 core
- 32 KB L1-I
- 32 KB L1-D
- 1 MB L2 with ECC

Core Complex 3
- 1 x Cortex-M4F
- 16 KB L1 I and D
- 256 KB SRAM
- 1 x I^{2}C, 1 x UART, 1 x GPIO

Core Complex 4
- 1 x Cortex-M4F
- 16 KB L1 I and D
- 256 KB SRAM
- 1 x I^{2}C, 1 x UART, 1 x GPIO

Multimedia

GPU
- 1 x 4-8 Shader OGL, Vulkan VX Extensions
- bridge
- 1 x 4-8 Shader OGL, Vulkan VX Extensions

VPU
- Video: h.265 dec 4K/2K h.264 dec/enc 1080p

Display
- Display Processor with SafeAssure®
- Display Processor with SafeAssure

Audio
- 1 x HiFi 4 DSP
- 32 KB I
- 48 KB D
- 64 KB TCM

Display and Camera I/O
- 1 x MIPI DSI (4-lanes)
- 1 x MIPI DSI (4-lanes)
- 1 x LVDS Tx
- 1 x LVDS Tx
- 1 x HDMI 2.0a/eDP 1.4/DP 1.3 with HDCP 2.2
- 1 x HDMI 1.4 Rx with HDCP 2.2
- 1 x MIPI CSI (4-lanes)
- 1 x MIPI CSI (4-lanes)

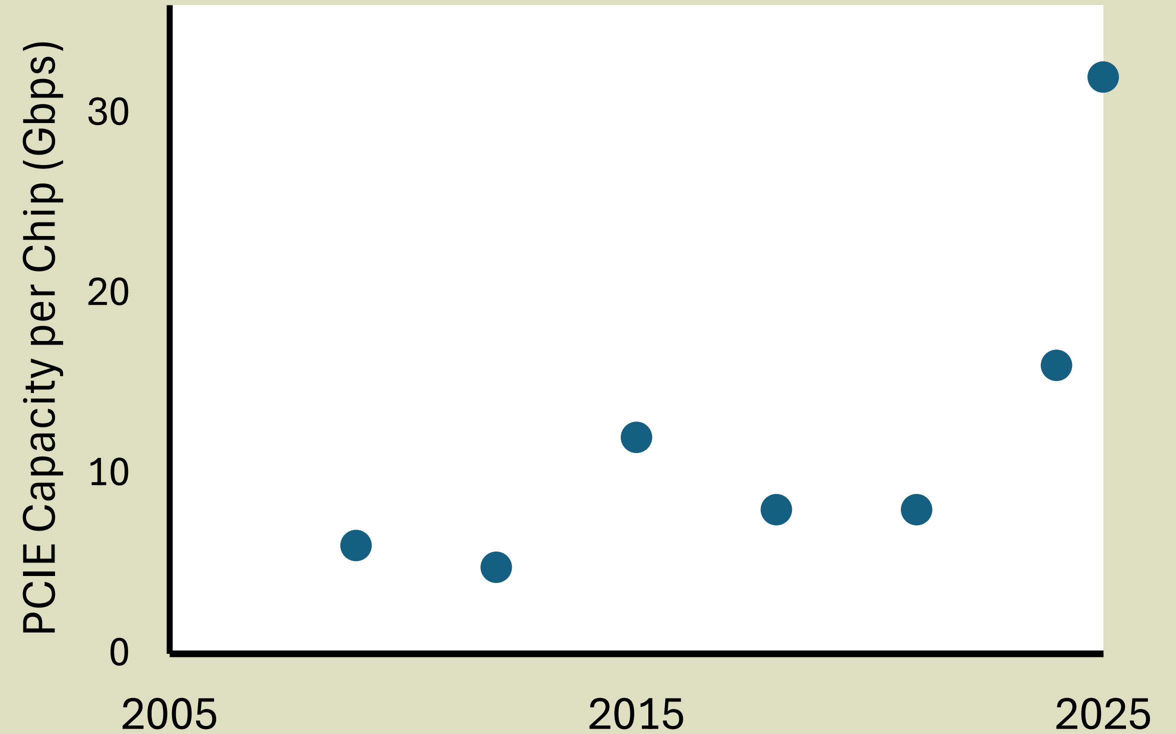
Memory
- LPDDR4 (1600 MHz)
- DDR4 (1200 MHz)
- 1 x QSPI
- 1 x QSPI
- 1 x FPGA Interface (QSPI based)
- 3 x SD 3.0/eMMC 5
- NAND (SLC/MLC) – BCH62

Security
- HAB, SRTC, SJTAG, TrustZone®
- AES256, RSA4096, SHA-256
- 3DES, ARC4, MD-5
- Flashless SHE, ECC
- Tamper, Inline Enc Engine

System Control
- Power Control, Clocks, Reset
- BootROMs
- PMIC interface (dedicated I^{2}C)
- Domain Resource Partitioning

Connectivity
- PCIe 3.0 with L1 substate – 1-lane
- PCIe 3.0 with L1 substate – 1-lane
- 1 x SATA3 and PHY 1-lane (or PCIe with L1 substate 1-lane)
- USB3 dual-role and PHY
- USB2 OTG and PHY USB2 Host/HSIC
- 2 x 1 Gb Ethernet+AVB
- 3 x CAN FD
- MLB150
- 1 x S/PDIF Tx/Rx, 1 x ASRC
- 2 x ESAI, 4 x I^{2}S/SAI
- 5 x I^{2}C High-Speed with DMA
- 8 x I^{2}C Low-Speed (no DMA) Attached to Camera, Display IO Available if Cam/Disp not used
- 4 x SPI
- 8 x PWM
- 2 x 12-bit ADC (16-Channel)
- 5 x UART

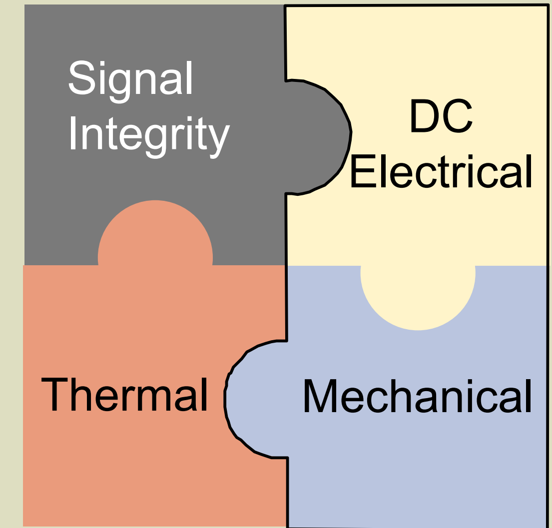
Die Communication Trends



- Chip designs are getting more challenging

Objective

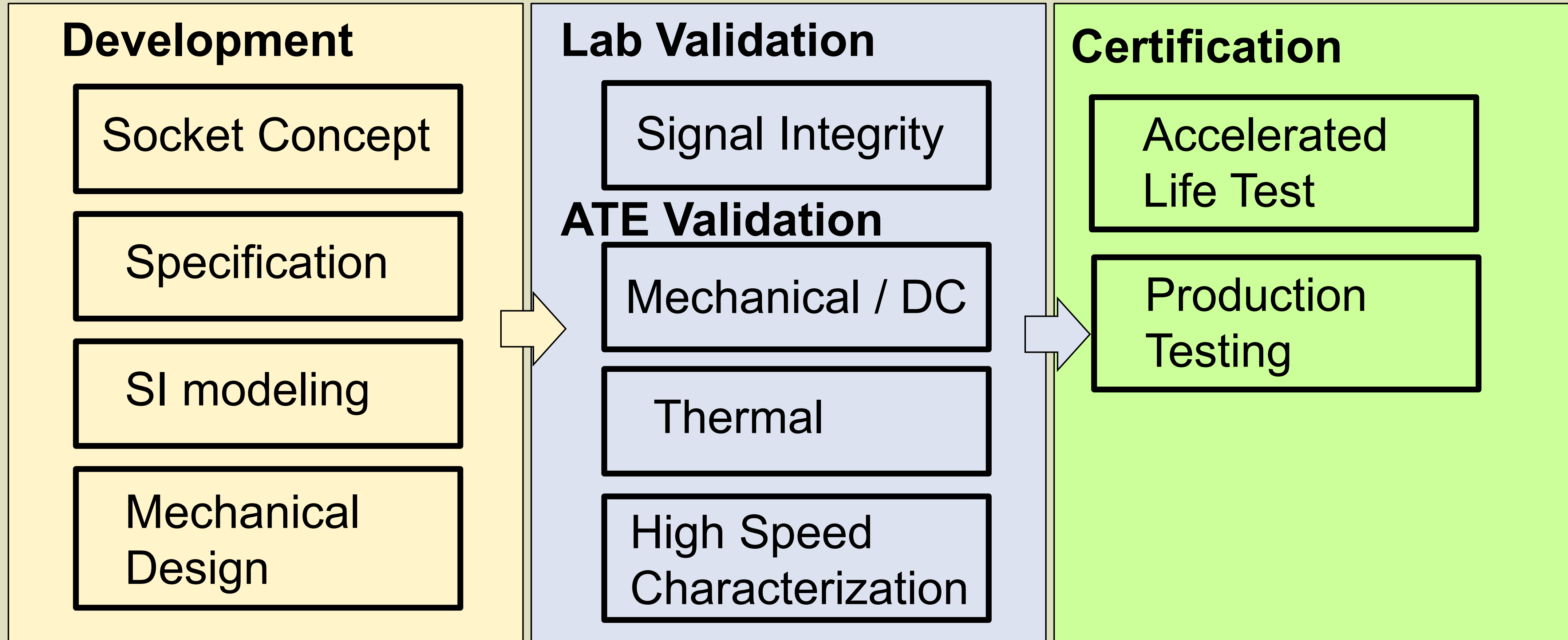
- Quantify and compare key aspects of socket performance in a highspeed digital application



Test Application

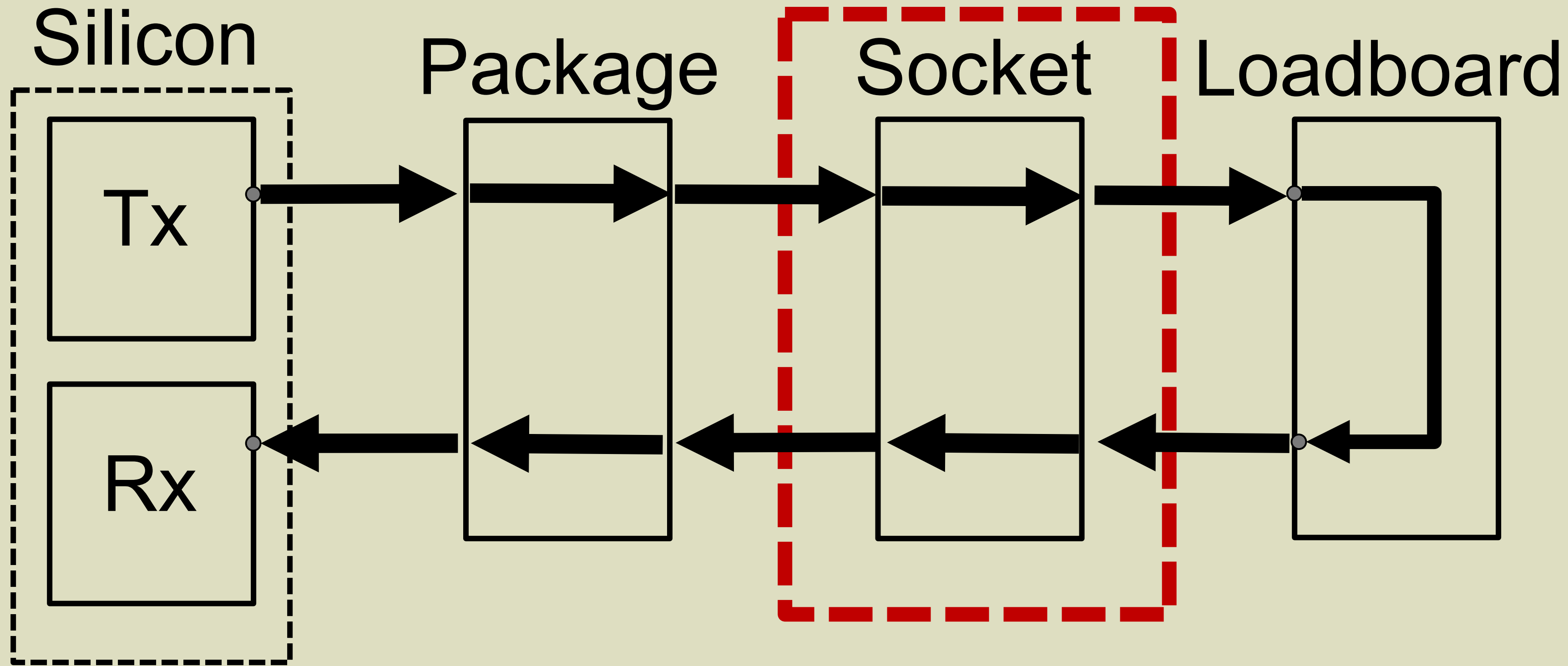
- High volume production final test
- 5 nm Automotive product
- Lidded Flip Chip BGA
- Multiple high speed off chip communication protocols
- Significant digital content
- Hundreds of IO
- Approximately 1000 contacts
- PCIe 4.0
- LPDDR4X

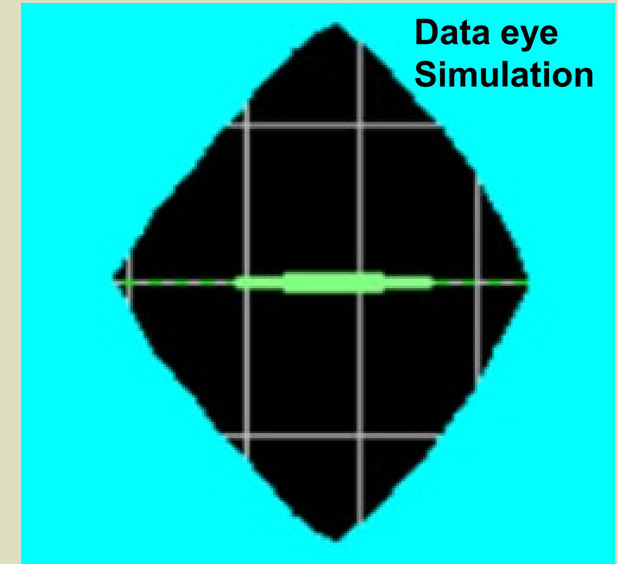
Socket Technology Early Life Cycle



SIGNAL INTEGRITY (SI)

Loopback Test Transmission Line



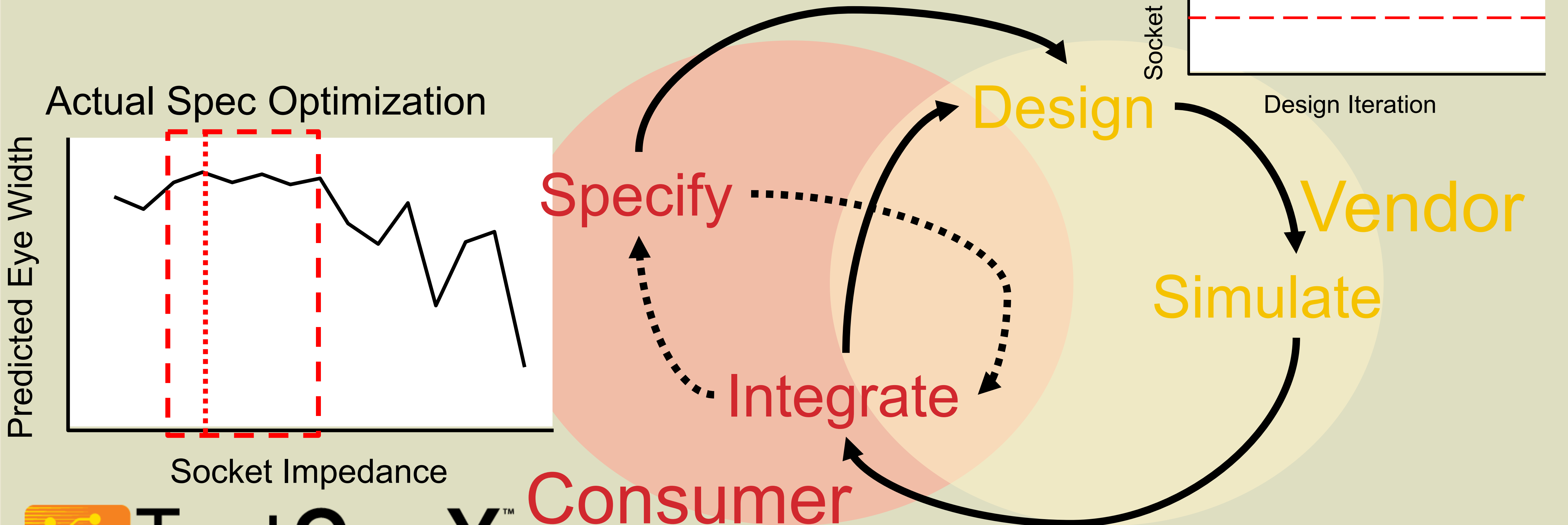


Data eye simulation

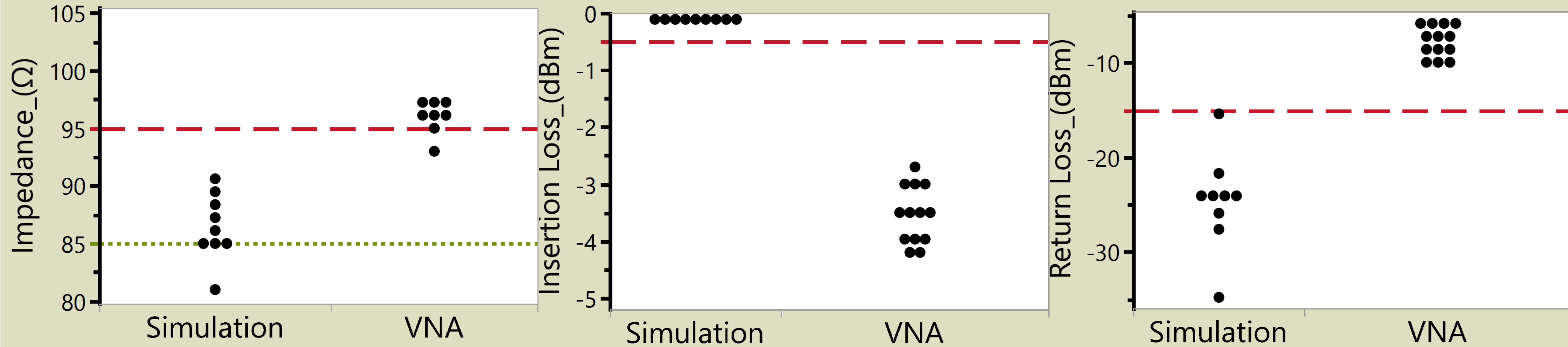
- Models needed for each component
- Interfaces and random effects are neglected

Socket Development

- Collaborative and iterative cycle



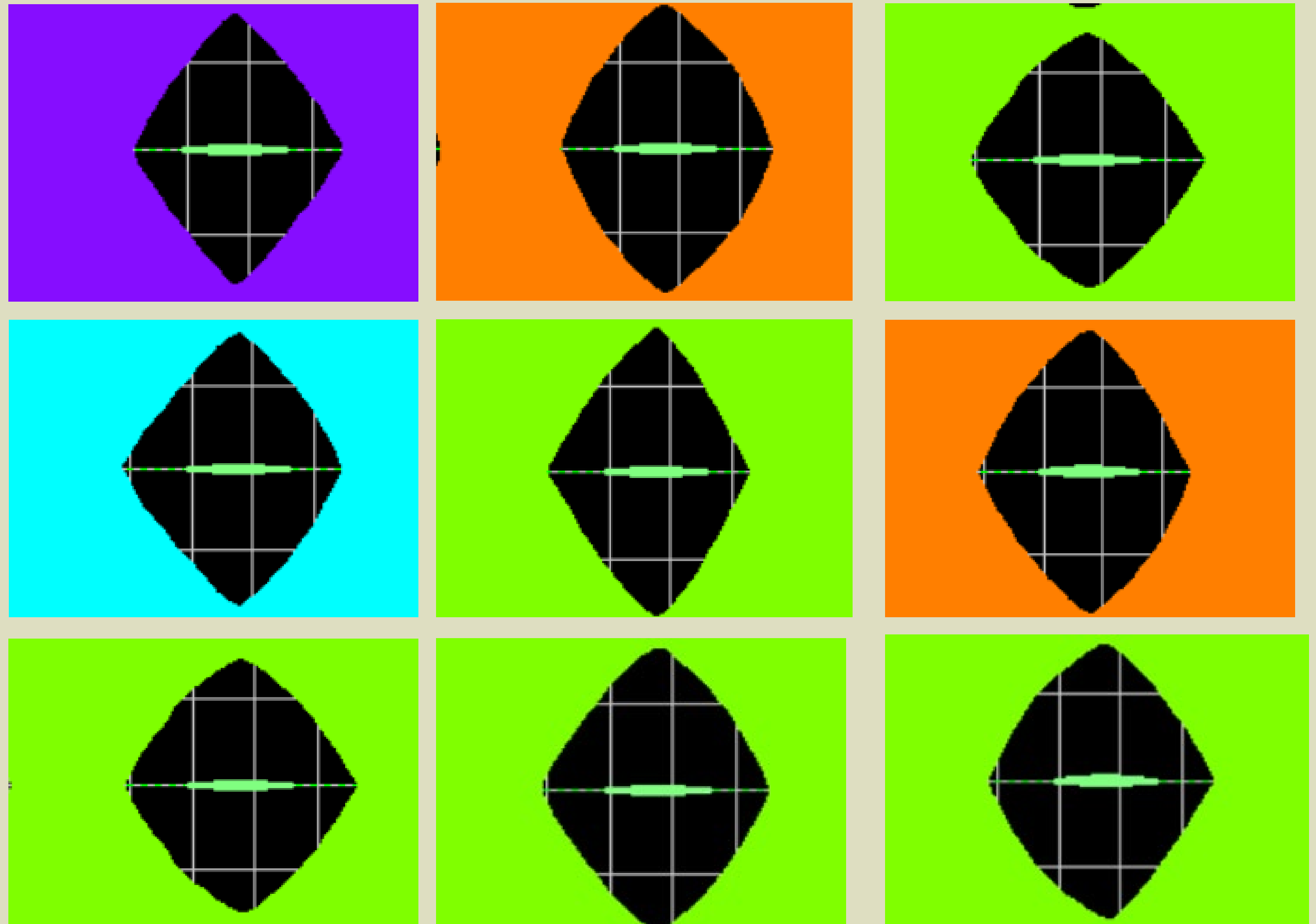
Measured Signal Integrity



- VNA values include loadboard effects
- Impedance is socket observed within the system

Measurement Based Data Eye Simulation

- Integrate VNA measurements with silicon models
- Approximate data eye by socket type



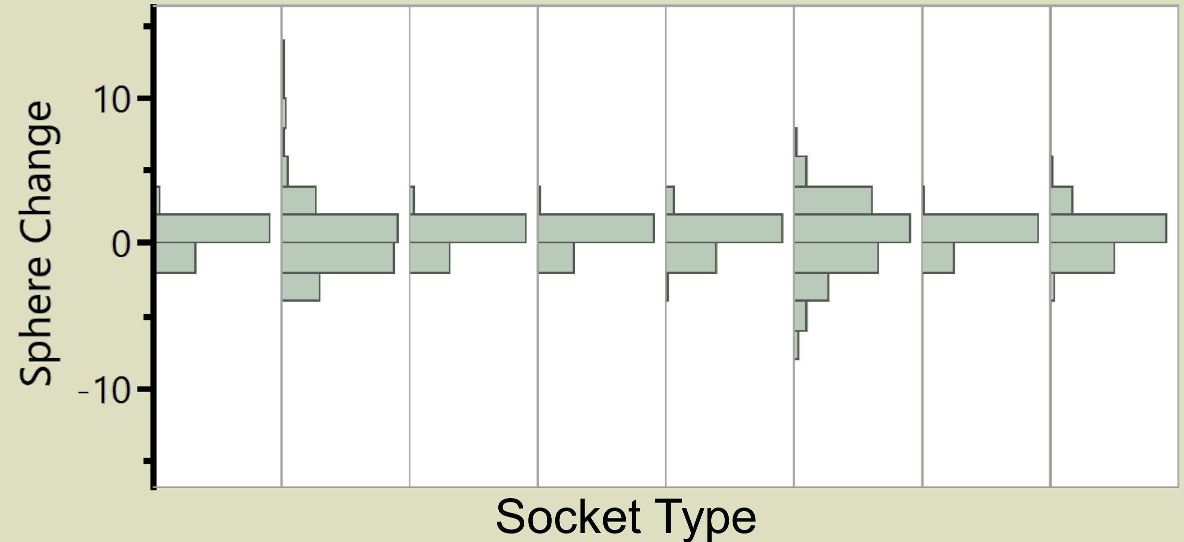
Eye approximation for different socket technologies

ATE SOCKET VALIDATION

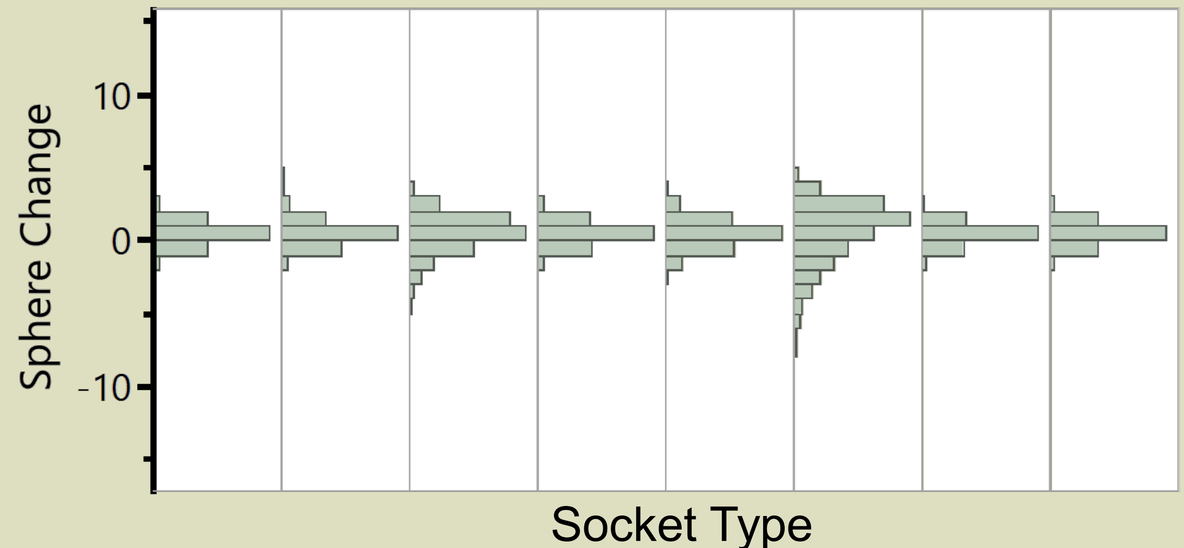
Solder Ball Deformation

- Some sockets deform solder balls
- Hot and cold behave differently

-45°C



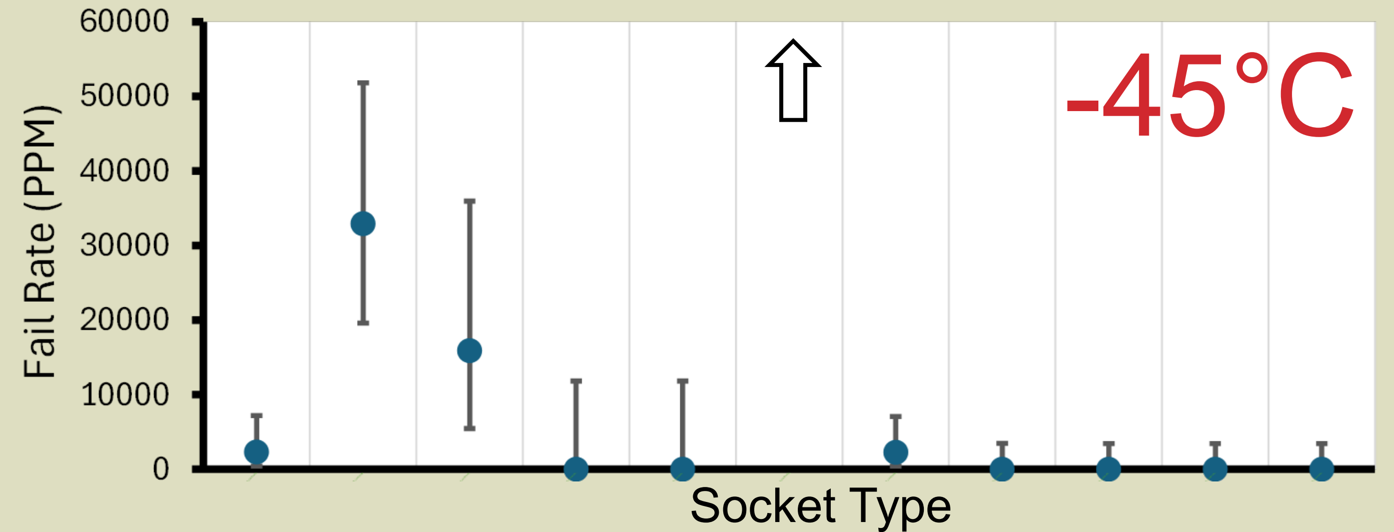
125°C

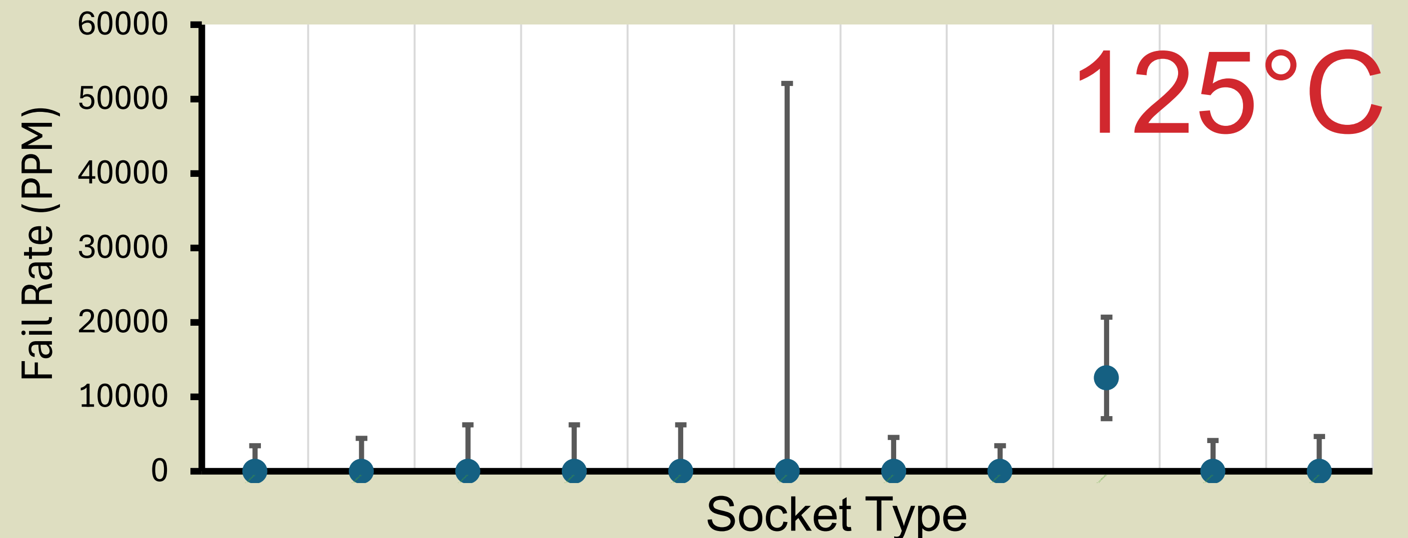


ICOS analysis of spheres before and after 7 inserts

Continuity

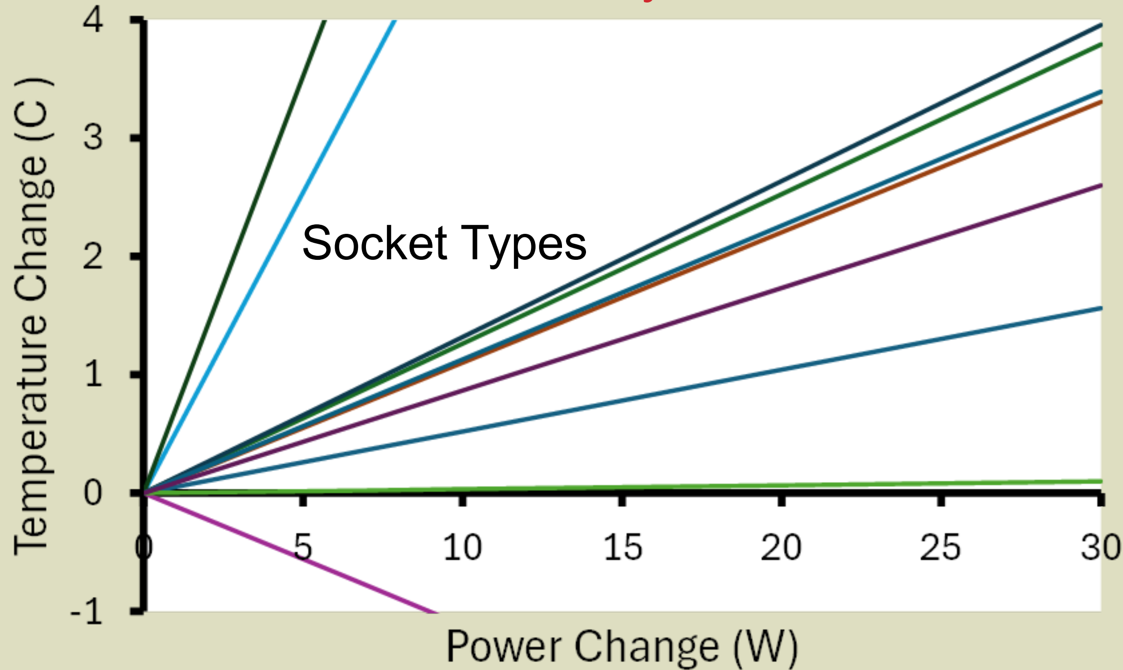
- Clear difference in socket performance
- Temperature effect not always consistent

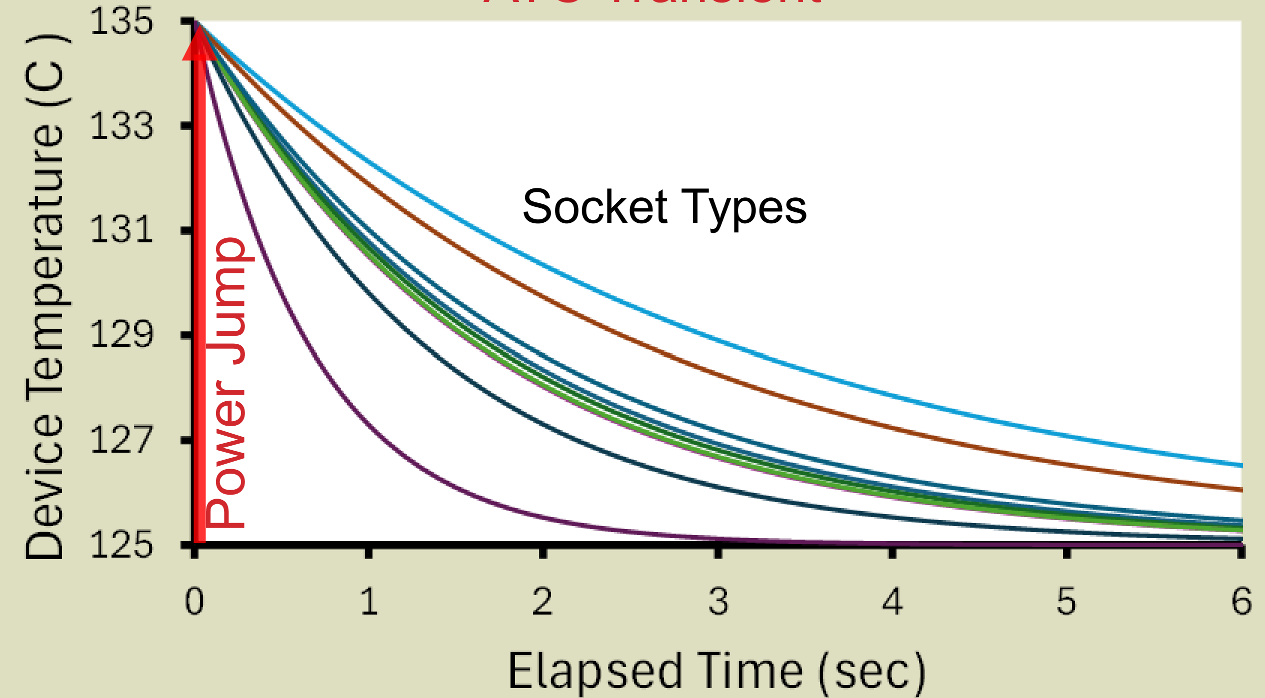




- ~900 devices tested
- Some cells aborted early

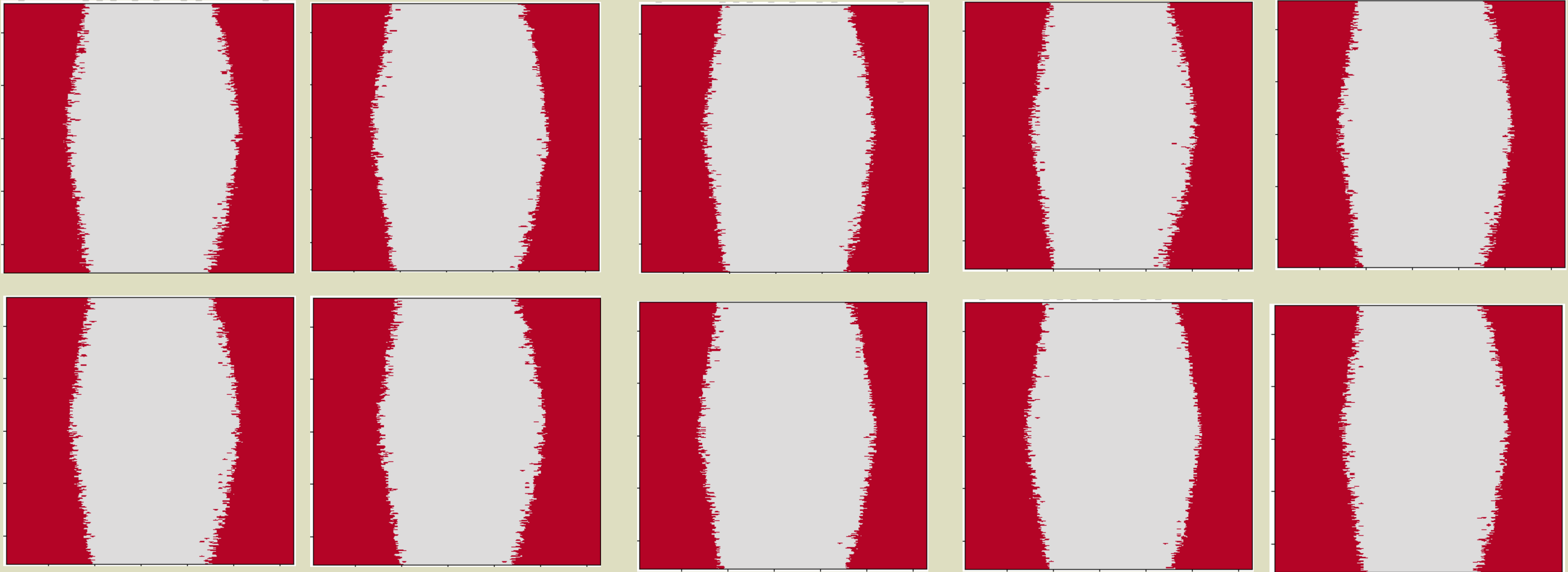
Thermal Performance





- Socket design impacts thermal performance
- Same handler settings used for all sockets

ATE Data Eye Characterization

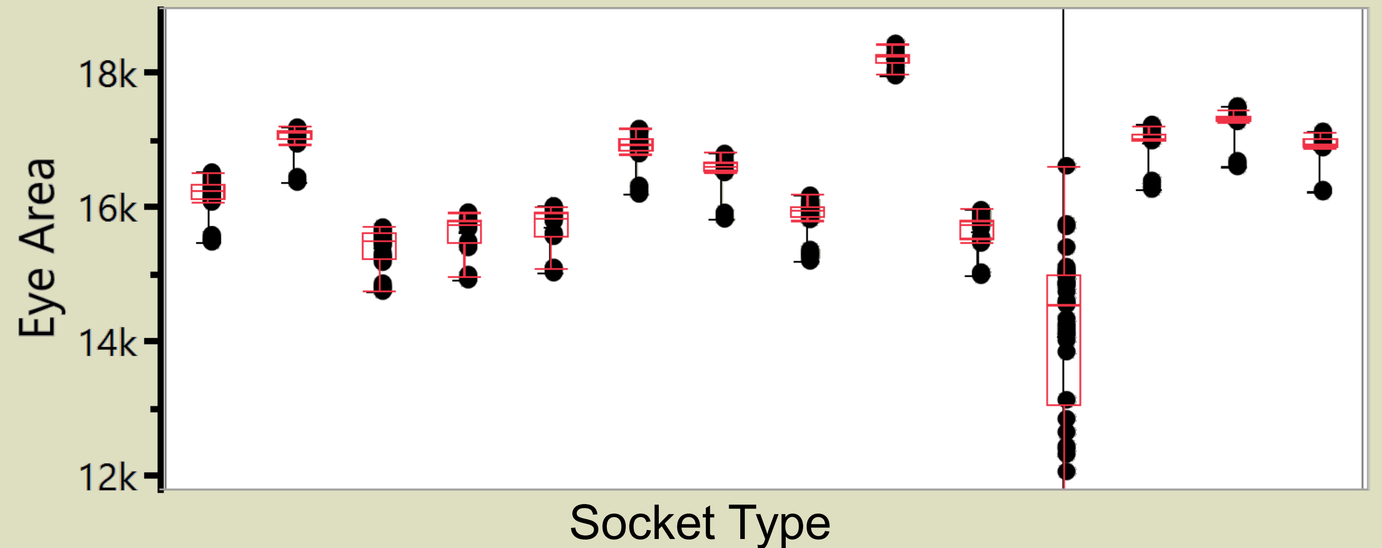


- Similar test conditions different socket technologies
- Data eye amplitude is clipped by CZ routine

PCIe Data Eye Area

- Socket effect is slightly larger than die variation

- Plenty of margin with most designs



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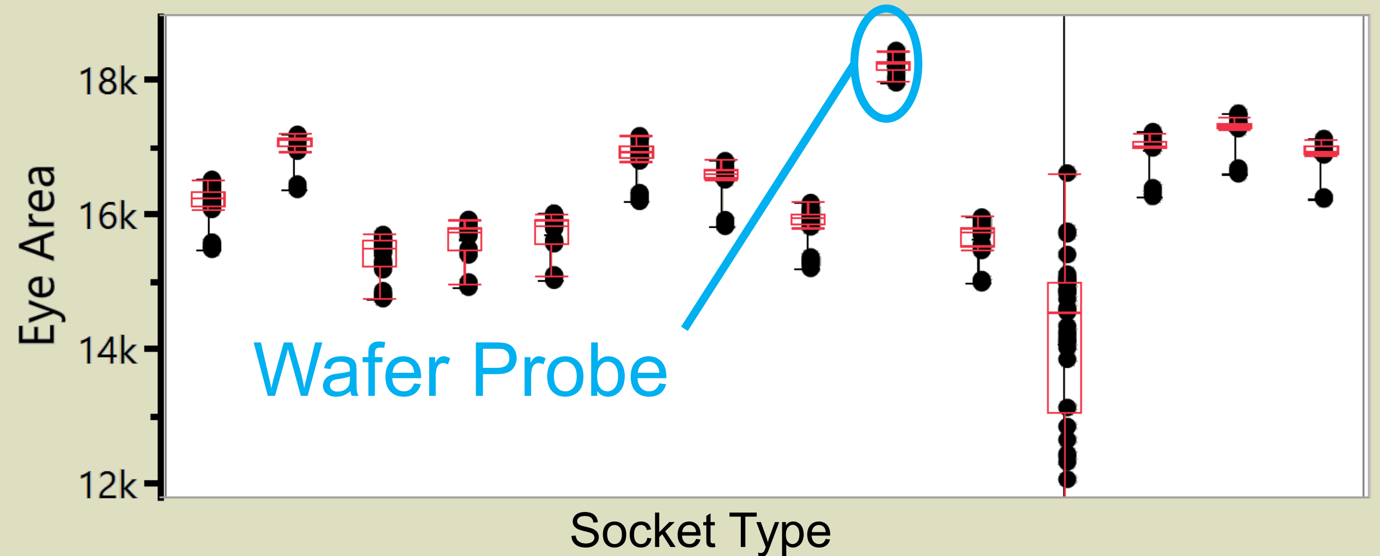
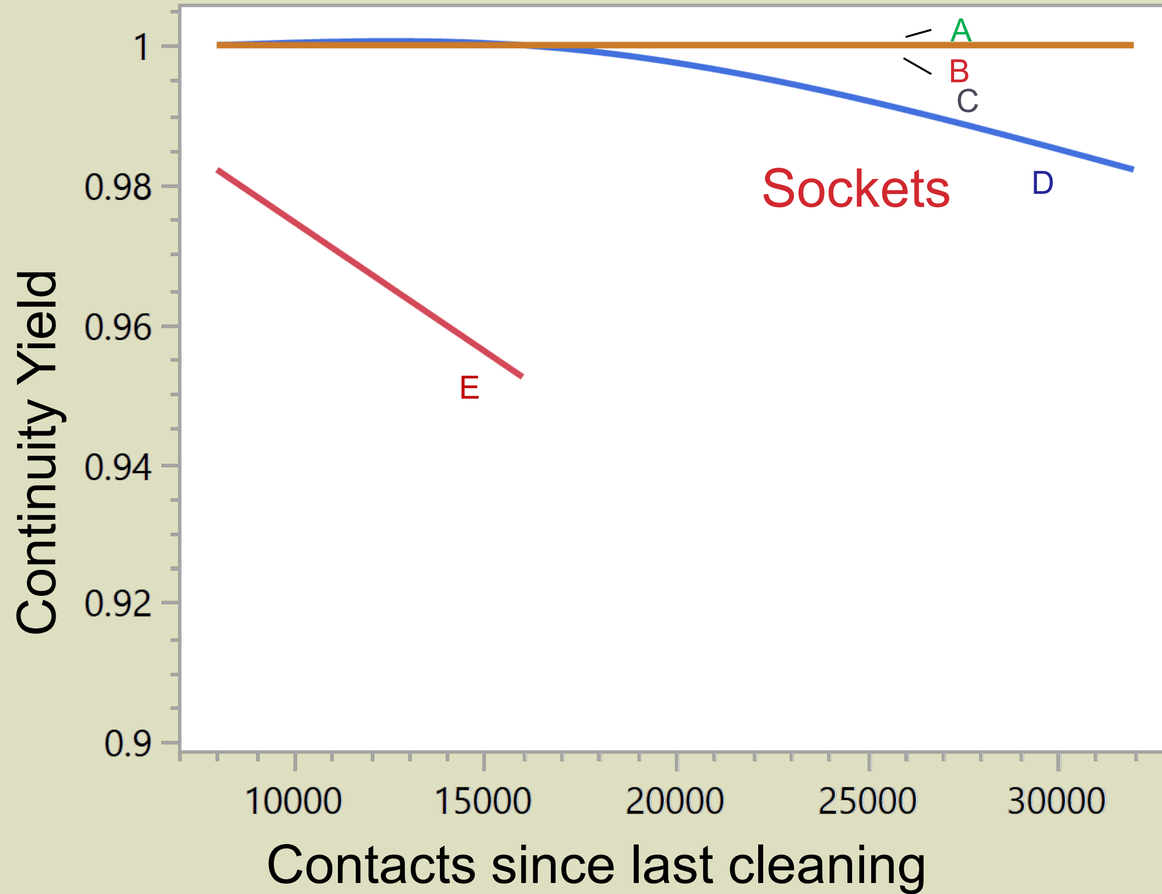
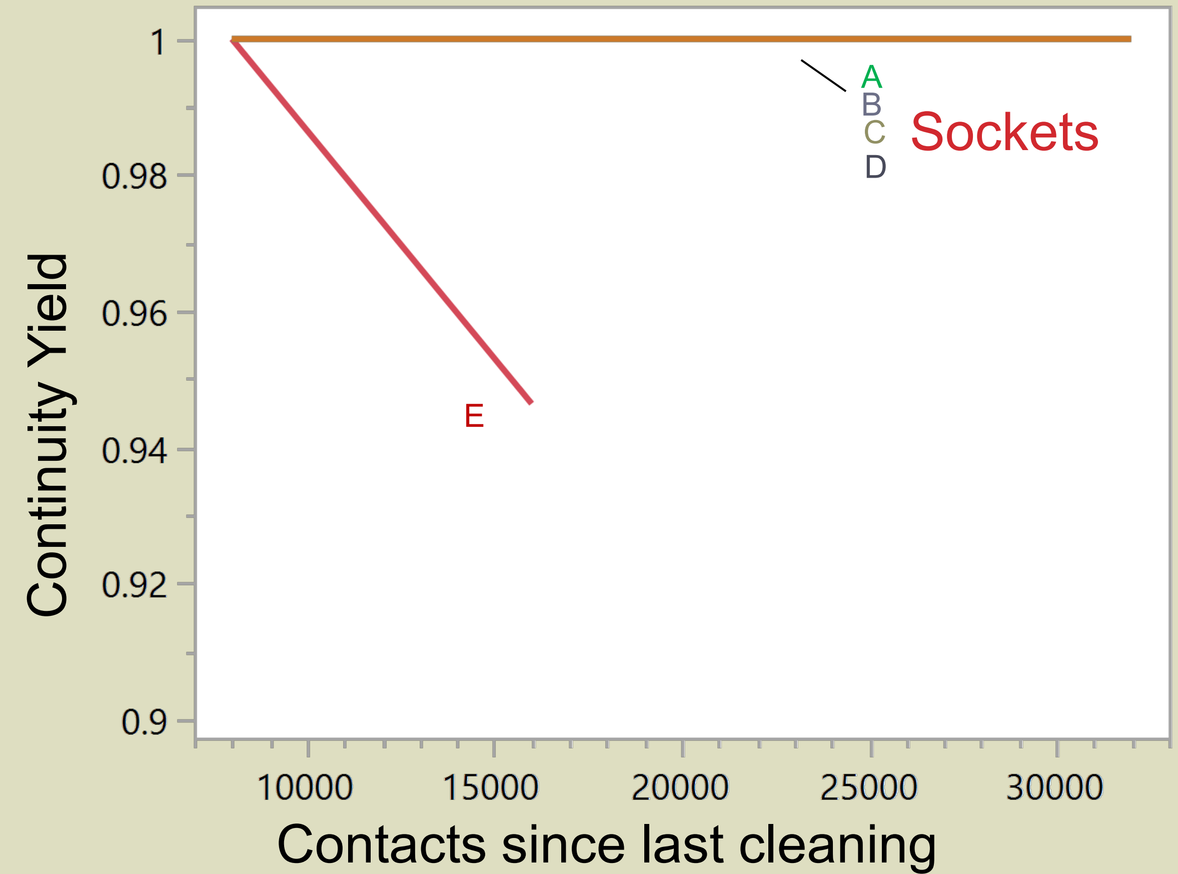


SOCKET CERTIFICATION

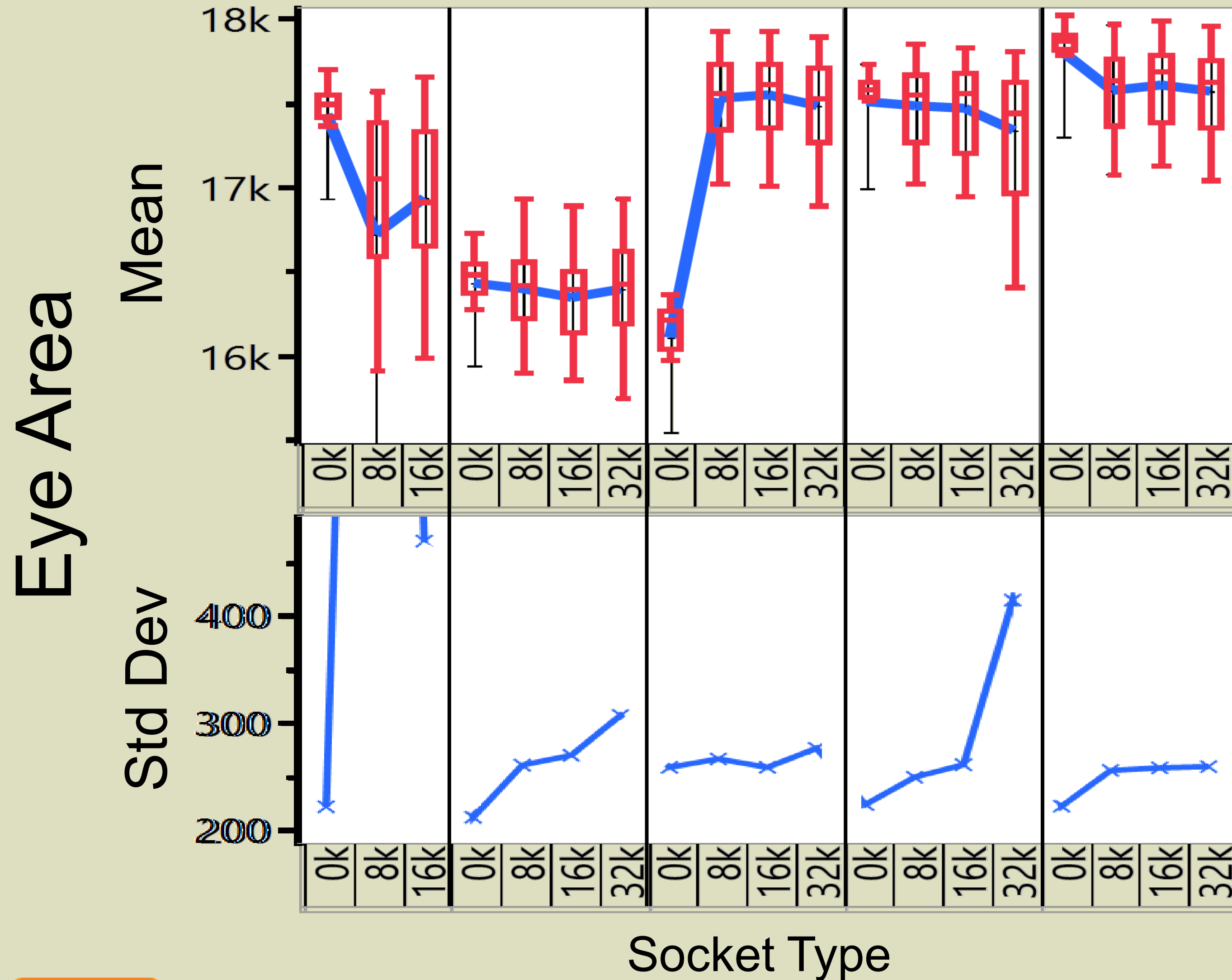
Life Test





- Good sockets may not last

PCIe Data Eye by Socket Usage



- Eye area trends smaller
- Variance trends larger

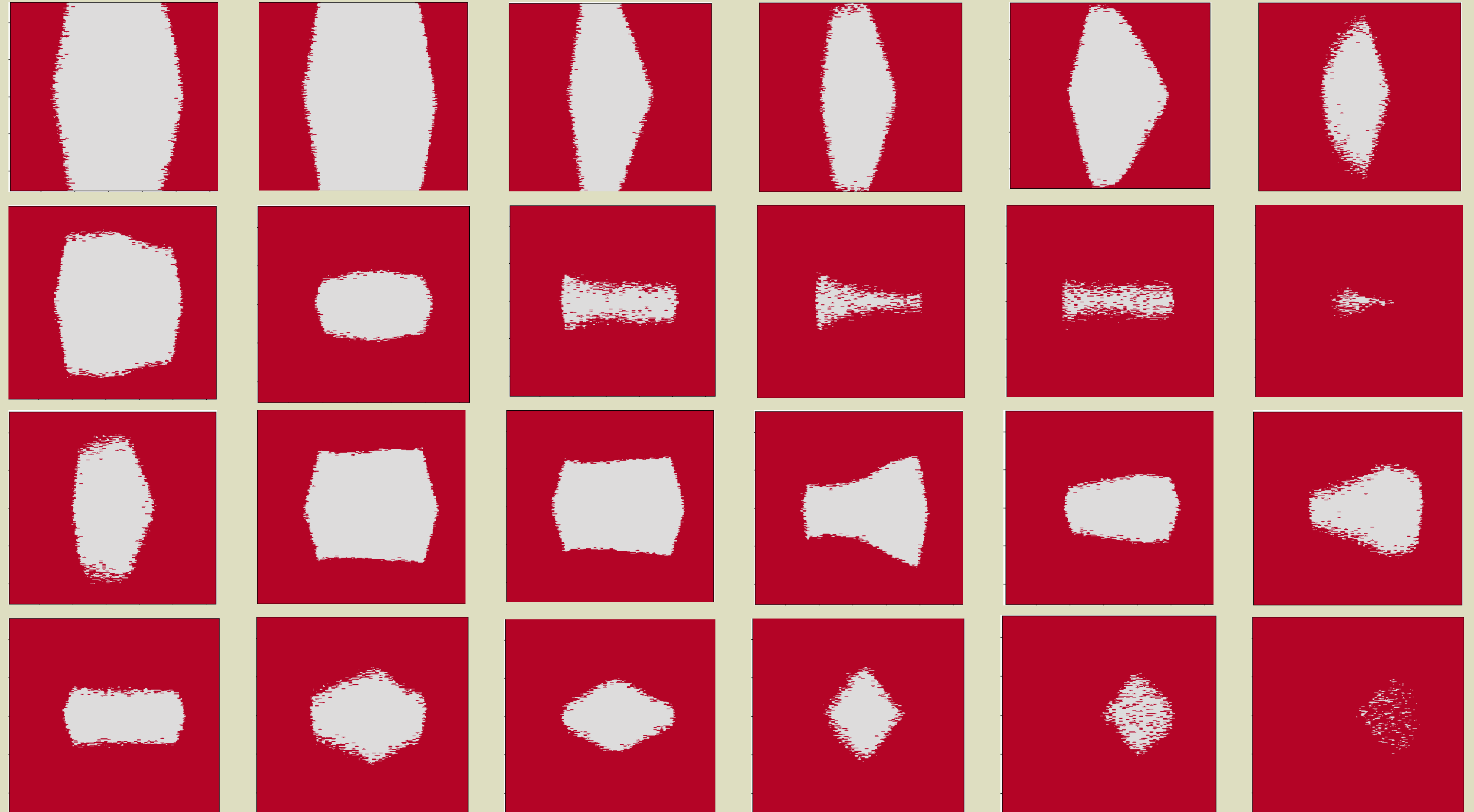
Contacts since last cleaning

Summary of Findings

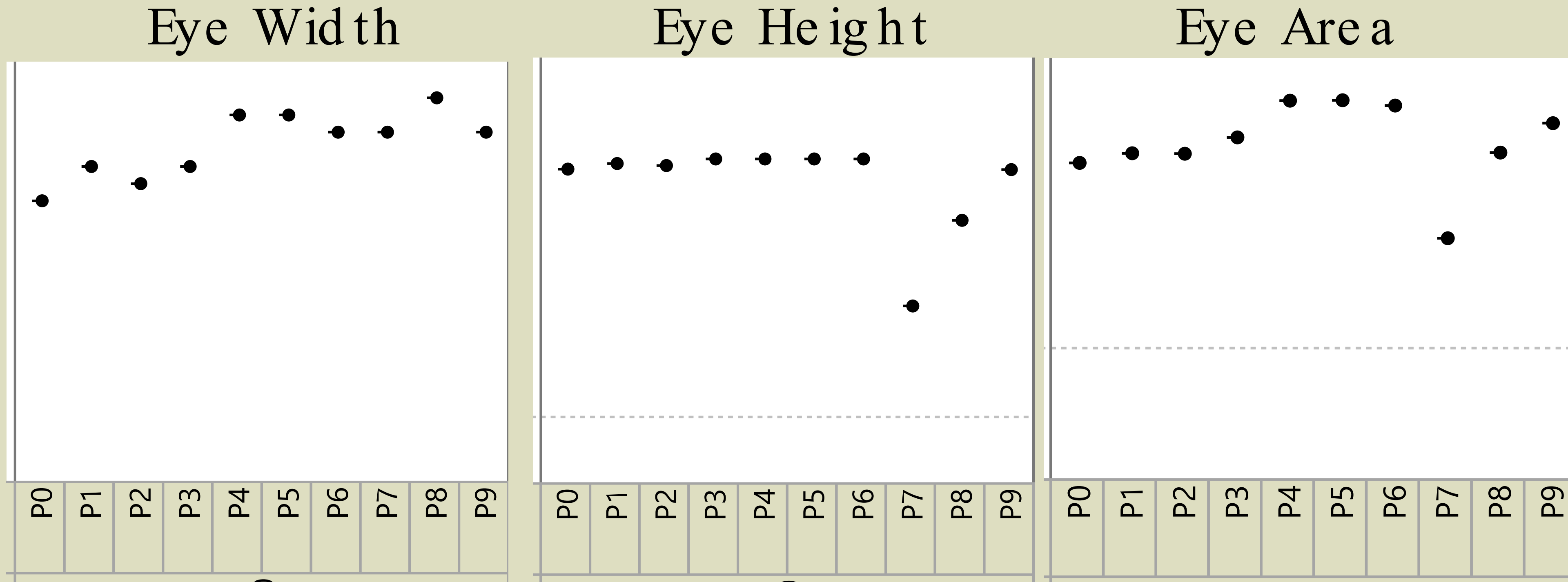
- Socket integration to loadboard degraded SI
- Test hardware measurably affected data eye
- Test conditions measurably affected data eye
- Data eye often correlated to mechanical performance
- Socket design affects thermal performance

Actual ATE PCIe Data Eye Examples

- Same silicon
- Same Scale
- Different test conditions

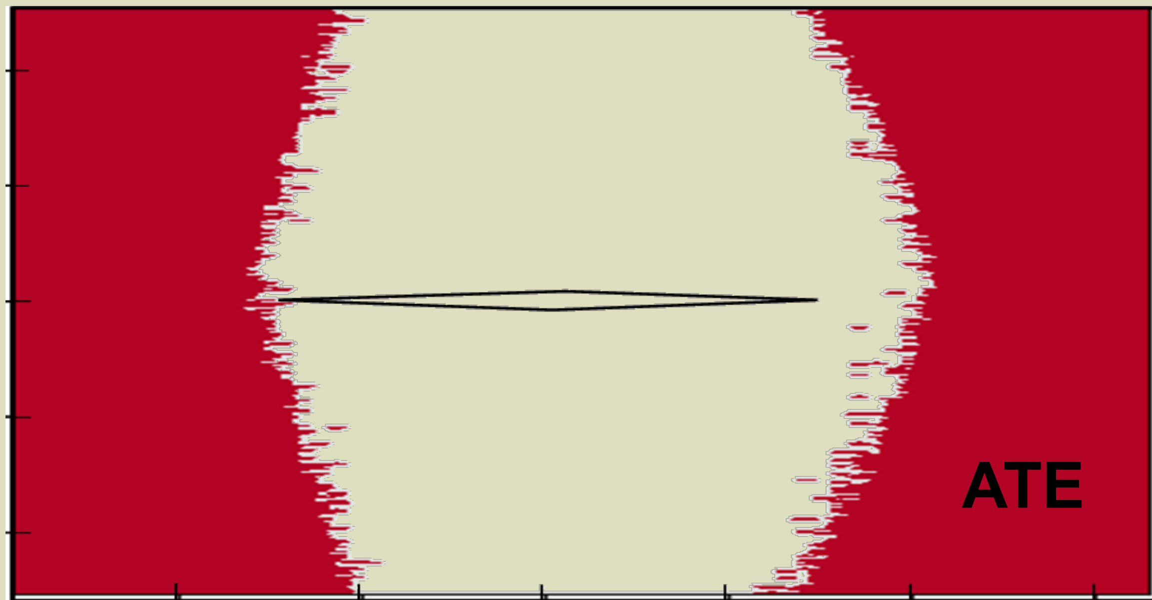


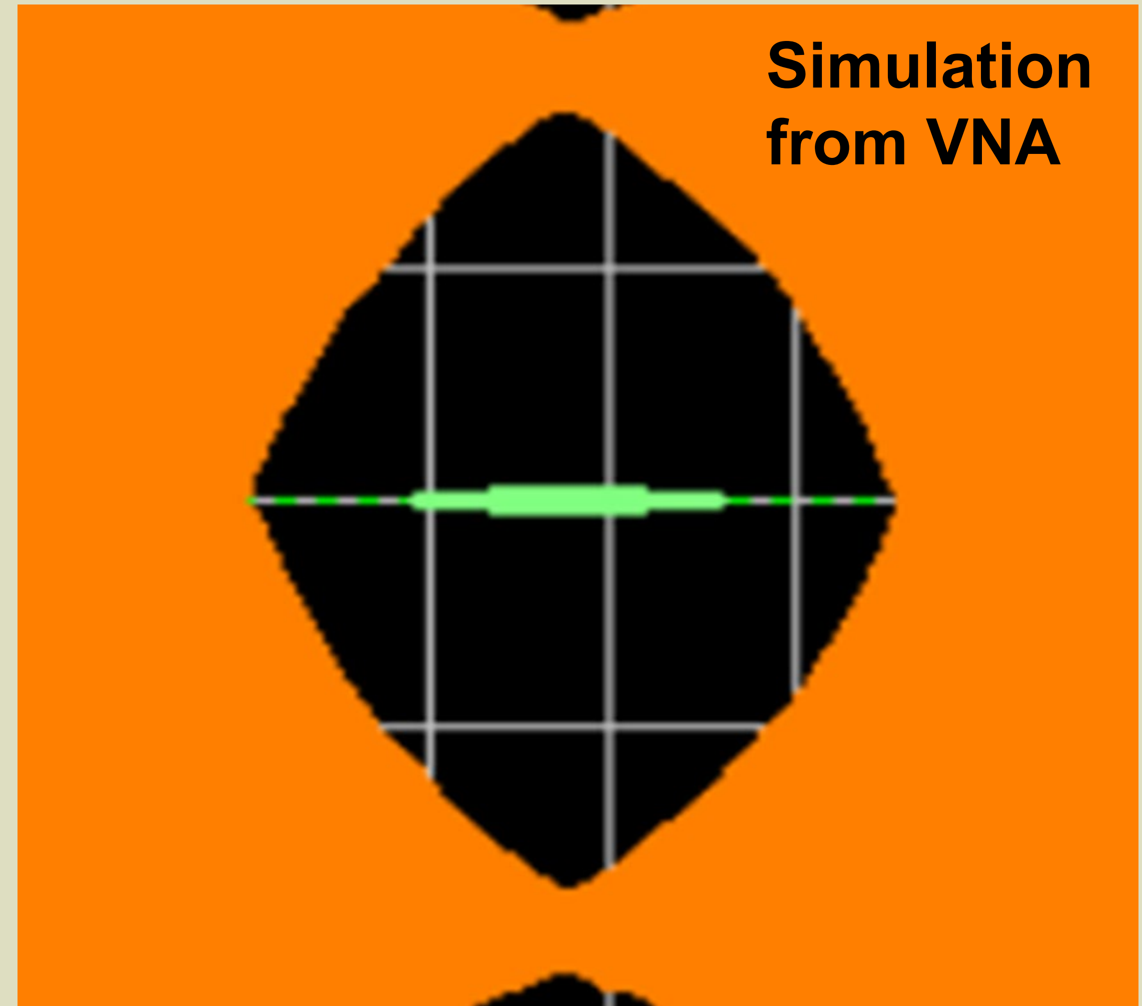
PLC Effect on Data Eye



- PLC settings affect eye statistics differently

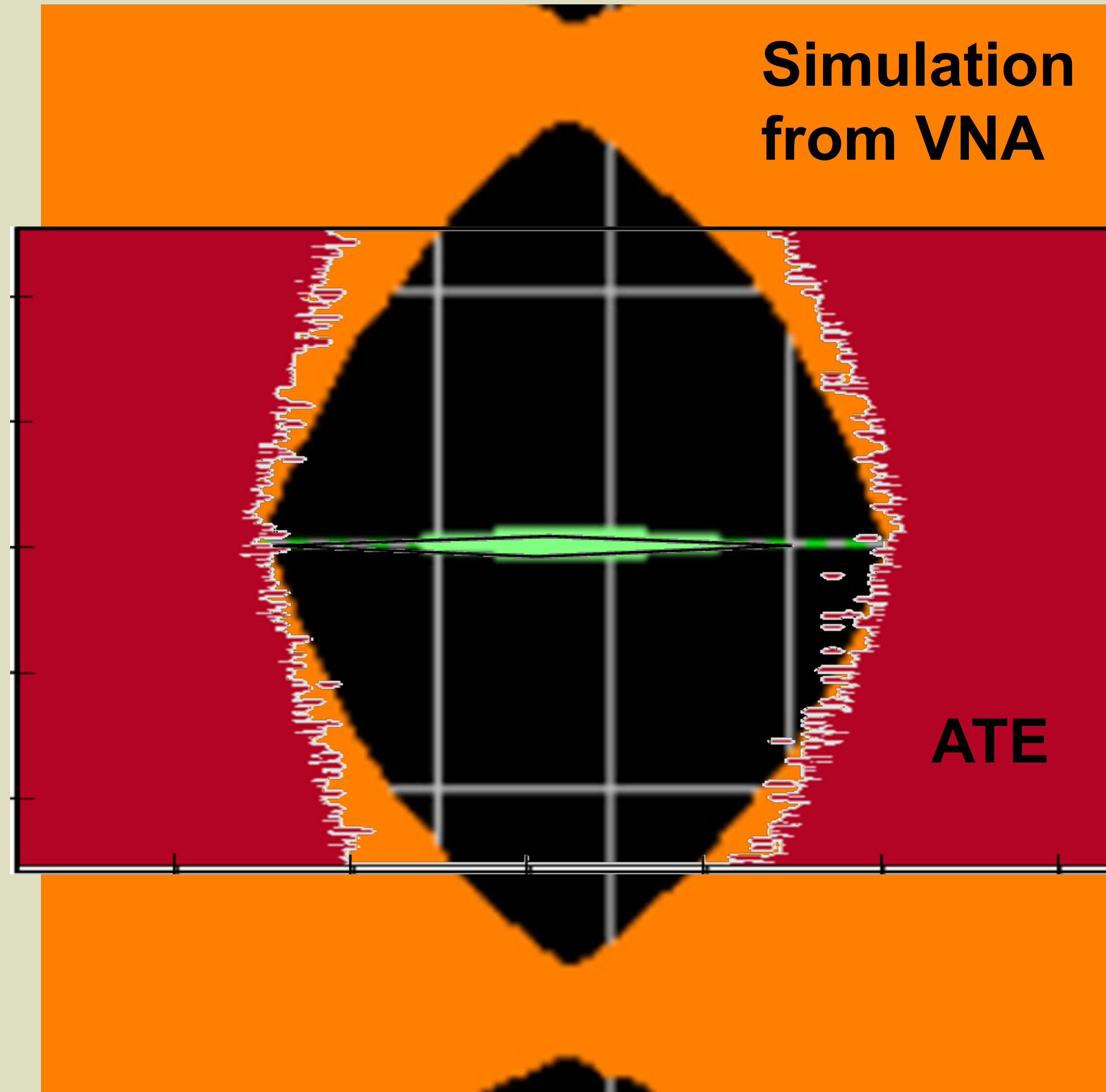
Example Data Eye Prediction





Example Data Eye Prediction

- Bench eye prediction is encouraging



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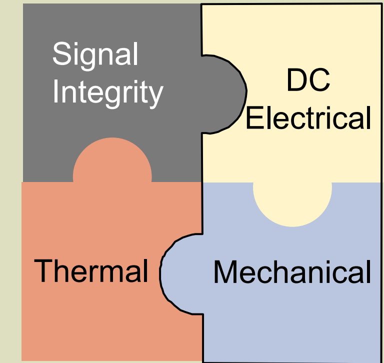
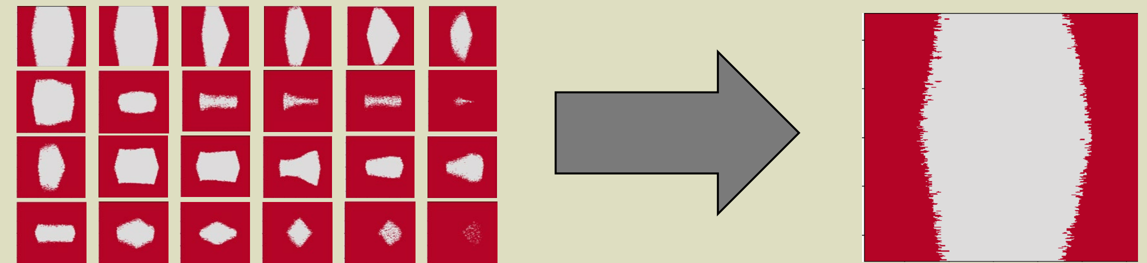
Conclusions



- Team precisely measured socket performance
- Test methods and socket design can improve SI robustness
- Early joint SI development with vendors led to successful sockets
- Comprehensive socket evaluations expose specific improvement opportunities



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