System Level Test – A need for Chiplet based AI and HPC Devices

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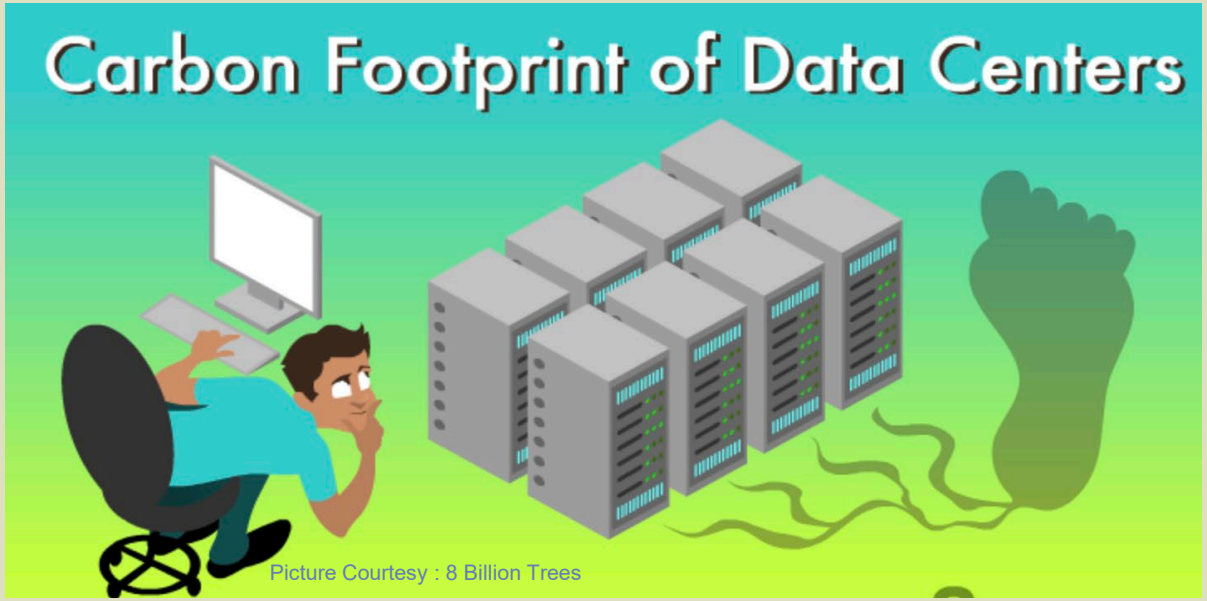
Agenda

- Trends in HPC and AI Product Development
- Chiplet based Heterogenous Test Challenges
- System Level Test – Key Differentiation in volume Test
- Test Flow for Chiplet Based HPC and AI Devices
- Summary

Trends in HPC and AI Product Development

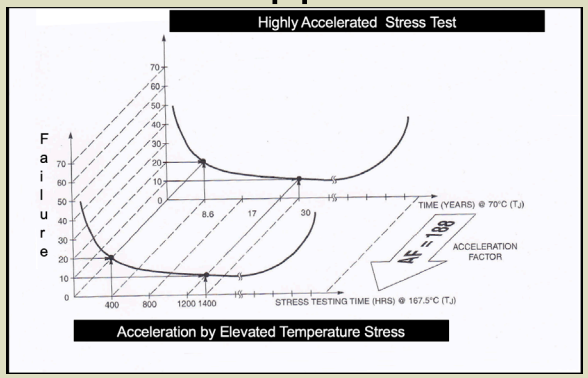
- Data centre offers massive computing resources, typically in the form of an elastic cloud platform
- Carbon Footprint
  - Electricity Consumption
  - Water Consumption
  - Lifetime of the Equipment
- Needs of Diverse Domain Specific Architectures
  - Machine Learning, Deep Learning, Block Chain and NLP
  - Dedicated Memory
  - More / Scalable ALU
  - Host of Interfaces, etc.
- Chiplets
  - Reduce Product Development time
  - Integrating Pre-Developed Die (KGD)
  - Different Process Node in the Same Package
  - Substrate a key element in System Performance



Data centres are responsible for 2% of overall U.S. **greenhouse gas emissions**

Trends in HPC and AI Product Development

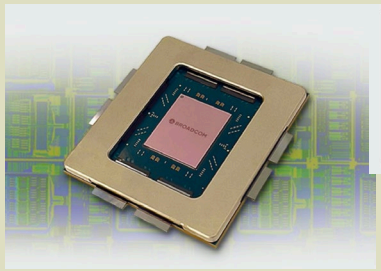
- Adoption of smaller process nodes in Mission Critical applications like Automotive
  - Reliability
  - TDP v/s Operating Temp

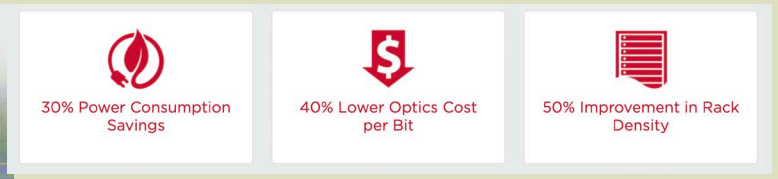


- Connected Vehicles
  - Latency (100 μs for 6 G)

- Hi-speed Interconnect standards (PCIE, CXL …)

- Co-Packaged Optics





https://www.broadcom.com/info/optics/cpo

Trends in HPC and AI Product Development

Key Essence

Product Development	Importance for Test
• Carbon Footprint - Electricity Consumption - Water Consumption - Lifetime of the Equipment	• Every mW of power optimization saves M $ - Substrate Design optimized for PDN - Thermal Management - Silicon Monitoring & Traceability
• Reduce Product Development time - Chiplets - Integrating Pre-Developed Die (KGD) - Different Process Node in the Same Package - Substrate influence in System Performance	- Chiplets designed considering DFT - KGD could be from many different vendors - Test / Validation of Substrate Performance - Traceability and Security

Chiplet based Heterogenous Test Challenges

KGD in Monolithic

Assembly defects and functionality at speed are tested at package level.

Functional requirements of the packaged parts do not change drastically from the die level.

DPPM target is with in the product company control.

KGD in Heterogenous

Assembly defects after package of a particular KGD many not be 100% directly detectable – Additional test.

Individual Die not necessarily define the full functionality of the Packaged IC .. could be only partial.

Third party Die could be integrated .. such as HBM.

Individual Die DPPM comes into picture .. The over all package level DPPM becomes an addition of individual KGD DPPM

Chiplet based Heterogenous Test Challenges

Die to die interconnect within the package only going to be in millimeters

- This will help to optimize the drive strength which will help to optimize the power consumption
- Testing them as an individual die poses a challenge.

Loop back test might be very much applicable for Hi-speed Interface

Reality of SI Simulation on Substrate interconnect actual manufactured substrate cannot be assumed to match

- Tight manufacturing tolerance of line width, space etc. is critical.
- Net list Open/Short test data of substrate + critical hi-speed substrate trace testing on sampling would help to improve packed IC yield. Possibility of critical signal trace coupon can be explored.

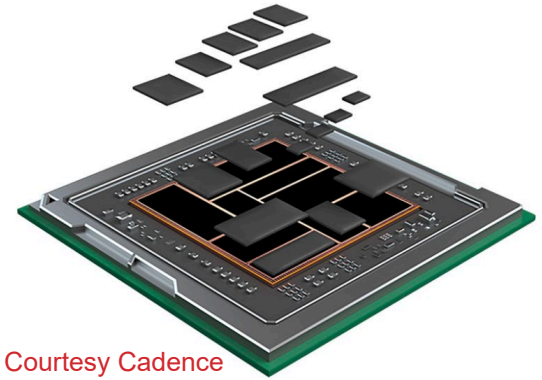


Image Courtesy Cadence

With Chiplet PPA is not just for Chip Design – now to Substrate Level

Thermal Consideration – Influence of Chiplet just few mm apart

Substrate material – Laminate / Silicon-Passive / Silicon-Active

Power Plane impedance inside the Package

Chiplet based Heterogenous Test Challenges

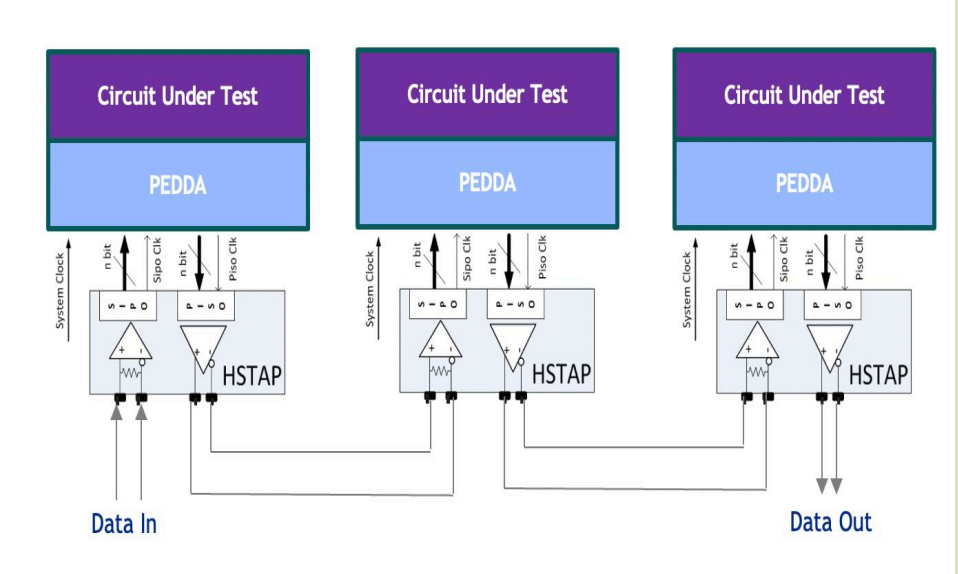
DFT

Package level failure that points to a specific Chiplet.

DFT architecture need to be implemented as sub-block approach.

Scan vectors could be still run by isolating the faulty sub-block/chiplet and able to verify the remaining integration.

SSN/1149.10 based DFT architecture need to be explored.



Has the industry evolved to openly give DFT vectors of the chiplet to external companies?

- **LBIST and MBIST** enablement and result registry access.

Would the robust good old boundary scan IEEE-1149.1 be a fallback solution?

- Chiplet to chiplet interconnect on the substrate can be thought of multiple ICs on the PCB
- Ride on HSTAP / JTAG interface if available.

Chiplet based Heterogenous Test Challenges

What is happening inside the Chip? – Monitor (Design , Volume Test and In-Field)
In-Chip-Monitor – Instantaneous Environmental Monitor.

- Process Monitor.
- Power Rail Voltage Monitor.
- Temperature Monitor.

Dynamic Voltage and Frequency Scaling (DVFS)

Process Monitor

- Decision making before classify the Die a KGD
- Behavioral understanding of Wafer Level and Lot Level

On Die / Active Silicon Interposer

Power Rail Voltage Monitor

- Compute Performance optimization by monitoring Voltage
- Alarm / Interrupt Signal activation to other subsystem and bring the device to safe state
- Could be considered as a part of POST

Temperature Monitor

- Compute Performance optimization by monitoring Temperature
- Alarm / Interrupt Signal activation to other subsystem and bring the device to safe state
- Could be considered as a part of POST and for Mission Mode Test.

Chiplet based Heterogenous Test Challenges

Thermal Management - Requirements

Active Thermal Control (ATC) for products requiring near 1 KW power dissipation

High speed, 1 ms closed-loop ATC for applications in Engineering Development, Test, Burn-In and System-Level Test

Control loop to interface with Device Diode Temperature sensor

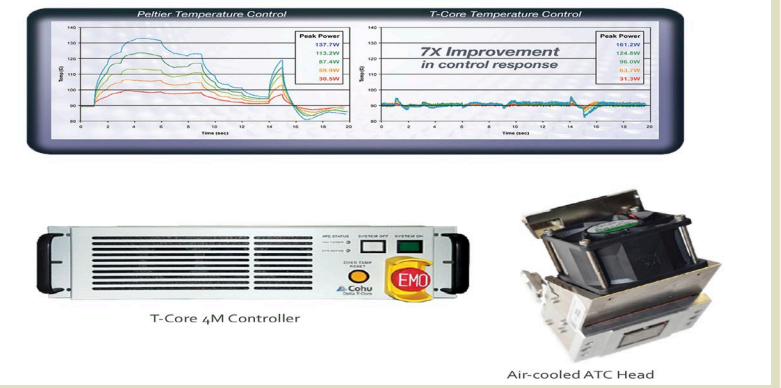
Architecture to support multiple sites with multiple RTD sensors per site

Fast temperature ramp up/ Ramp Down in the range of 100 °C/s

Closed-loop Automatic Flow Control (AFC) for liquid-cooled, air-cooled or phase-change (refrigerant-cooled) thermal heads

Support for tri-temp testing with single insertion during Char routines / System Level Test

Multi-site Handler that has a capability to interface with ATC for volume test



Picture courtesy Cohu, Inc.

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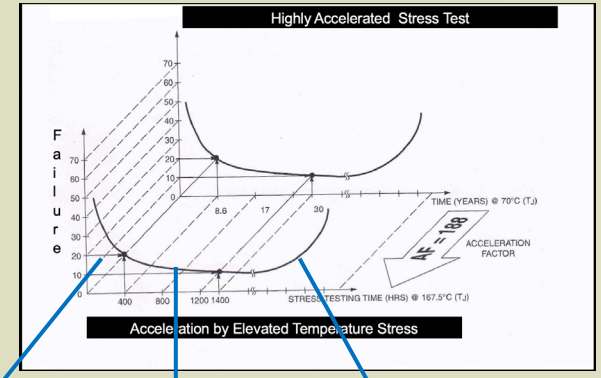
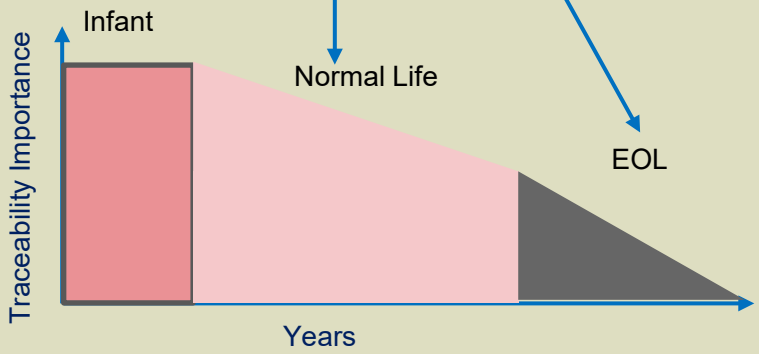
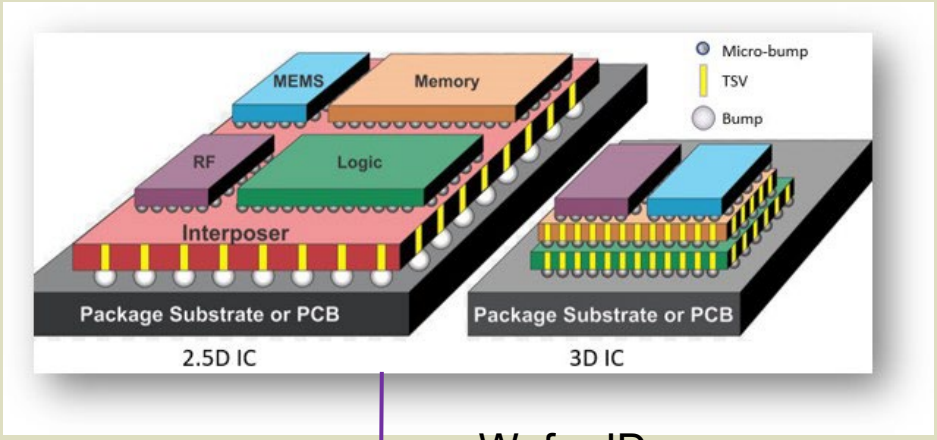
Chiplet based Heterogenous Test Challenges

What happens when the Heterogenous packaged IC Fails in the Field?







- Wafer ID
- Die ID
- Assembly Data
- Test Data

Traceability of Chiplet to Individual Die level info form the Packaged IC on a established protocol Interface for quicker retrieval .. Thus, enabling Datal Analytics need to considered of Importance

OSAT provide Unit Level Traceability (ULT) by 2d Barcode on a Packed Device. Commercial Device may need about 5 years of traceability but for Automotive it would extend to 15 Years

Identifying root cause sooner would be important for Automotive Grade IC (especially for ADAS Levels 4 and 5) and probably for high end HPC ICs

Chiplet based Heterogenous Test Challenges

In-Chip-Monitor – Structural Monitor

- Semiconductor do have ageing as inherent property as it is influenced by NBTI (Negative Bias Temperature Instability), HCI (Hot Carrier Injection) and TDDB (Time dependent dielectric breakdown).
- Aging affecting Propagation Delay

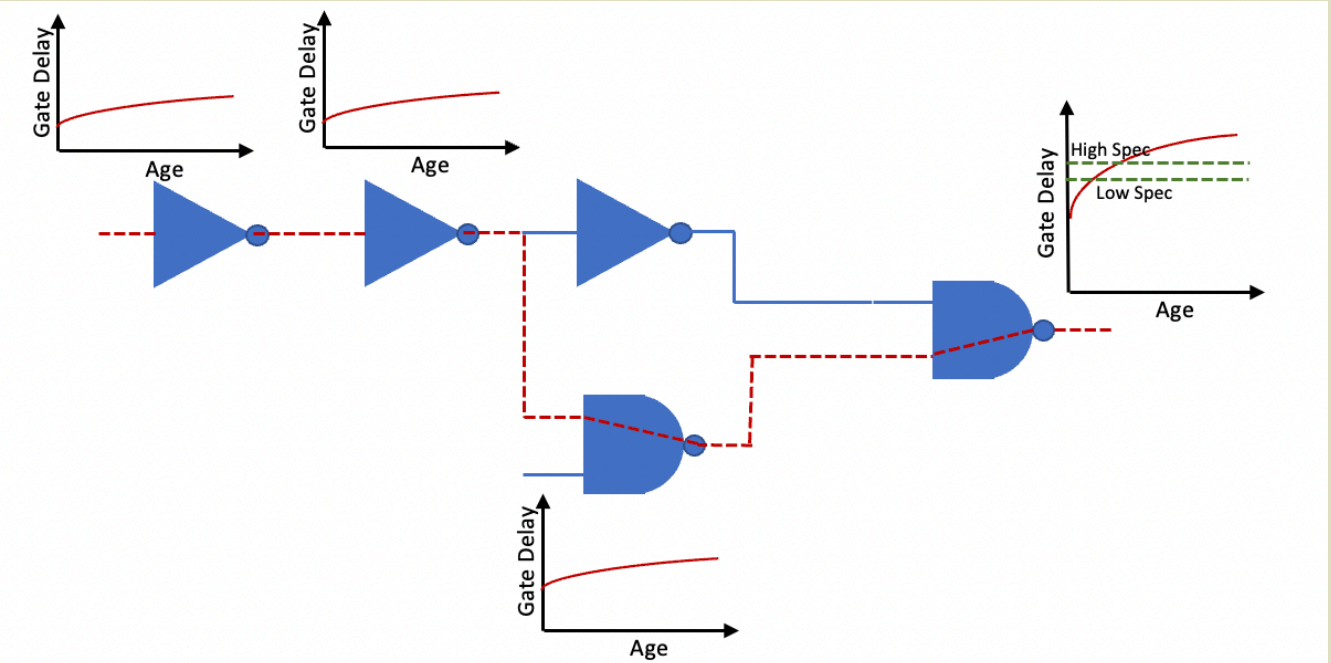


Figure 1: Foundry provides aging model of the transistors to do timing analysis of the circuit. As the transistor ages over period, it increase the gate delay. This could violate the timing spec that is required for the proper function of the circuit during its expected operating lifetime.

Chiplet based Heterogenous Test Challenges

In-Chip-Monitor – Structural Monitor

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Path Margin Monitoring

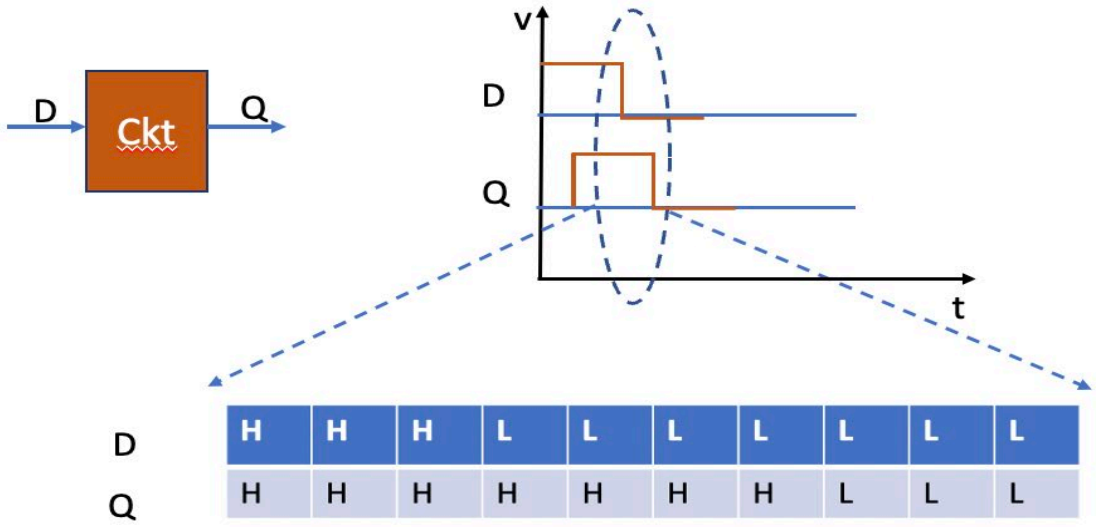
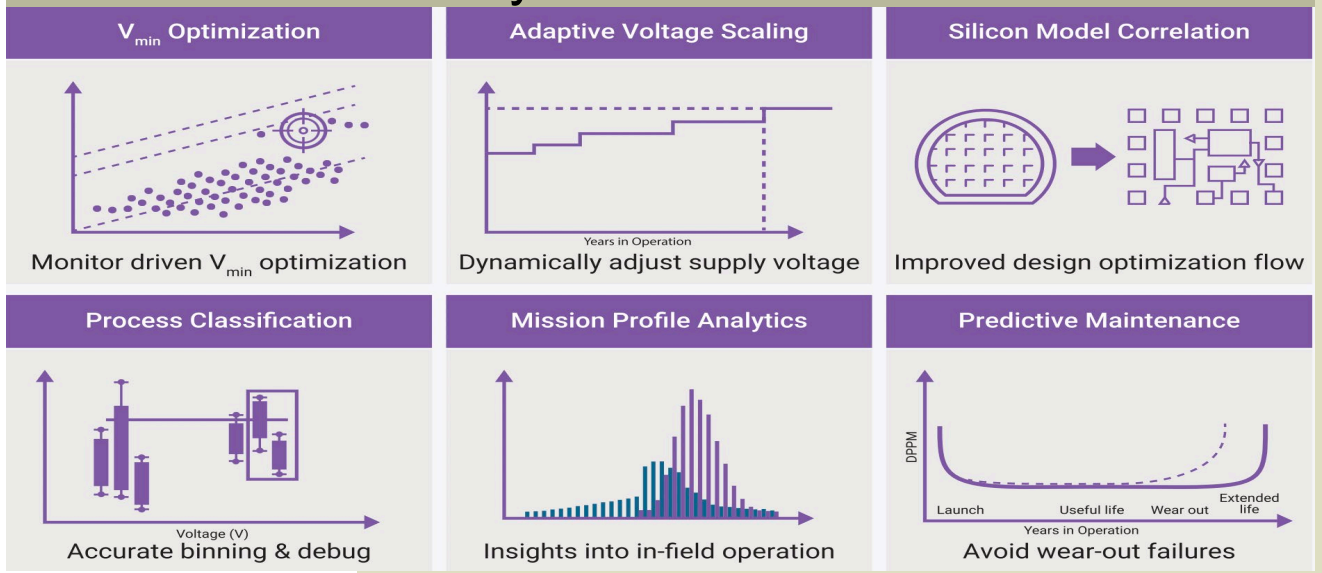


Figure 2 : Response of a digital path in a circuit constituting a Delay and its time domain response. The dotted line captures the state of the input D and out put Q, which are sampled faster.
In this illustration 10 logic states are collected from D and Q to form a Signature

SLM Use Case : EDA Vendors now provide Silicon Life Management Tool (SLM) for end-to-end Visibility.. Right from Design, Product Ramp, Volume Production and finally In-Field



Courtesy : Synopsys https://www.synopsys.com/solutions/silicon-lifecycle-management.html

Seems no SLM Standards established yet !!

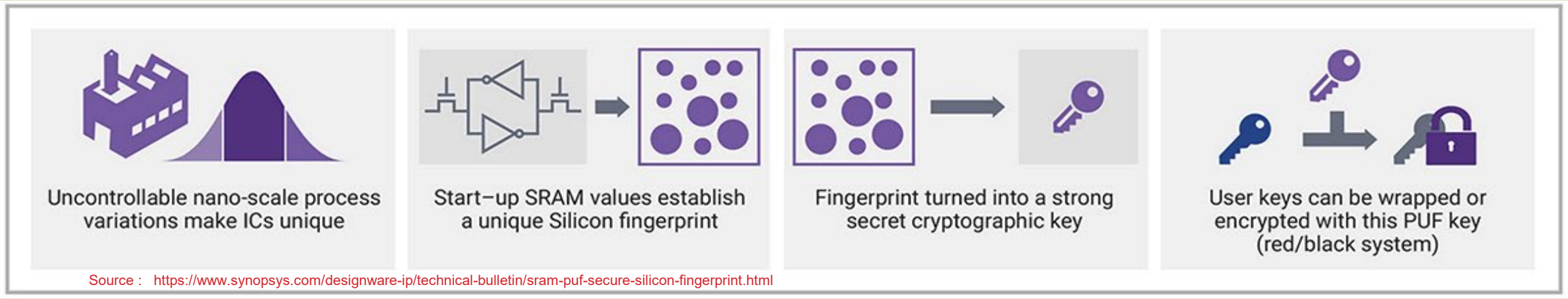
Chiplet based Heterogenous Test Challenges

Integrating multiple chiplets into a heterogeneous package opens the door for security breaches and potential risks for cyber attack

Companies that has own chiplets, which minimizes supply chain threats of clone. But companies assembling and integrating commercially developed chiplets will have a much tougher time.

SRAM PUF (Physical Unclonable Functions)

The behaviour of an SRAM cell depends on the difference of the threshold voltages of its transistors. Even the smallest differences will be amplified and push the SRAM cell into one of two stable states. Its PUF behaviour is therefore much more stable than the underlying threshold voltages, making it the most straightforward and most stable way to use transistor threshold voltages to build an identifier.



Source : https://www.synopsys.com/designware-ip/technical-bulletin/sram-puf-secure-silicon-fingerprint.html

System Level Test – Key Differentiation in volume Test

ATE Test Facts – HPC Perspective

In ATE based test, the focus is getting the various blocks of the IC for a pass and fail

DFT targets Struct at 0, Struck at 1, Bridge Faults, Delay Faults .. Not computational work loads

DFT – SCAN chains are optimized for the current capability of the ATE DUT power supply.

Focused mainly on testing the structural content on the Digital, PLL, HSIO Eye Mask etc

Load Board Designed for ATE based testing is far from Real life Application Board

ATE Load bard usually do not include the external Memory and Support IC such as PIMIC etc..

Number of parallel device tested in ATE is limited by ATE available resource and hence usually 4 to 8 device tested in parallel for high pin count device

Burn-In Ovens – HPC Perspective

Traditional Burn in ovens only provide setting up the ambient temperature do not support ATC

System Level Test – Key Differentiation in volume Test

System Level Test - Facts

Compared to ATE test time, usually in seconds .. SLT test time could run to several minutes

SLT's massive parallel test brings the opportunity to move SCAN / BIST from ATE to SLT

SLT is performed in massive parallelism and hence a specialized SLT Handler Equipment needed .. Additional CapEx

System Level Test – Key Differentiation in volume Test

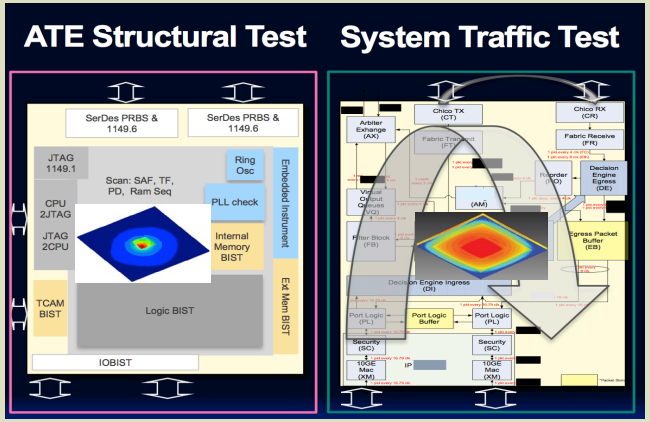
Real Application Test Needs

HPC, Automotive IC needs to be tested along with the other supportive ICs such as PMIC, External Memory, Display, running on a customer-specific firmware. It is important to mention that the external support ICs mentioned may not be from the same manufacturer.

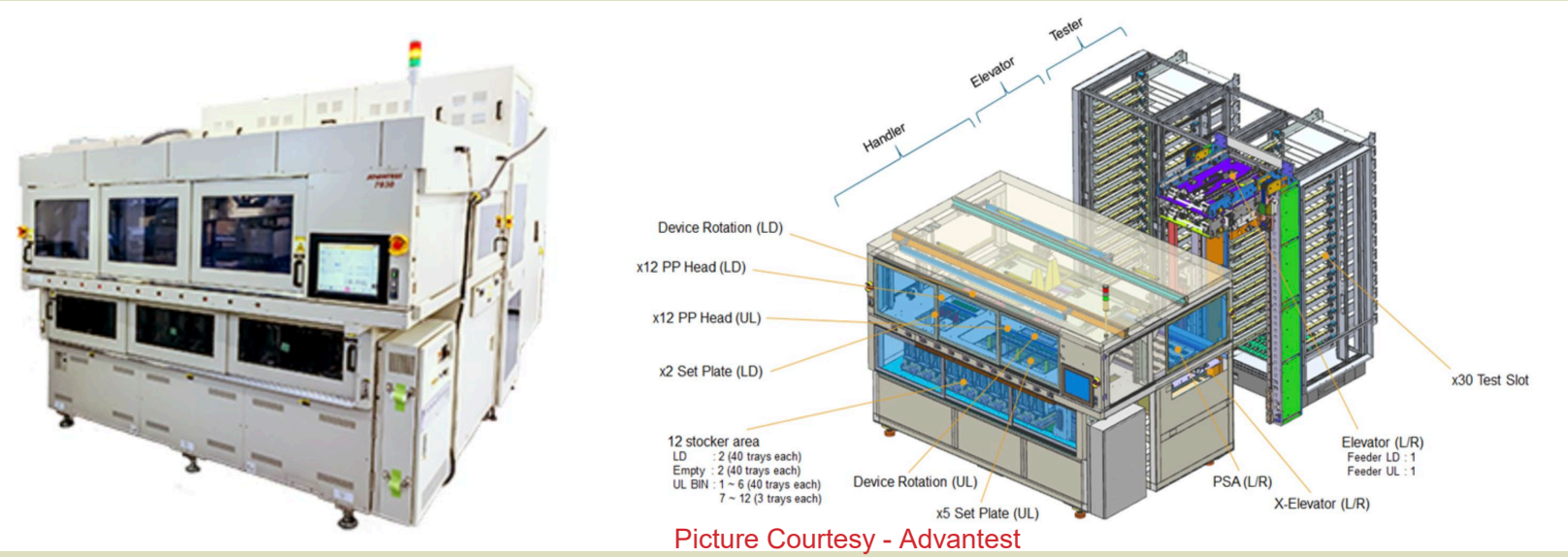
Testing for customer-specific Use Case is becoming a key need for the devices that are used for mission-critical applications such as Automotive and Data Centers (Silent Data Corruption) along with the need for DPPM quality levels… Drives SLT requirement

System-level test is the ability to test a chip, or multiple chips in a package, in the context of how it ultimately will be used.

***Source: Semiconductor Engineering 9 Oct 2017**



System Level Test – Key Differentiation in volume Test



Picture Courtesy - Advantest

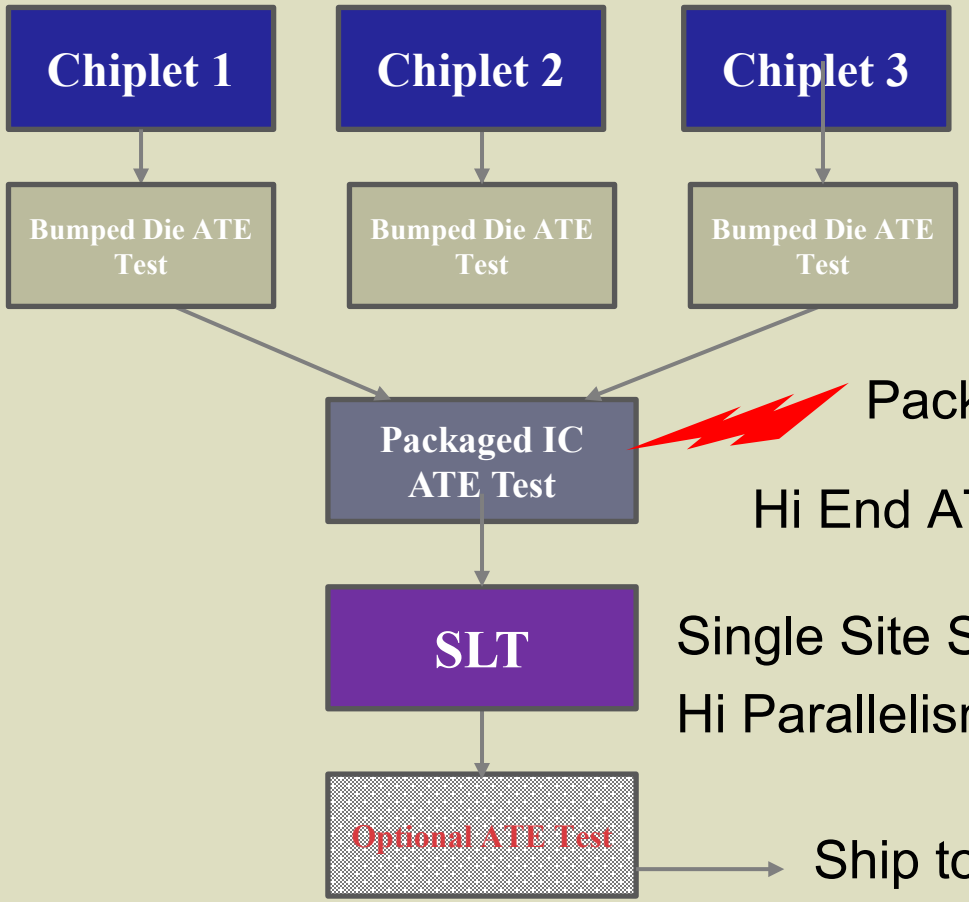
A typical Test Engineer with ATE experience may not have the knowledge of writing Test Use Case.

Writing Test Use Case are requires understanding the BSP , Bare Metal Programming and on the Operating Systems such as Linux, Android etc.

A collaborative approach of Embedded expert along with experience of volume Test is required to enable a SLT solution to production.

Single Site SLT to run small volume for NPI safe launch

Test Flow for Chiplet Based HPC and AI Devices



Low Cost ATE - Parallelism more than 8

Package Substrate performance

Hi End ATE – Parallelism 4 to 8

Single Site SLT for NPI - Use existing Handler

Hi Parallelism SLT for Volume – SLT Handler

Ship to customer

Summary

Traditional ATE test focused on Structural Fault Model and Scan chains optimized for the ATE DUT Power Limitation

SLT Vendors provide additional HSIO hardware in SLT to run SCAN, LBIST, MBIST

System board modified for Socketed SLT need to take care of the parasitic of Test Socket

Embedded Expertise step into Test (Engineer having ATE Test and Embedded Software Expertise would worth a Gold)

Efficient use of in Chip Monitoring while integration with ATC is key for testing the HPC device to its Limit

Implementing Chiplet level / Die level traceability as part for SLT may add a great value in RMA

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