TestConX 中国 China
November 13, 2025
Shanghai
www.testconx.org
© 2025 TestConX– Image:iStock-123ArtistImages

Implementing Effective Test Limits for Rapid Root-Cause Analysis in RMA Investigations

Hailin Wang, David Chang
ElevATE Semiconductor

TestConX中国™ China
Shanghai ▪ November 13, 2025

ELEVATE SEMICONDUCTOR

Presentation Outline

- Problem Statement
- Root cause investigation
- Test Methodology
- Solution & Validation
- Conclusion

Problem Statement

- Customer reported gross functional failures
  - 4x RMA (Return Merchandise Authorization) were given for analysis
  - Abnormalities reported in Force & Measure circuits
- Customer goals
  - Sustainable problem resolution
  - Rapid containment
  - Address root cause
- ElevATE goals
  - Fulfill customer needs
  - Preserving yield

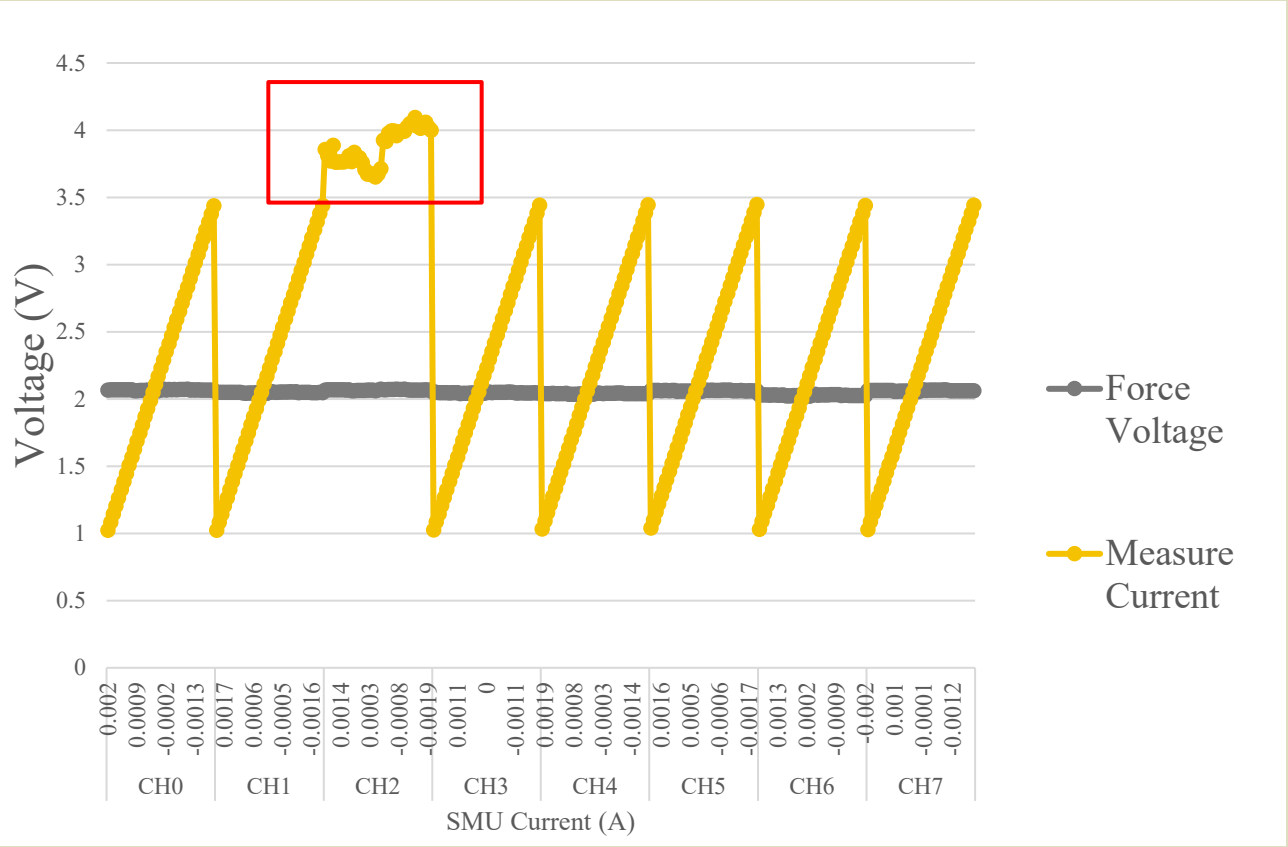


Figure 1: Electrical testing results of failing RMA Devices failing Channel boxed in red

Determination of failure

- All devices passed final test
  - Proved parts exiting facility were good parts
- Defects only appeared post-test (field use)
  - Early life failures?
  - Randomly distributed?
  - Undetected Latent defects?

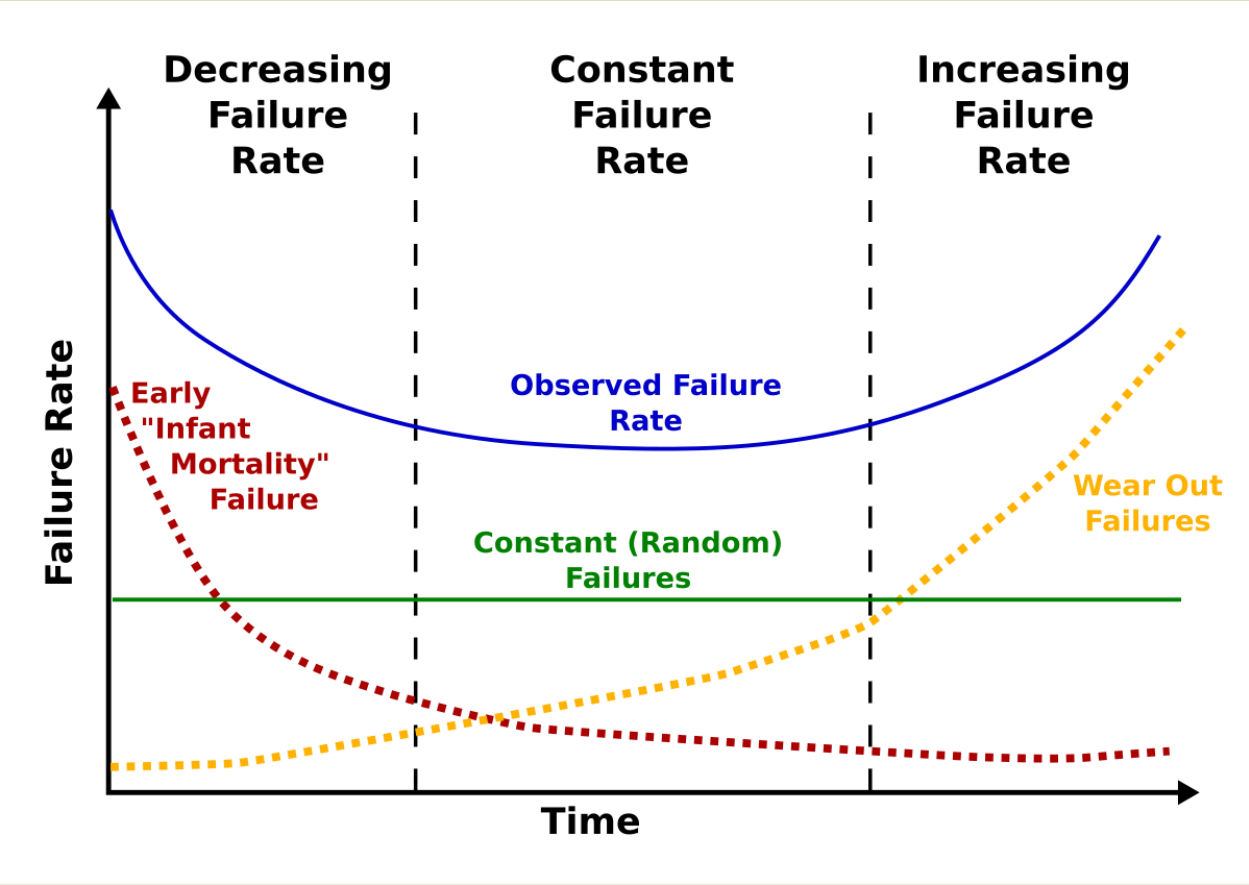


Figure 2: Reliability bathtub curve for semiconductors [1]

Root Cause Investigation

- Testing process
  1. Rescreen RMA devices
  2. Issue replication on bench
  3. FA (Failure Analysis) imaging using PEM
  4. Validation of tests

- Result
  Visible hotspot in imaging of Forcing and Measure circuitry

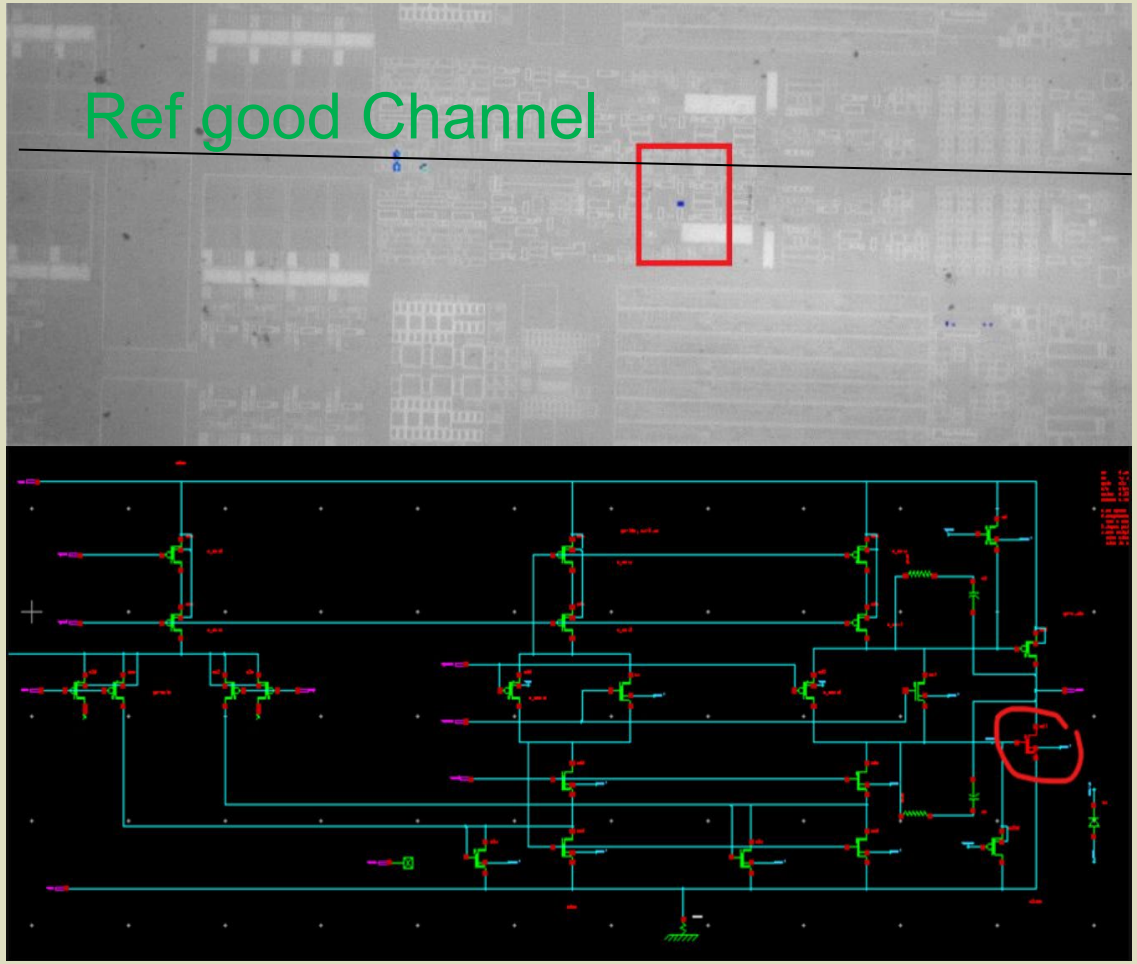


Figure 3: Top PEM imaging showing an area of high electron emission intensity
Bottom: Transistor impacted by failure caused by MIM Capacitor short

Physical Failure Signature

- Electrical signature
  - Electrons emitted from transistor gate via EMMI testing
  - Caused by physical MIM (Metal-Insulator-Metal) Defect
- Traceable to failure
  - Loss of functionality in Measure circuit
  - Capacitor short creates leakage path to gate of transistor

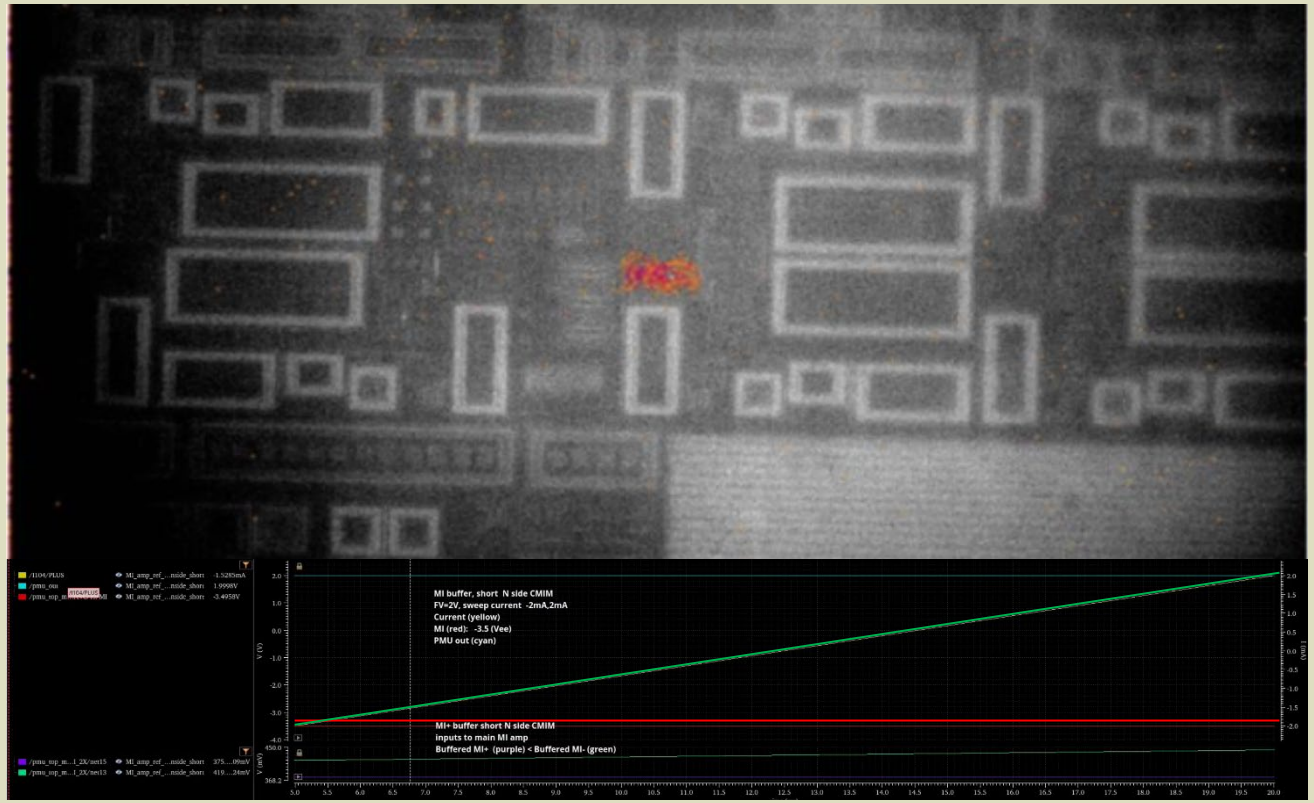


Figure 4: Increased electron emission caused by MIM Capacitor short confirmed in design simulation failing device red, reference device green)

MIM Capacitor Failure Mechanism

- Failure factors:
  - Voltage stress
  - Duration of stress
- Manufacturing defects can weaken the dielectric
  - Lead to accelerated breakdown of the insulating dielectric of the MIM capacitor

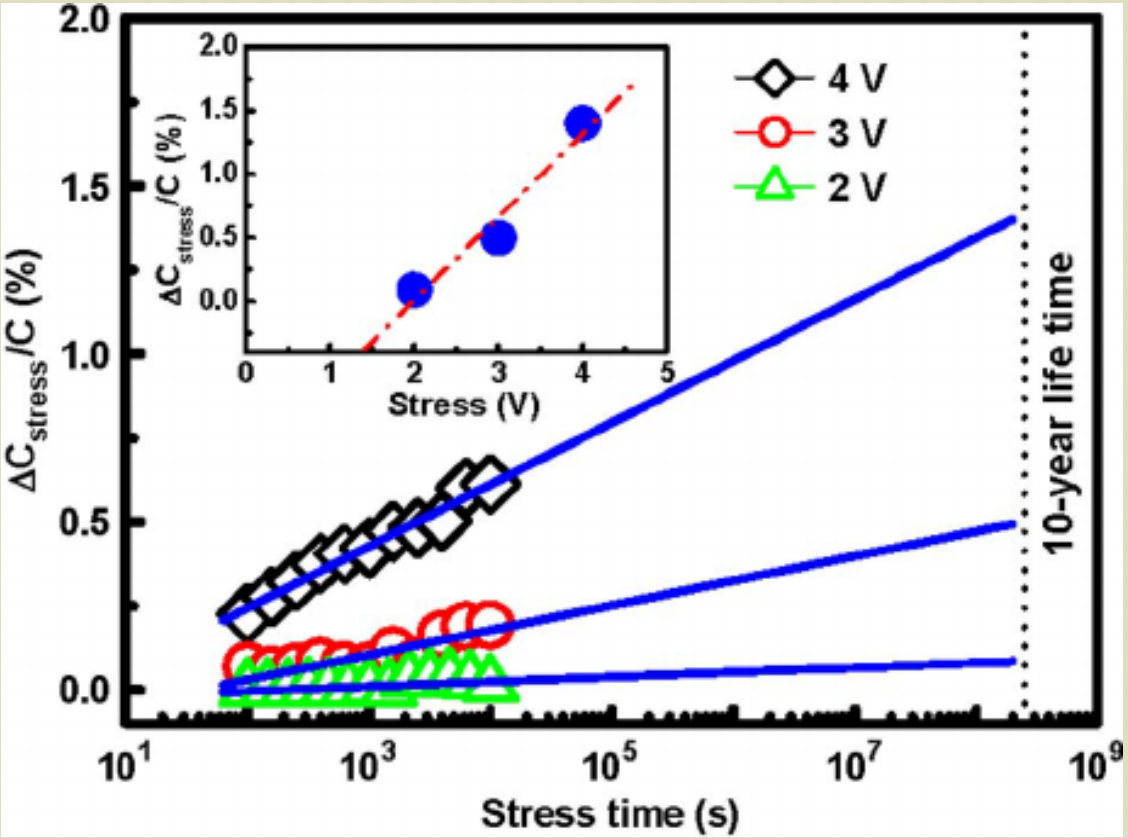


Figure 5: Change in capacitance vs external conditions [3]

Methodology Review

- Result
  - Confirmed root cause
  - Cross functional team for data collection, correlation, analysis
  - 100+ engineering hours
- Multi-step process
  - High cost
  - Time intensive

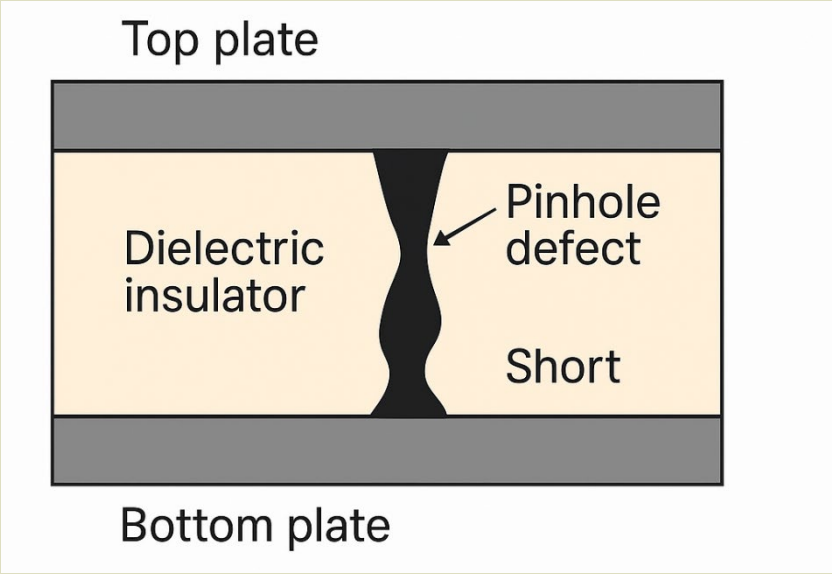


Figure 6: Diagram of root cause MIM capacitor defect

ATE Stress Testing MIM Capacitors

- Goal:
  - Develop a screen to detect defects
- Method:
  - Understand propensity for failure through targeted voltage stress on specific capacitor instances
- Result:
  - Distinct leakage measurements between failing and passing devices
  - ATE results correlate with failure mechanism from [3]

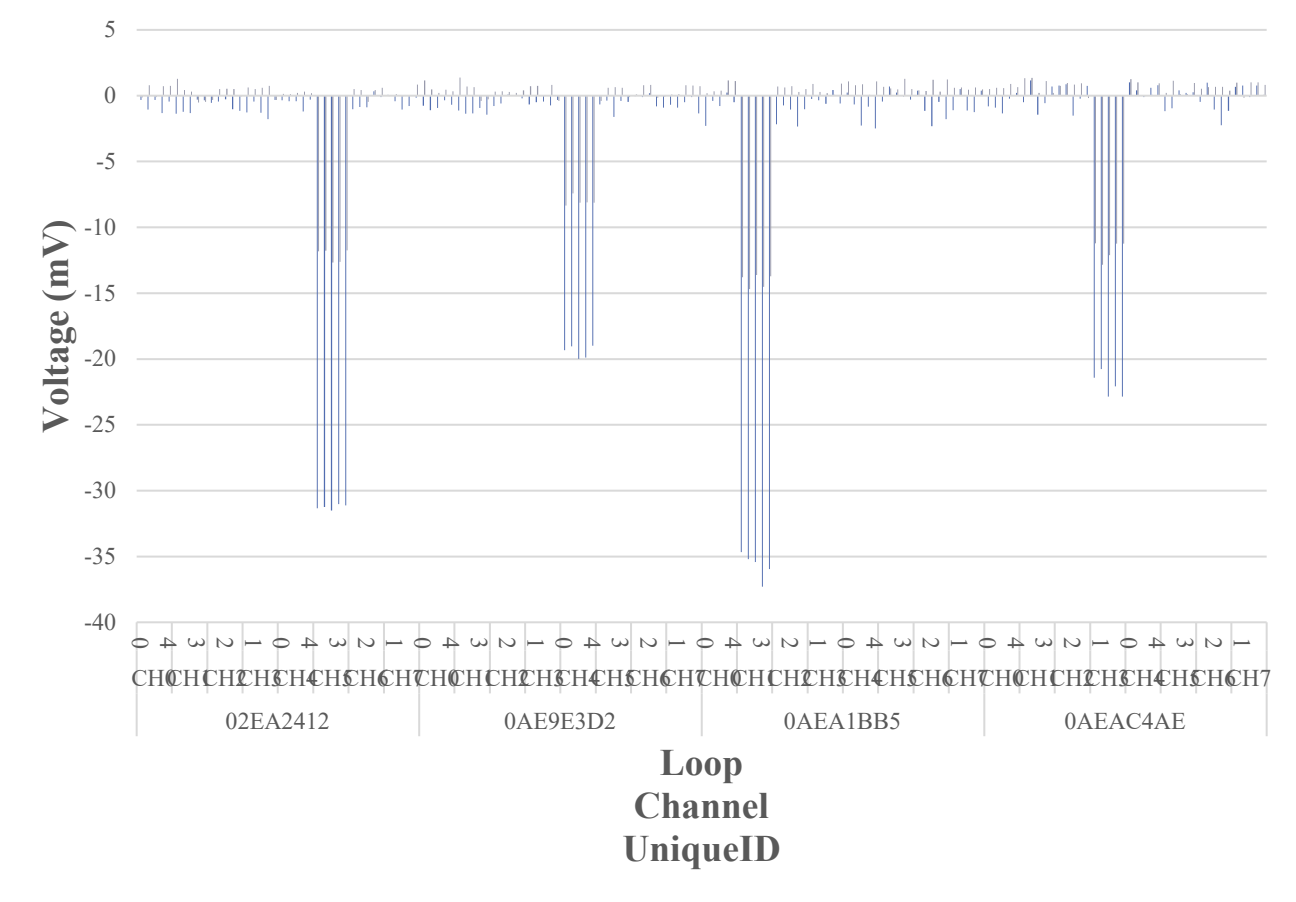


Figure 7: RMA failures tested for Voltage delta while Stressed At +7V & -2V 5xLoop

ATE Test Enhancements

- Revised ATE screen data successfully detected the MIM capacitor failures
- Further adjustments of limits focus on detecting:
  - Marginal failures
  - Lot variation
  - Ensuring repeatability & reproducibility

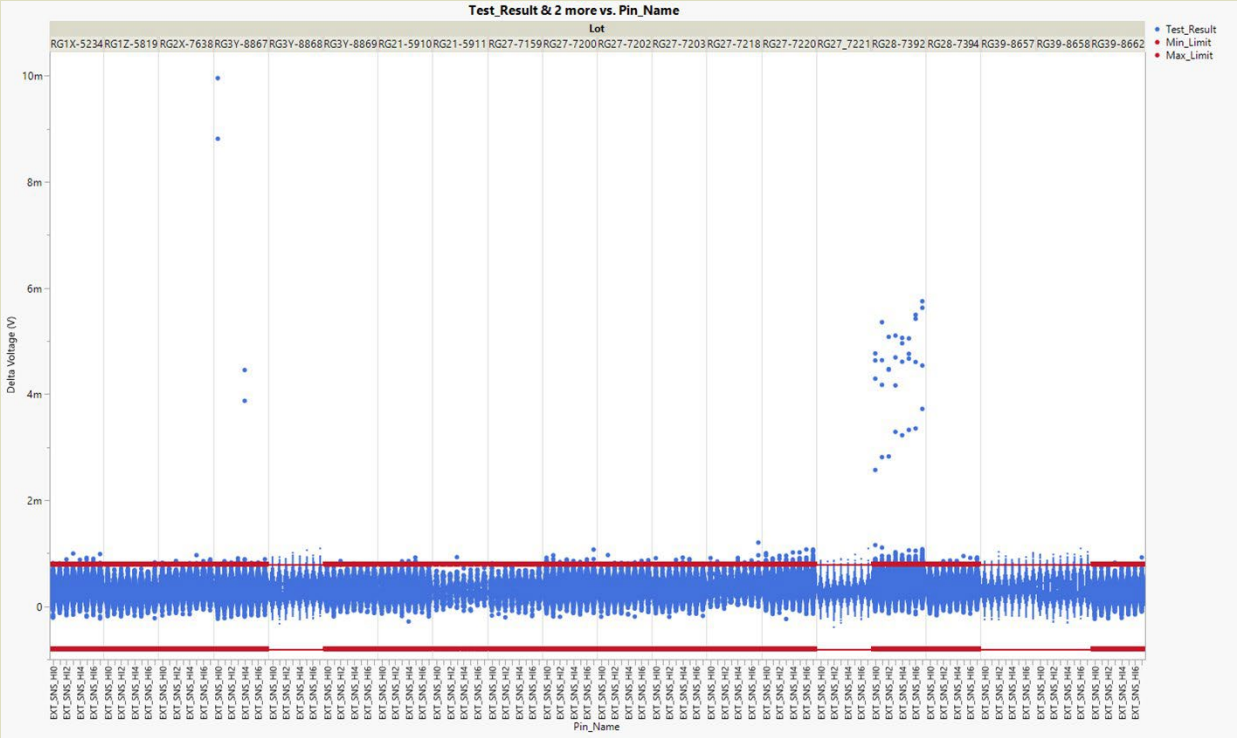


Figure 8: Qualification testing on ATE across various lots

Solution: ATE and Foundry Improvements

- Multi-faceted approach
  - **Short Term**: Developed targeted ATE screen
  - **Permanent Corrective Actions**: Foundry improvement for MIM capacitors

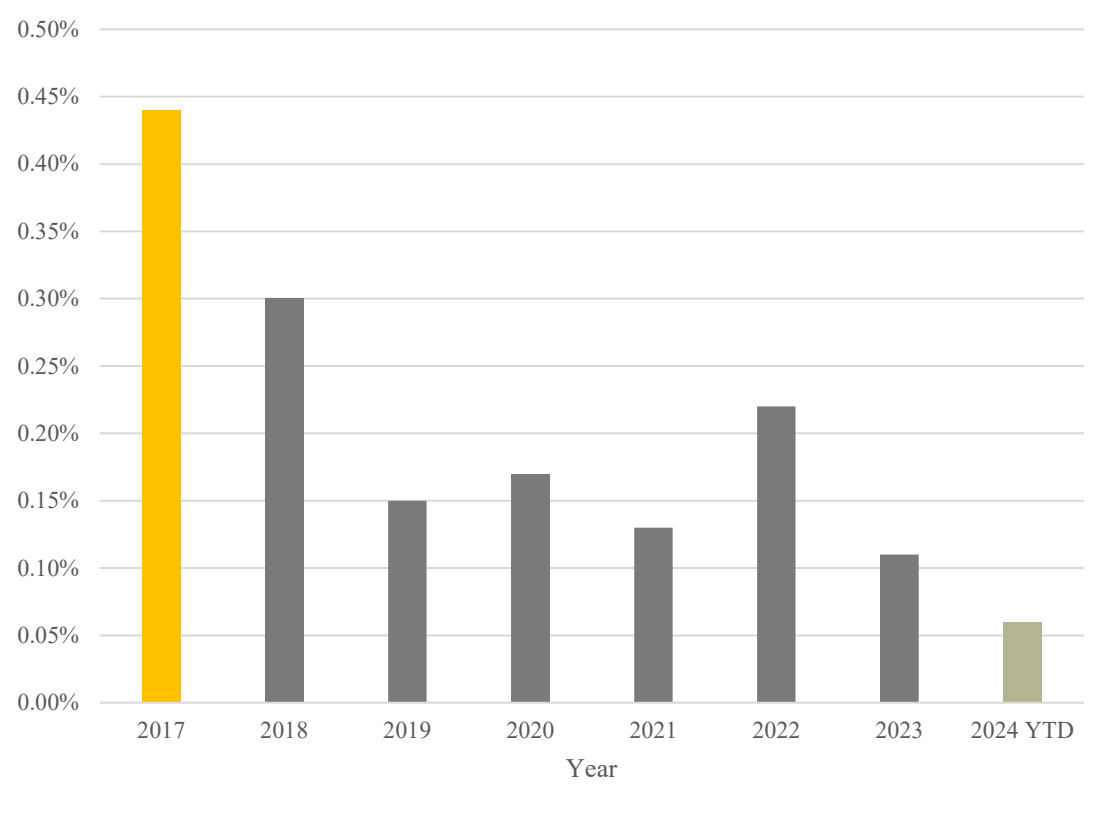


Figure 9: MIM Cap Failure Rate Improvement at New Foundry

Validation of Results

- Process improvement validated
  - Early Life Failure Rate (ELFR) qualification test over MIM caps based on JEDEC standard [5]
- Successfully identified MIM-cap related failures without yield loss
- Significantly reduced RMA process time
  - Multi-week root cause to days

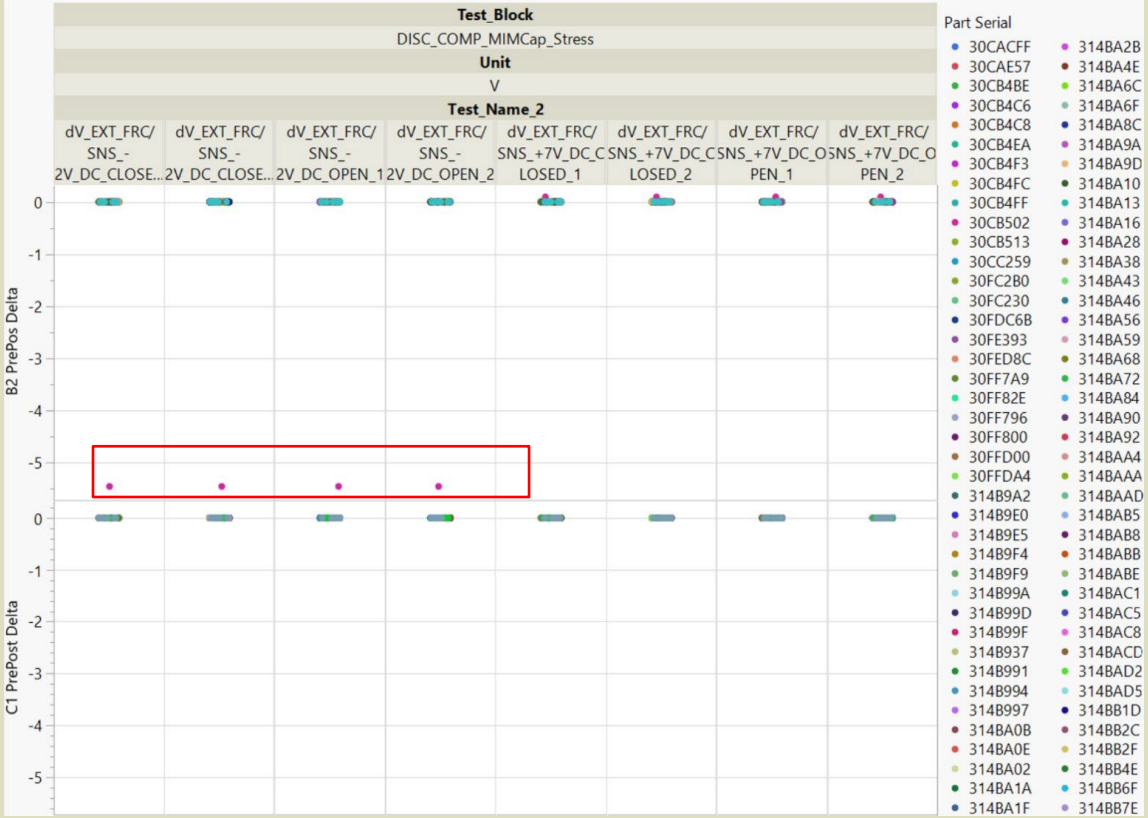
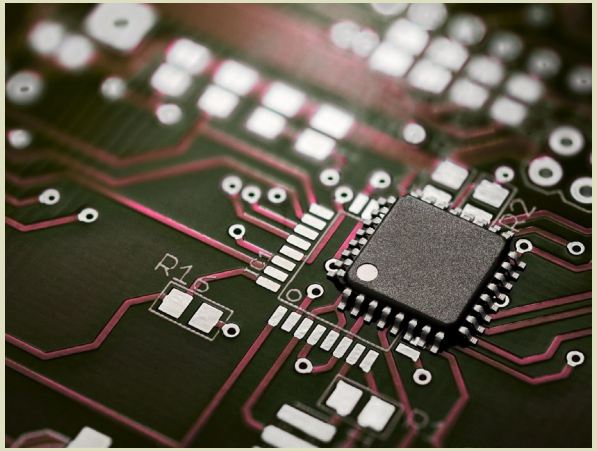
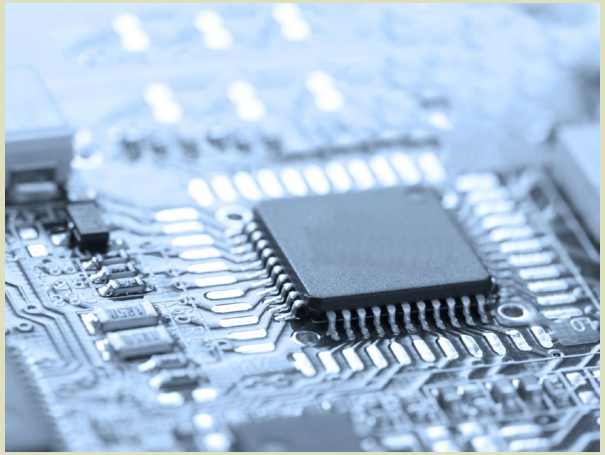


Figure 10:ELFR testing performed between foundries

Conclusion

- Effective test limits
  - Improved customer confidence
  - Rapid RMA resolution
- Collaboration accelerates problem solving
- Balance cost, effort, and implementation time
- Future Work
  - Monitor foundry Process Control Monitor (PCM) data
  - Correlate wafer-level data with test outcomes
  - Explore split wafer experiments





Sources

- [1] “Bathtub curve,” Wikipedia. [Online]. Available: https://en.wikipedia.org/wiki/Bathtub_curve [Accessed: Sep. 22, 2025].
- [2] E. Suhir, “Analytical bathtub curve with application to electron device reliability,” *Journal of Materials Science: Materials in Electronics*, vol. 26, no. 7, pp. 5205–5210, July 2015. doi: 10.1007/s10854-015-3263-1.
- [3] “GaAs IC Reliability in Plastic Packages, FA Approach on MIM (Metal-Insulator-Metal) Capacitor Failures,” International Symposium for Testing and Failure Analysis (ISTFA) Proceedings, ASM International, 2003. [Online]. Available: https://dl.asminternational.org/istfa/proceedings/ISTFA2003/30817
- [4] IST (Integrated Service Technology), “IC MIM Debug,” *IST Group Technical Articles*, Feb. 4, 2020. [Online]. Available: https://www.istgroup.com/en/tech_20200204-ic-mim-debug/.
- [5] JEDEC Solid State Technology Association, “JESD74A: Early Life Failure Rate Calculation Procedure for Semiconductor Devices,” JEDEC Standard, Nov. 2005. [Online]. Available: https://www.jedec.org/sites/default/files/docs/JESD74A.pdf

COPYRIGHT NOTICE

The presentation(s) / poster(s) in this publication comprise the Proceedings of the TestConX China 2025 workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the TestConX China 2025 workshop. This version of the presentation or poster may differ from the version that was distributed at or prior to the TestConX China 2025 workshop.

The inclusion of the presentations/posters in this publication does not constitute an endorsement by TestConX or the workshop's sponsors. There is NO copyright protection claimed on the presentation/poster content by TestConX. However, each presentation / poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

"TestConX", the TestConX logo, the TestConX China logo, and the TestConX Korea logo are trademarks of TestConX. All rights reserved.

TestConX中国 China

2025