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Test Insertions and Test Challenges for AI-HPC in CoW[P]oS Advanced Heterogeneous Integrated Packages

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TestConX中国™ China

November 13, 2025 – TestConX China 2025

"Generative AI's momentum is driving the massive demand for data center GPU and AI ASIC. Beyond that, **the whole ecosystem is being transformed**, involving CPUs, FPGAs, DPUs, network ASICs, and crypto ASICs. **The data center processor market will more than double in the next three years, surpassing $350B.**

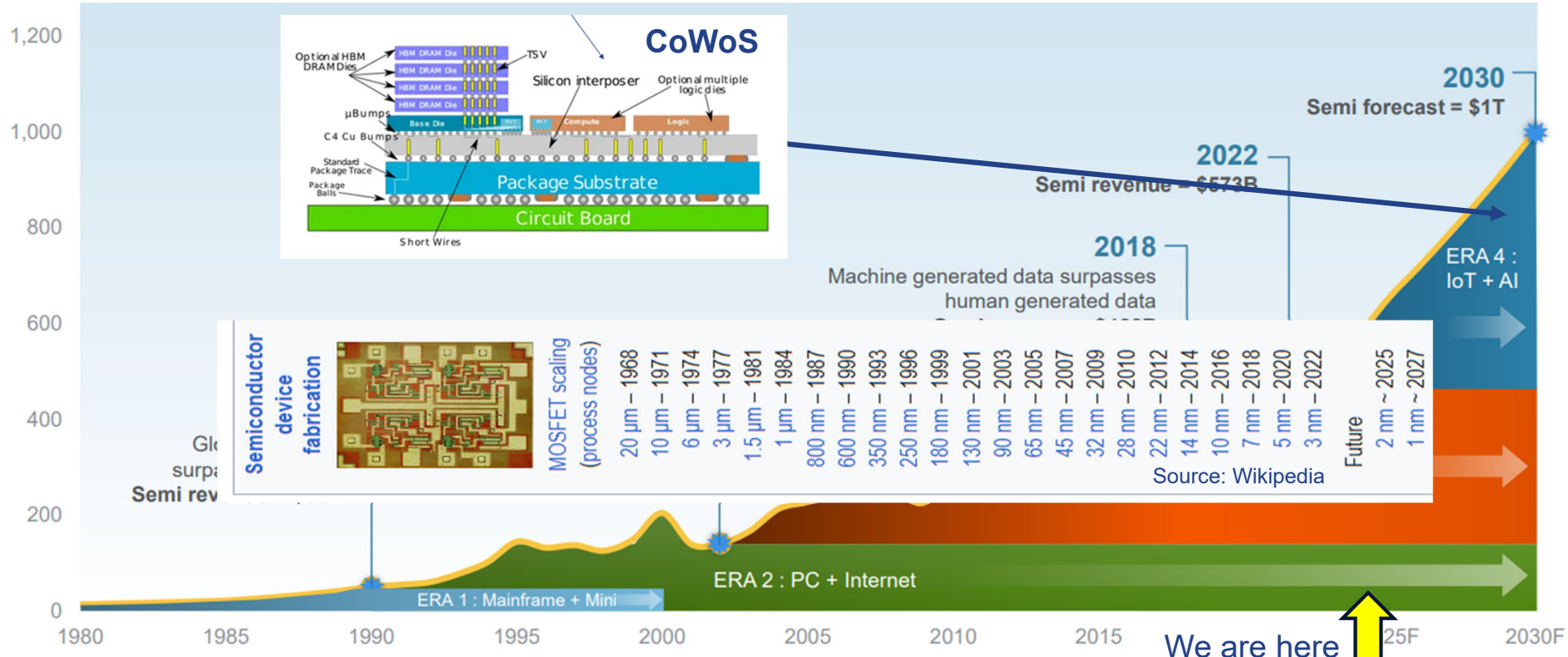
The **ASP of data center GPUs rose from $3K in 2020 to $16K in 2024 and is expected to reach $28K by 2030.** The average selling price (ASP) of GPUs is increasing due to a higher mix of flagship GPUs and the increase in GPU die size and HBM memory capacity.

Nvidia leads the AI race, but **Google and AWS are betting big on in-house AI ASICs**"

– *Yole Group, 2025*

From The Mobility Era to the AI Era: The Largest, Steepest Rise In Semi Revenues

Semiconductor Industry Growing to $1 Trillion by 2030



Source: https://ir.appliedmaterials.com/static-files/eba697b2-25c5-4ecd-a194-b08727636faa

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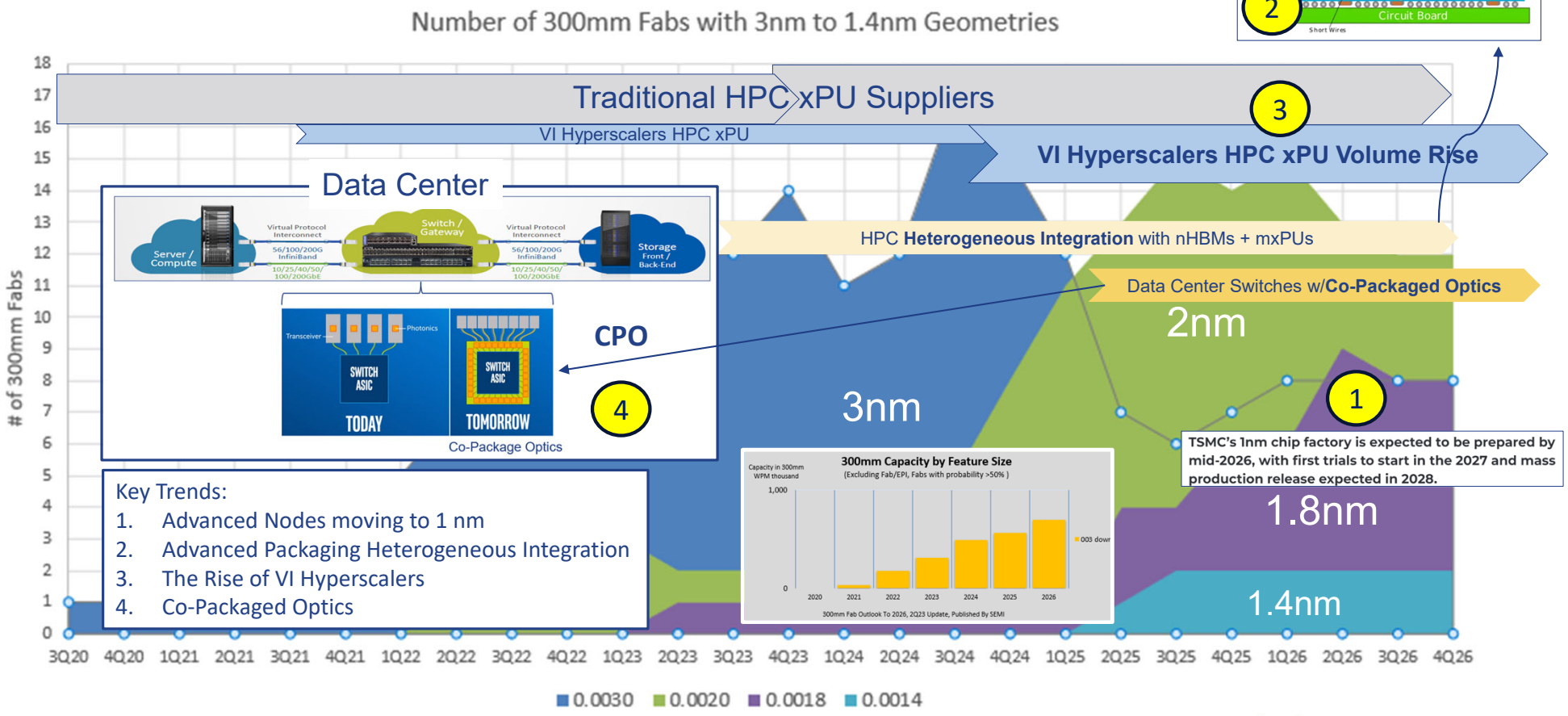
Key Trends Driving AI Data Center Computing Semiconductors Growth



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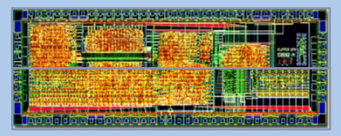
Industry Trends: Doubling of New Process Node Development Effort

Successful node adoption pressure on engineering tools including ATE for yield learning, peak production

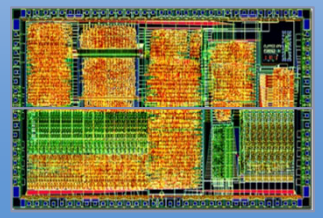
Advanced process nodes require more effort to go from design-to-production. **2X** effort for every node change.

This increase is also applicable to test engineering effort to develop a test program to achieve target quality and yield!

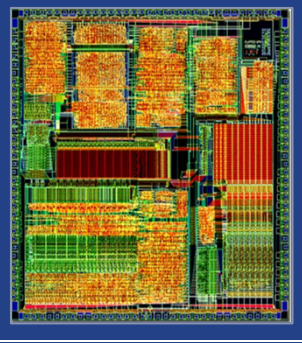
Advanced packaging (2.5D/3D) and heterogeneous integration driving KGD pressures



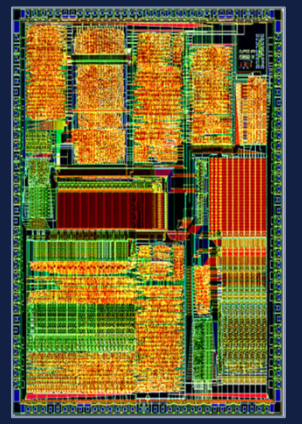
28nm
(100 Staff Years)



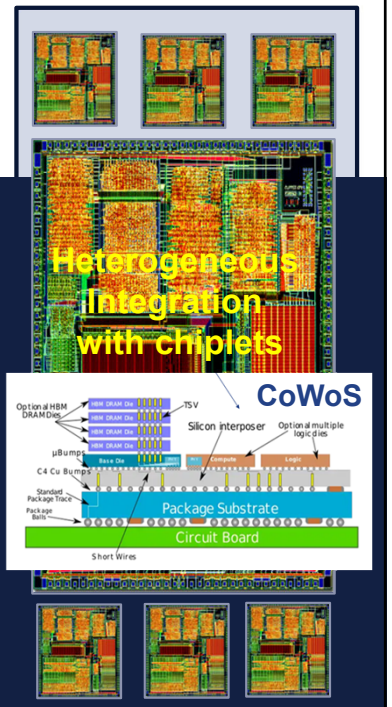
14nm
(200 Staff Years)



7nm
(500 Staff Years)



5nm
(1,000 Staff Years)



3-2nm
(2,000 Staff Years)

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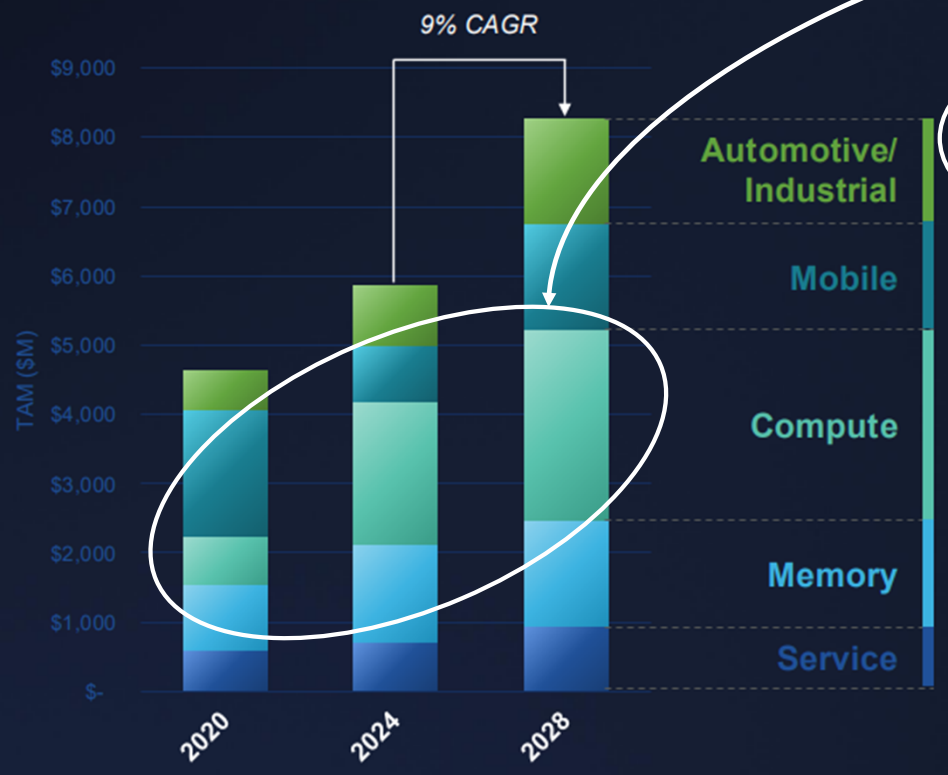
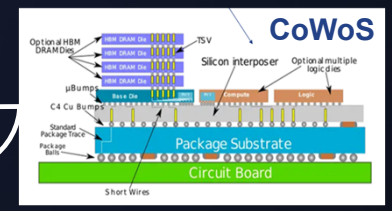
Semiconductor Test Midterm Outlook

ATE TAM History & Forecast



ATE Growth Drivers



AI Cloud Accelerators and Silicon Photonics

AI-featured Smartphones and Accessories

Expanding Automotive Electrification

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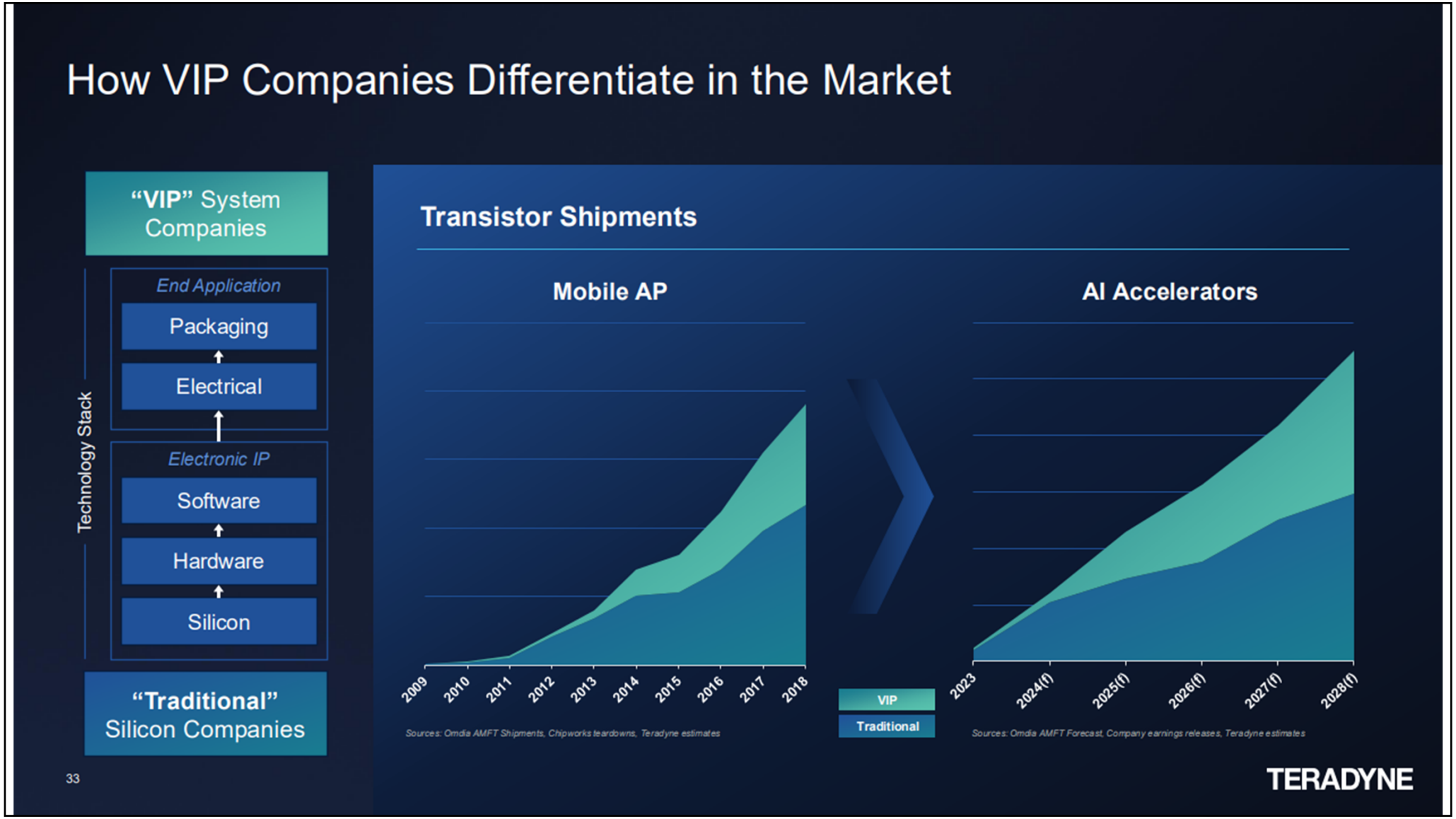
How VIP Companies Differentiate in the Market
"VIP" System Companies
Technology Stack
End Application
Packaging
Electrical
Electronic IP
Software
Hardware
Silicon
"Traditional" Silicon Companies
Transistor Shipments
Mobile AP
AI Accelerators
2009
2010
2011
2012
2013
2014
2015
2016
2017
2018
2023
2024(f)
2025(f)
2026(f)
2027(f)
2028(f)
VIP
Traditional
Sources: Omdia AMFT Shipments, Chipworks teardowns, Teradyne estimates
Sources: Omdia AMFT Forecast, Company earnings releases, Teradyne estimates
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Compute Segment Brings New Opportunities

- **AI accelerator and GPU complexity**
- **Networking bandwidth for AI datacenters**
- **Silicon photonics and co-packaged optics**
- **Power efficiency and yield improvements**

UltraFLEXplus ATE and Titan HP SLT test platforms

- **High-performance** testing
- **Scalable** ATE architecture
- **Comprehensive** silicon photonics and CPO solutions
- **High power** SLT with active thermal control

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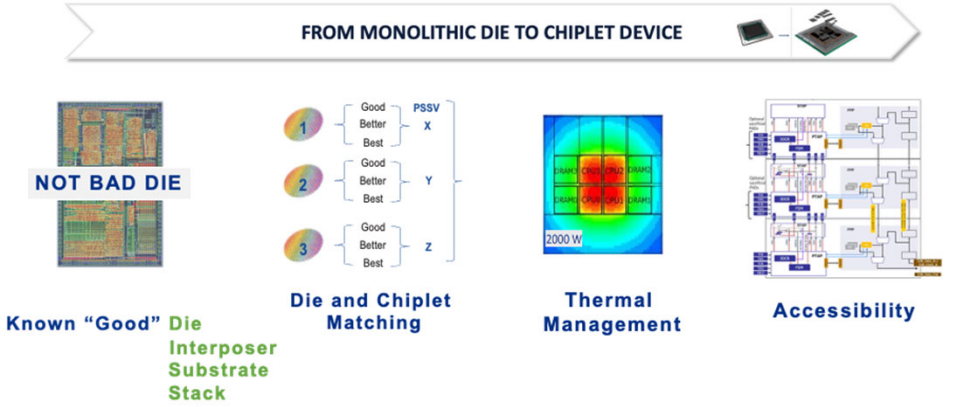
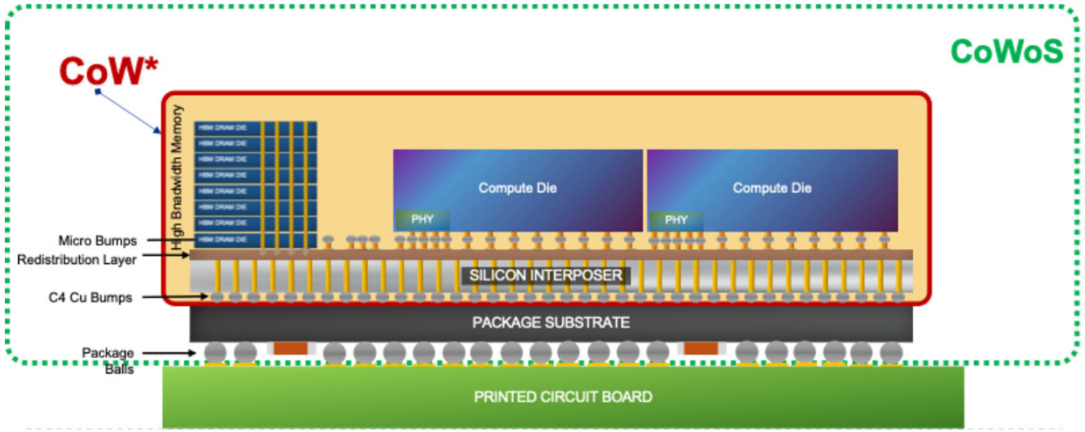
The Era of Complexity: From Monolithic to Chiplet Device





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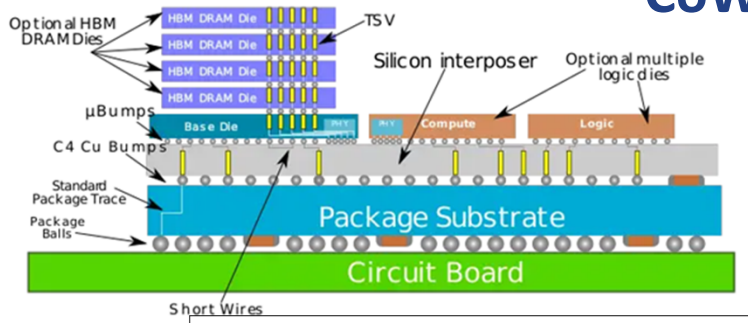
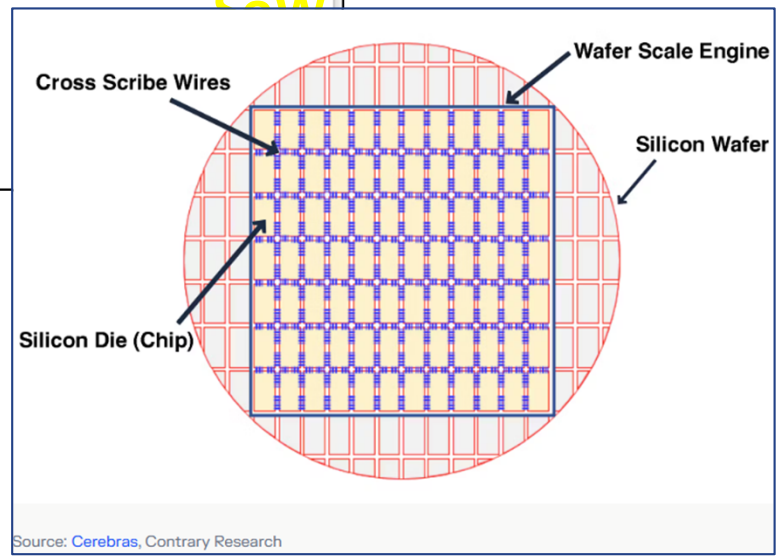
AI/HPC Advanced Packaging Terminology Definitions

CoWoS is a 2.5D wafer-level multi-chip packaging technology that incorporates multiple dies side-by-side on a silicon interposer in order to achieve better interconnect density and performance. Individual chips are bonded through micro-bumps on a silicon interposer forming a chip-on-wafer (CoW). The CoW is then subsequently thinned such that the TSV perforations are exposed. This is followed C4 bumps formation and singulation. A CoWoS package is completed through bonding to a package substrate.

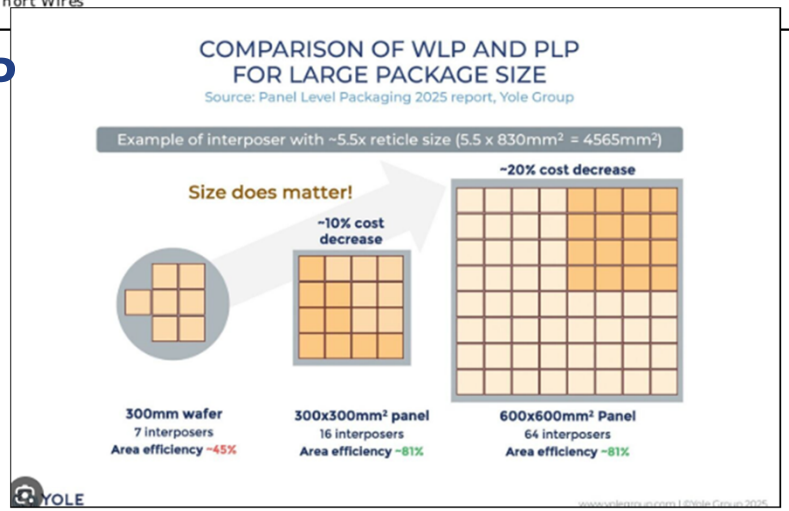
CoWoS



Wafer Scale Engine



CoP



Source: Various Internet Sources

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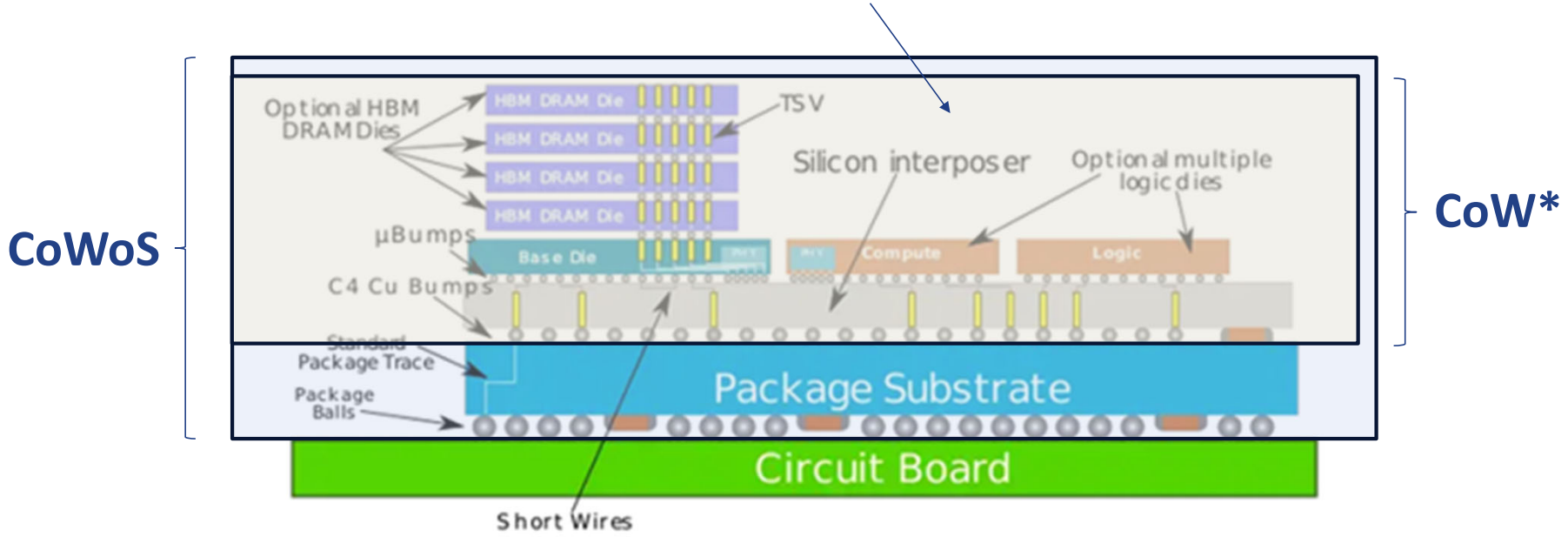
AI/HPC Advanced Packaging Terminology Definitions: CoWoS

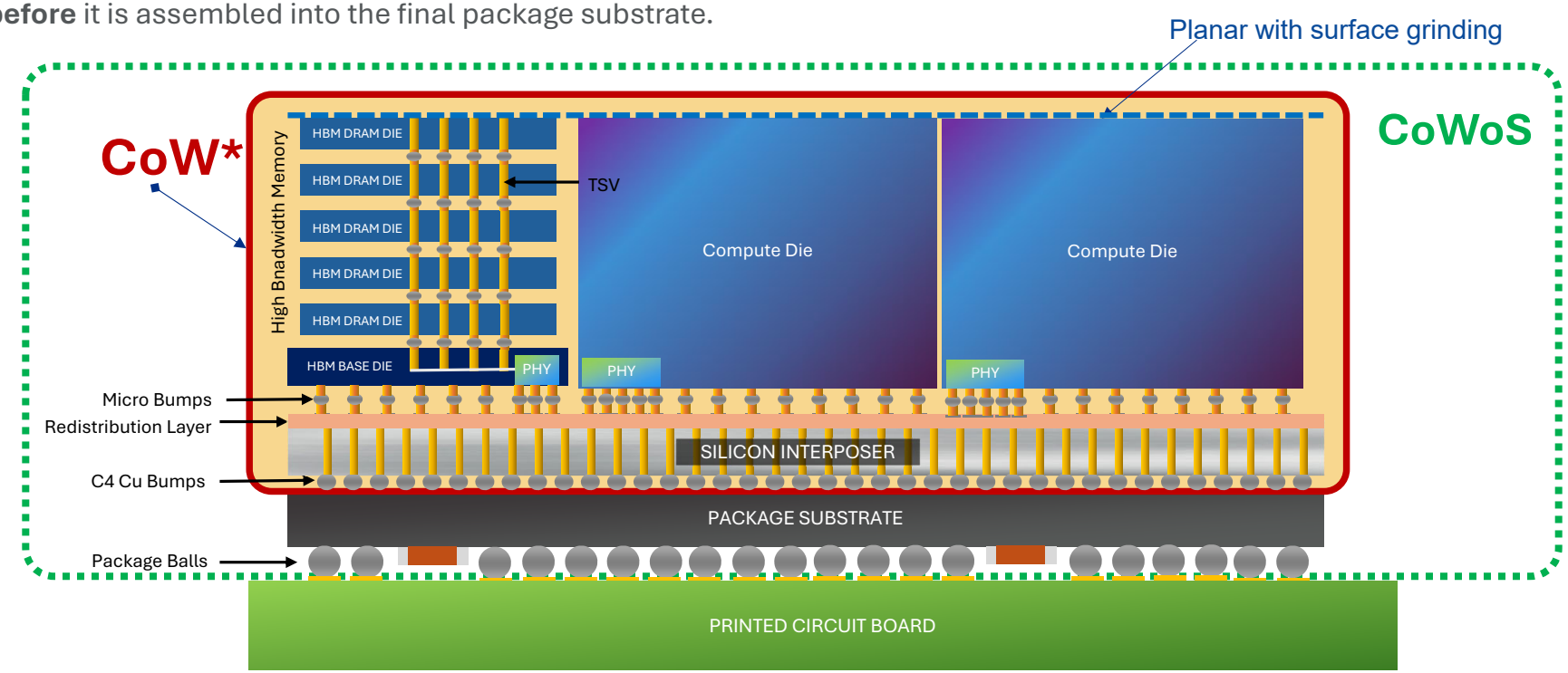
CoW needs a test insertion to verify the assembly integrity of the chiplet stack, uBumps, C4 Bumps interconnection **before** it is assembled into the final package substrate.



11 * Also known as “sub-assembly”, “mid-assembly”, “module”, etc.

Compute Advanced Packaging Terminology Definitions: CoWoS

CoW needs a test insertion to verify the assembly integrity of the chiplet stack, uBumps, C4 Bumps interconnection **before** it is assembled into the final package substrate.



* Also known as “sub-assembly”, “mid-assembly”, “module”, etc.

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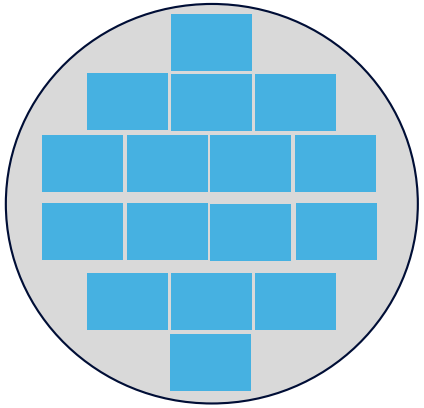
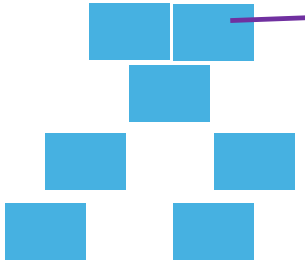
AI/HPC Advanced Packaging Terminology Definitions: CoWoS Possible Test Insertions

1. Wafer Sort

Compute Wafer

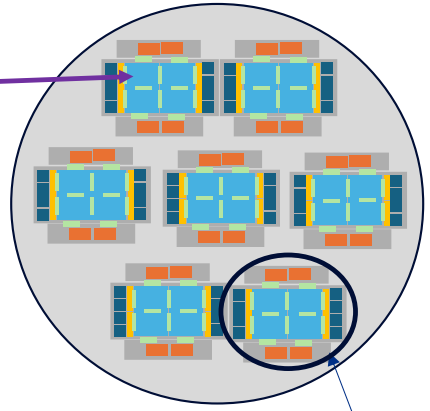


2. Singulated Die Test

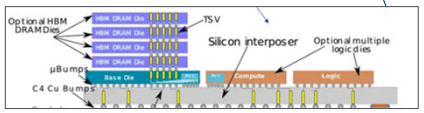


3. CoW Module Wafer Test

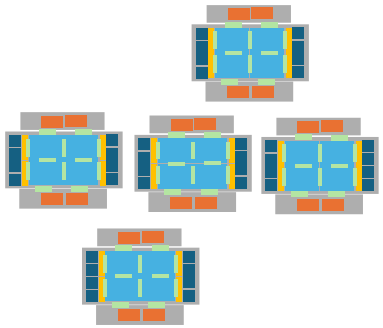
Interposer Wafer



CoW*



4. Singulated CoW Module Test

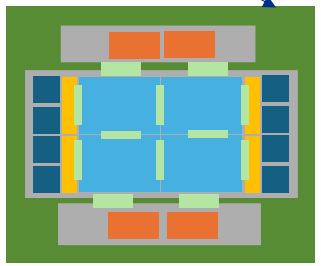


Test Cell Prober Upgrade Required

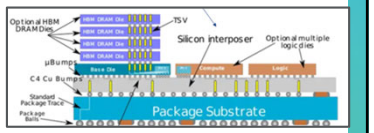
5. Package Test

FT or/and SLT?

Substrate



CoWoS



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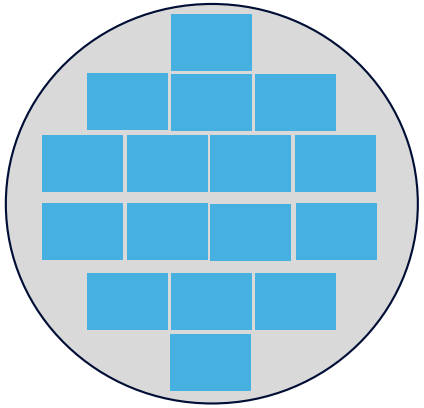
13 * Also known as “sub-assembly”, “mid-assembly”, “module”, etc.

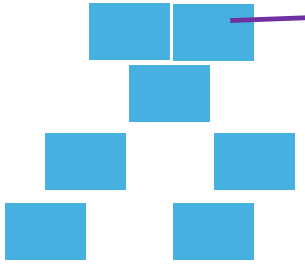
AI/HPC Advanced Packaging Terminology Definitions: CoPoS (310x310 mm) Possible Test Insertions

1. Wafer Sort

Compute Wafer

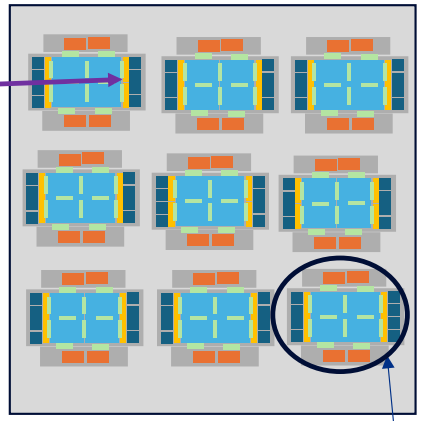


2. Singulated Die Test

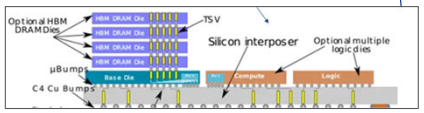


3. CoW Module Wafer Test

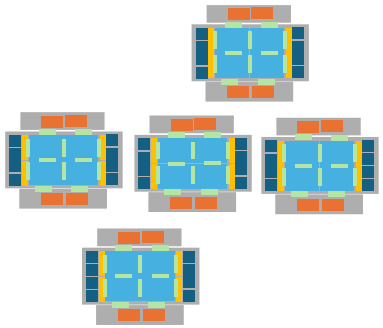
Interposer Panel



CoP*



4. Singulated CoW Module Test

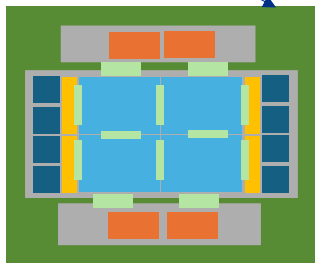


Test Cell Prober Upgrade Required

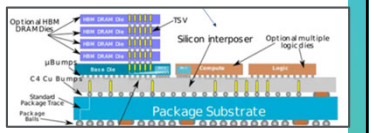
5. Package Test

FT or/and SLT?

Substrate



CoPoS



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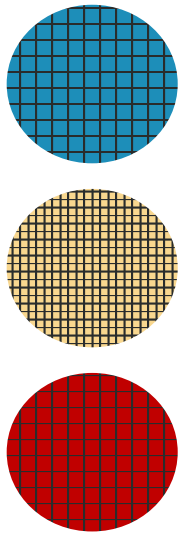
14 * Also known as “sub-assembly”, “mid-assembly”, “module”, etc.

"Interposer on Substrate" Advanced Packaging



Wafer Level Packaging

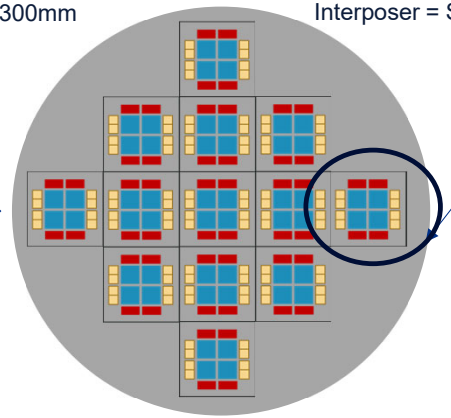
- Die are assembled on interposer
- 2, 2.5 and 3D
- Assembly is accomplished with wafer level process
- Interposers are **not** diced until assembly is complete - Or perhaps managed on wafer frame media?

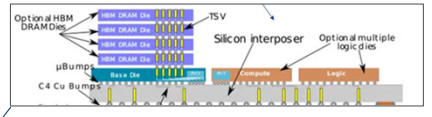
Panel Level Packaging

- Die are assembled on interposer
- 2, 2.5 and 3D
- Assembly is accomplished with wafer level process
- Interposers are **not** diced until assembly is complete - Or perhaps managed on wafer frame media?
- Higer space utilization and thus lower cost than WLP

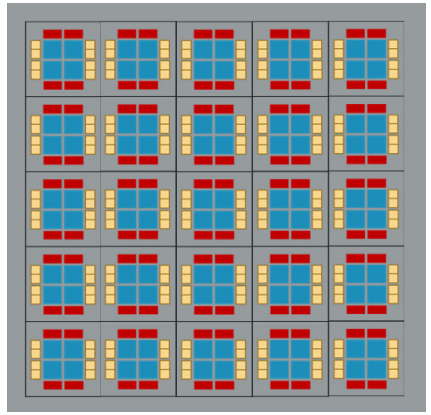
300mm

Interposer = Si





e.g. TSMC CoWoS

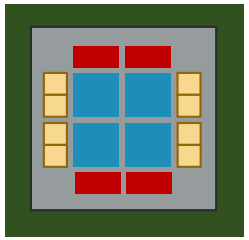


310mm x 310mm (enables media/handling compatible with wafer)

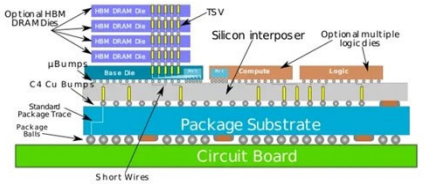
Interposer = Si?, Glass, Organic

Final Packaging

FT or/and SLT?



e.g. TSMC CoPoS



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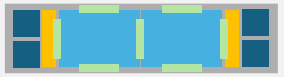
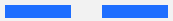
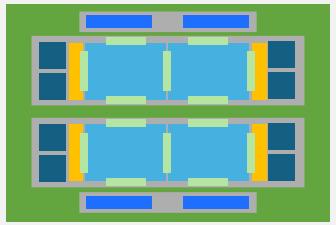
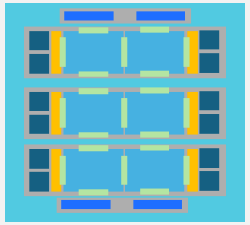
Advanced packaging is driving ATE TAM changes/growth with new insertions

Compute ASIC die	Singulated CoW module	AI Accelerator CoWoS Package	AI Accelerator CoWoP Package
	 Dis-aggregated I/O die 		

Insertions

WS – Wafer sort SD – Singulated die	SM – Singulated module	FT – Final Test SLT – System Level Test	?

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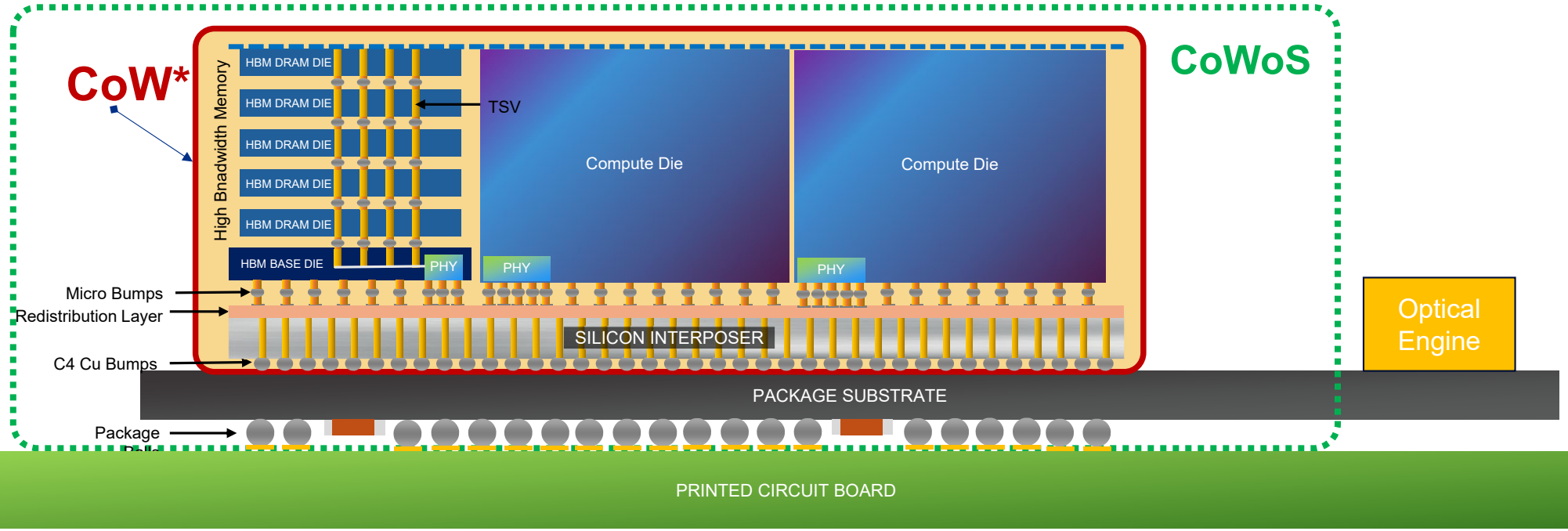
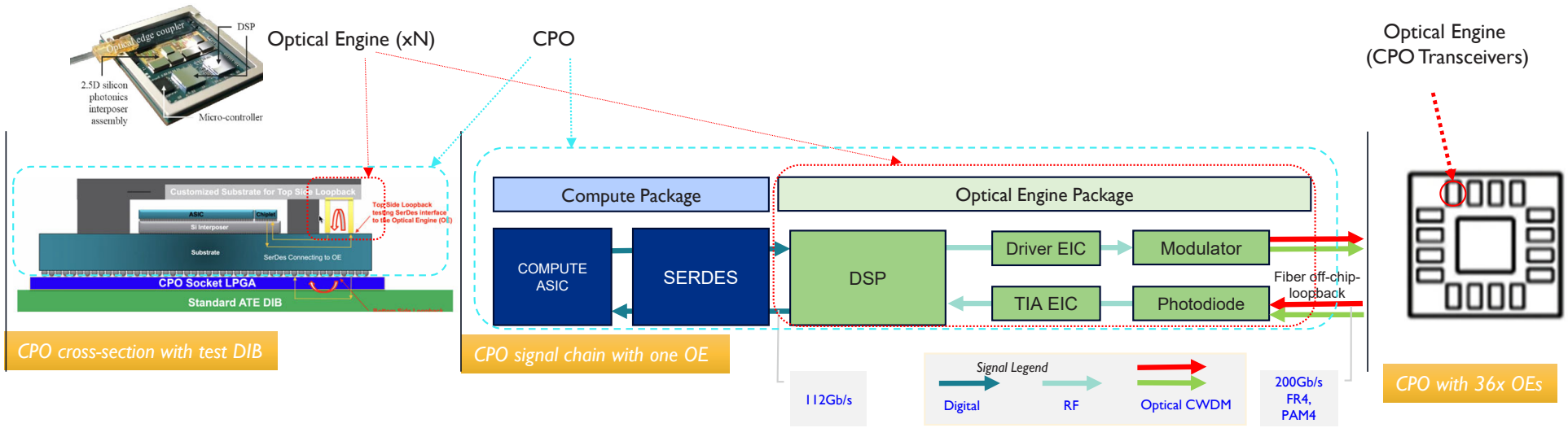
Co-Packaged Optics

Enabling 10x bandwidth at 30% lower power in the data center



* Also known as “sub-assembly”, “mid-assembly”, “module”, etc.

Optical Engine and CPO Definitions[1]



Optical Engine (*aka CPO Transceiver*) is a package which includes both EIC (TIA, Driver etc.) and PIC (SiPh die) in a single package. A DSP chip may also be present, however the compute die (Switch tile or x-PU) is not present in the optical engine. Optical engines are integrated into CPO modules.

CPO is a Module which includes Compute ASIC (Switch or GPU+HBMs) with SERDES Chiplet and Optical engines (x 4,8,16).

[1] *These definitions are in alignment with IEEE HIR Photonics Test document, and, Yole CPO 2023 report definitions.*

See also:

Co-Packaged Optics: Test Challenges for Data Center Technology of the Future

By Dr. Jeorge S. Hurtarte, Teradyne

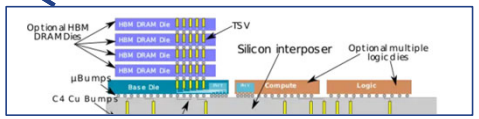
https://magazine.semiconductordigest.com/html5/reader/production/default.aspx?pubname=&edid=4e148f27-d423-45ec-8558-e412e5962332

TERADYNE

CoWoS (Chip-on-Wafer-on-Substrate) Metrology Opportunities

CoW – Chip-on-Wafer (individual chips are bonded through micro-bumps on a silicon interposer)

High value – evolution



Pre- bond inspection

- **Interposer fab**
  - TSV / iCAP: Communication between bottom side and top side (substrate and chips) and integrated capacitance
  - RDL: Fine pitched metal layers for routing and signal distribution between chips and substrate
  - Micro-bumping or Hybrid bond surface preparation
- **Die placement**
  - KGD: Logic dies and HBM stacks are placed onto the interposer with high precision
- **Micro-bump bonding**
  - Bonding can move to hybrid bonding for higher density and tighter pitch pushing below 10-11um pad pitch

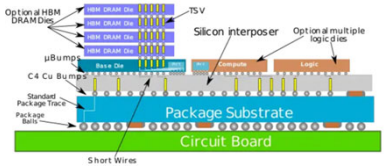
Post-bond

- **Underfill Encapsulation**
  - Underfill material is applied to fill the gaps between the dies and the interposer – this enhances mechanical strength and thermal management of the package

WoS – Wafer on Substrate

AOI*

- **Interposer Thinning**
  - Interposers are prepped and thinned down to expose the TSV
- **C4 Bump formation**
  - Larger C4 bumps are formed on the bottom side of the interposer



- **Package singulation**

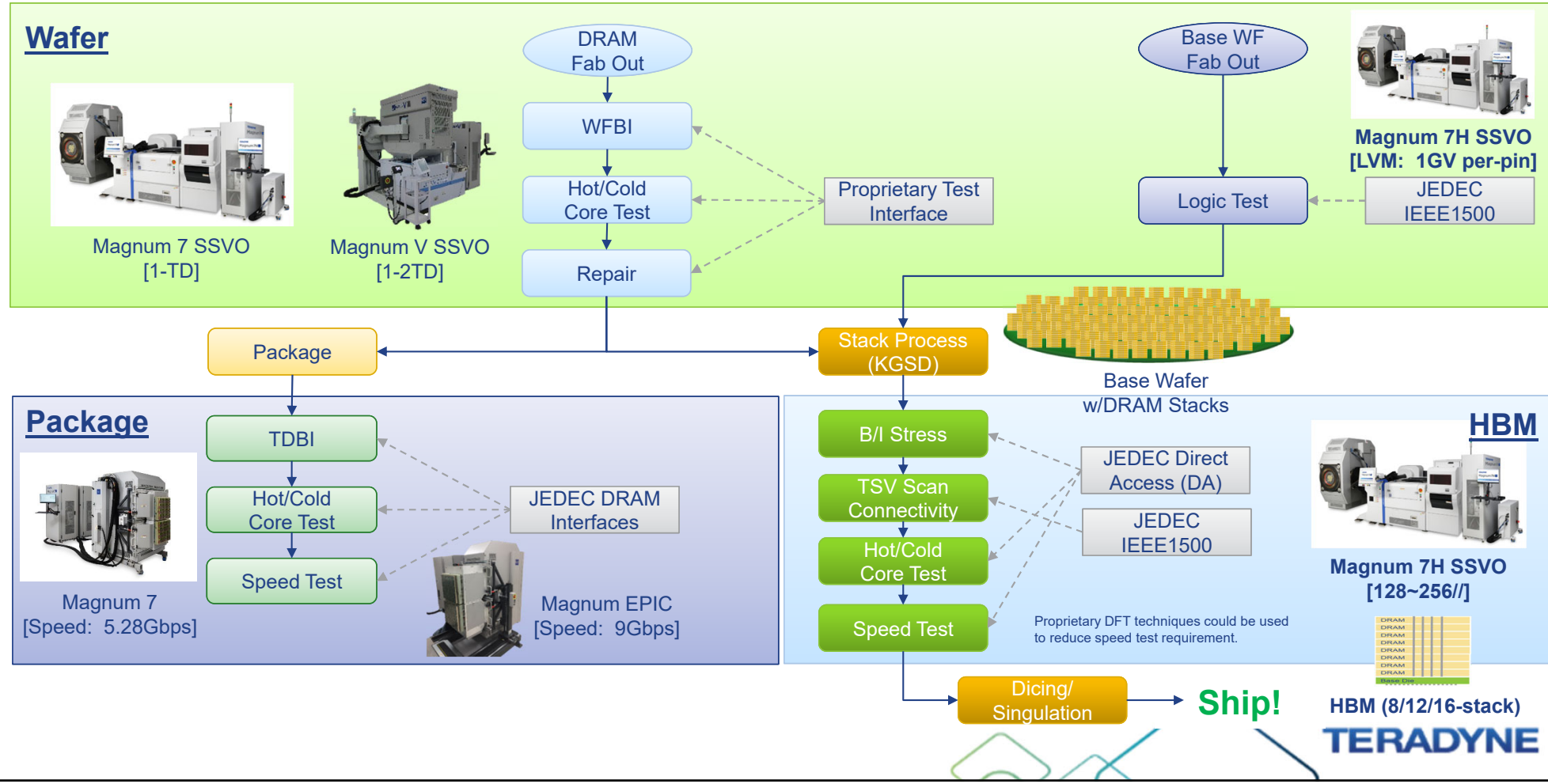
Post-bond

- **Substrate bonding**
  - The interposer is bonded to the substrate completing the package assembly

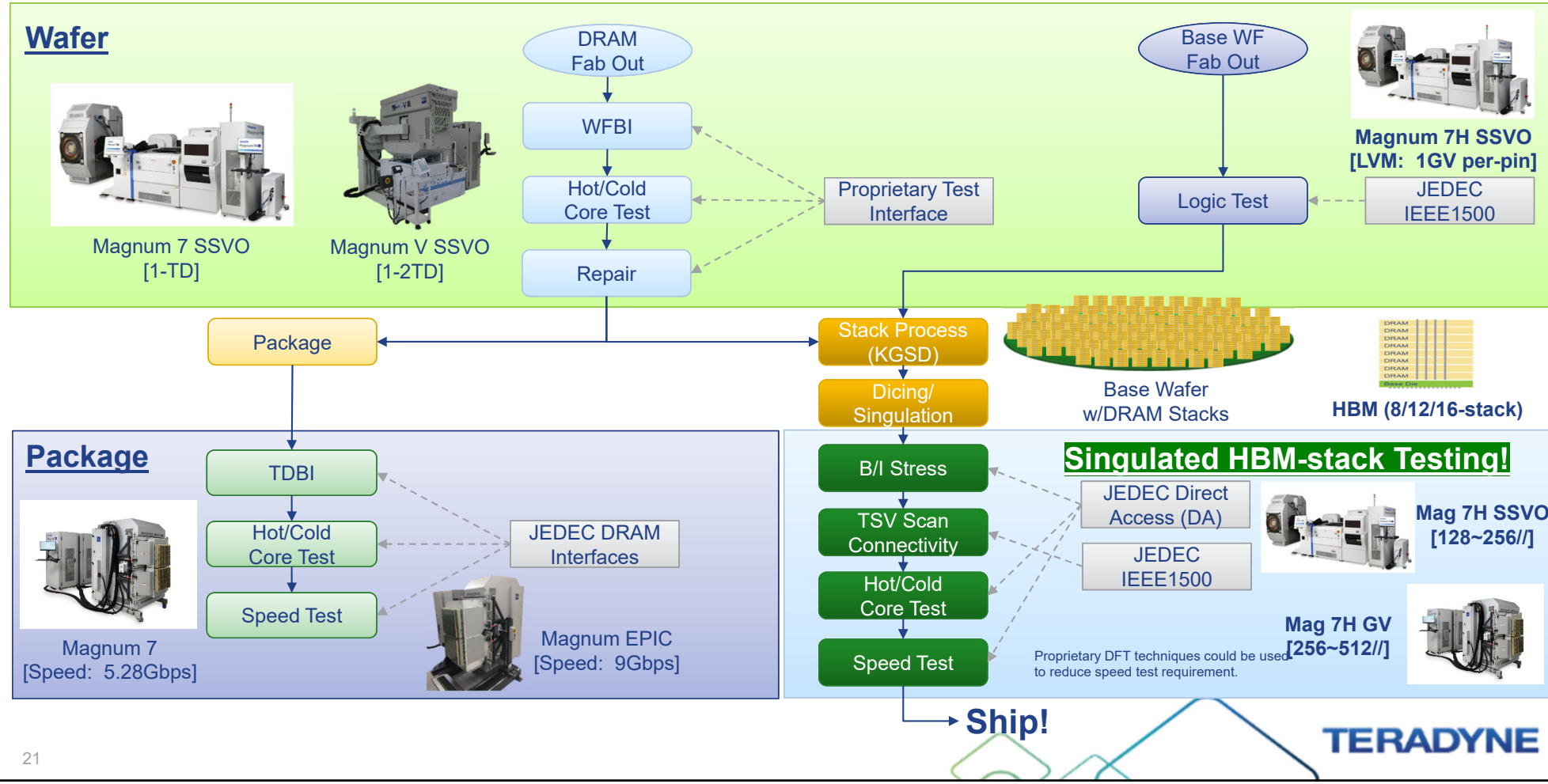
* AOI: Automated Optical Inspection

TERADYNE

Manufacturing Test Steps for Conventional DRAM vs. HBM



New Manufacturing Test Steps for *Singulated* HBM

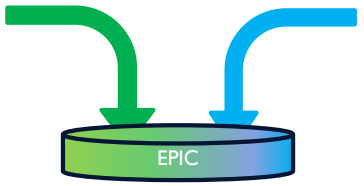


Possible Silicon Photonics and CPO Test Insertions

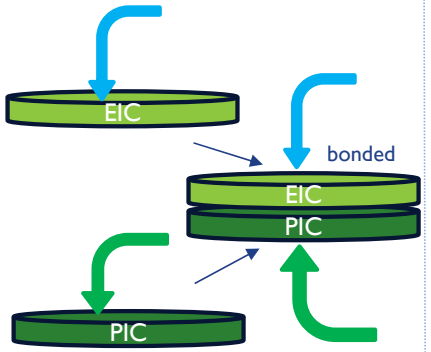
ATE | In-Circuit Test | ATE or SLT

Wafer Test | Die Test | Optical Engine Test | Multiple-Up Panel Pluggable PCA Assembly Test | CPO Module Test

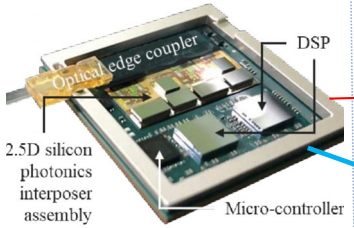
Foundry Approach I
Simultaneous PIC, EIC on same side of the wafer



Foundry Approach II
Wafer Bonding Technology.

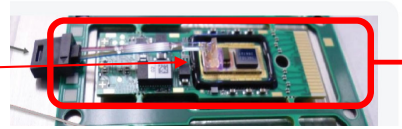


Die test
- Edge couplers
- RF Parametric Test
- Ideally, die test migrates to wafer level reducing COT and test insertions



Optical Engine
- Multi-die package (EIC+PIC) with BGA pins at the bottom
- Loop back high speed
- Parametric
- No compute die present (Switch or x-PU)

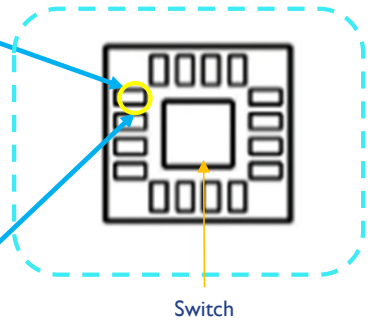
Definitions
PIC: Photonics IC
EIC: Electronics IC
CPO: Co-packaged Optics



Multiple Up-panel Pluggable Assembly
- Connector, Fiber Array, Light Source, Si Pho IC, Electronics IC
- Tests:
  - Open / Shorts
  - Resistor / Capacitor Measurements
  - Other discrete components test
  - Optical connector alignment test

Pluggable Module

CPO Module



Optical Engines xN

Photonics KGD a Must for CPO $S and reliability!

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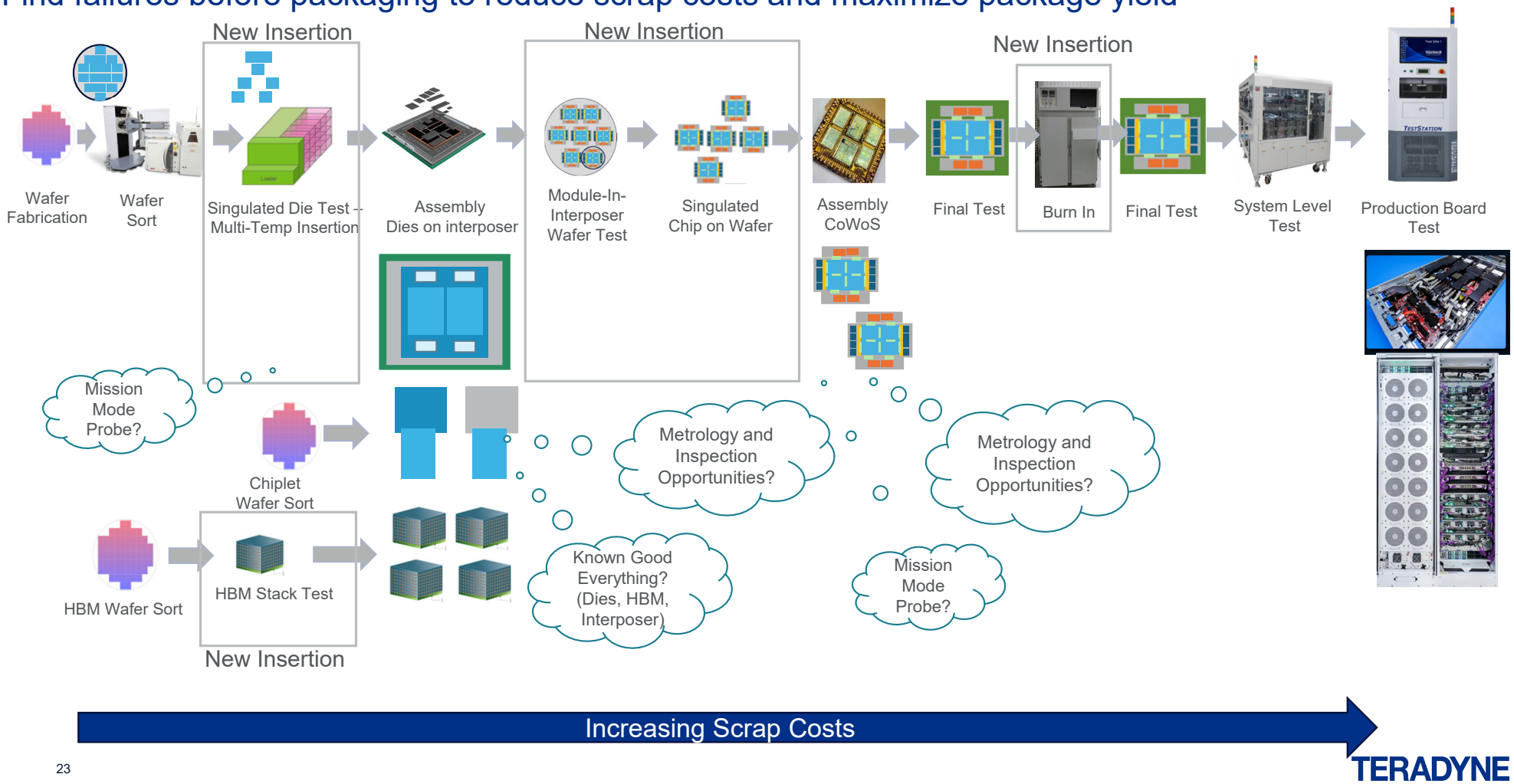
Test Flows in the AI Era:

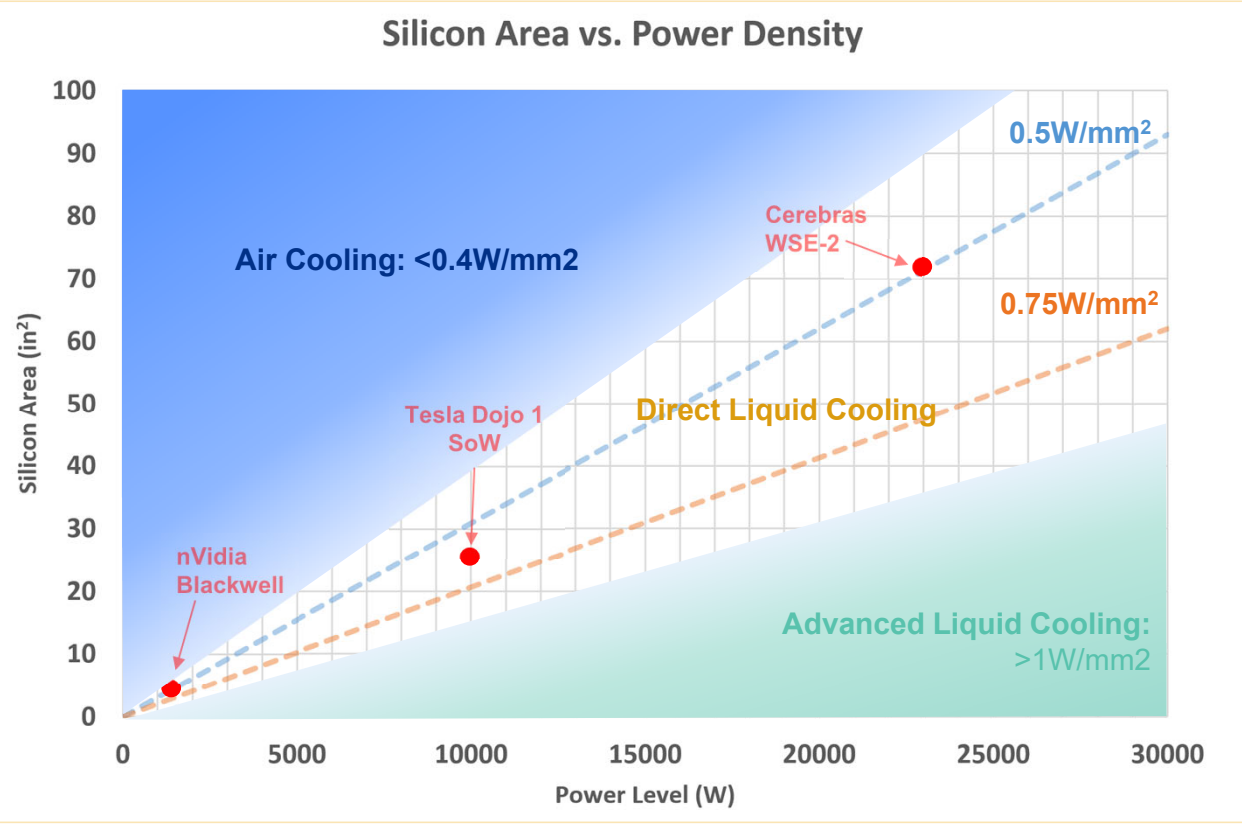
Find failures before packaging to reduce scrap costs and maximize package yield



23

TERADYNE

Advances in Thermal Management Enable Higher Device Power



- Device power density is exceeding the capability of air cooling
- Direct liquid cooling enables high power density on large devices today
- Silicon micro-channel and immersion cooling schemes will enable even higher power density in the future
- **Sources:**
  - IEEE: Establishing the Single-Phase Cooling Limit for Liquid-Cooled High Performance Electronic Devices
  - IEEE: InFO_SoW (System-on-Wafer) for High Performance Computing | IEEE Conference Publication | IEEE Xplore
  - Microchannel: TSMC Mulls On-Chip Water-Cooling for Future High-Performance Silicon | Extremetech

TERADYNE

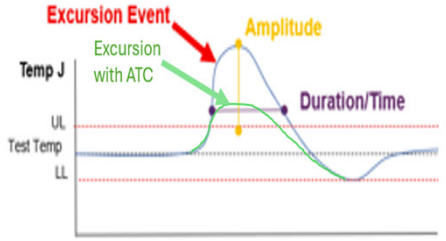
Active Thermal Control Challenges

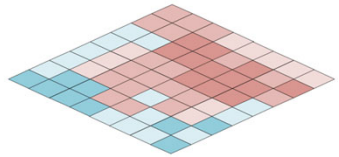
Rapidly Increasing Test Power requirement
Test power growing to 5kW and beyond, driven by coverage “shift left” and mission-mode functional test

Reduced Thermal Guardband
Increase test coverage and yield even as power increase requires more precise junction temperature control

Multizone Control
Large Die and Multi Chip Packages are driving up the number of power domains and thermal zones that require individual thermal analysis and control

Power and Thermal Telemetry
Large data volume for real time thermal control
data logging and profiling for test optimization and machine learning





Intelligent Power: Native DUT Interface Features

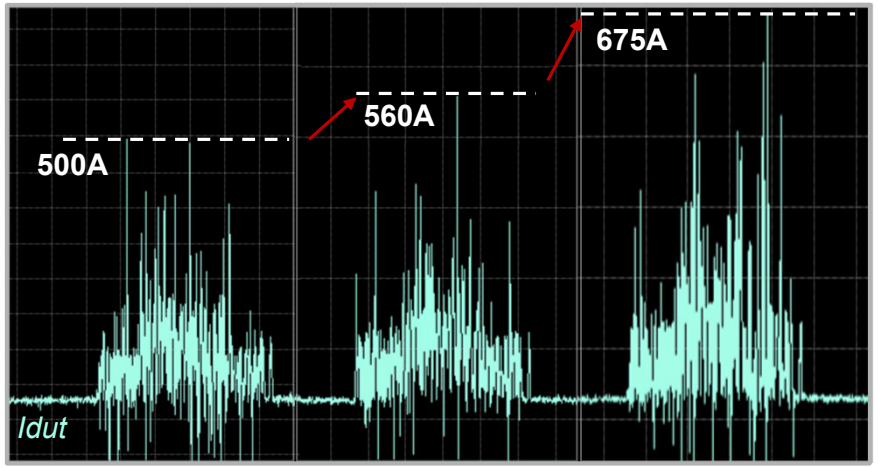
Enabling Comprehensive Functional Testing

Device Power Throttling

Native programmable power throttle signal from the instrument to the DUT

- Safely push to real-world condition limits (like SLT)
- Accurate power/performance trimming and binning

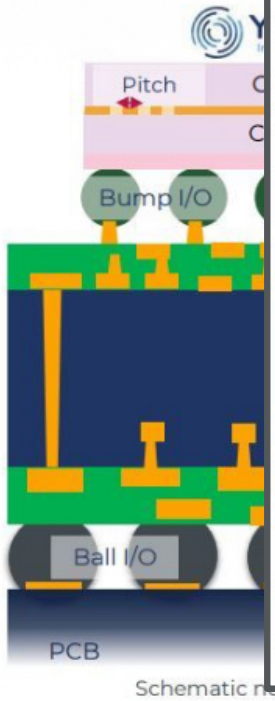
Mission-Mode Functional Test on ATE Example



Adjustable throttle threshold allows the device to safely be tested at its full performance limits

TERADYNE

ADVANCED PACKAGING ROADMAP: I/O PITCH AND RDL L/S



Schematic not drawn to scale

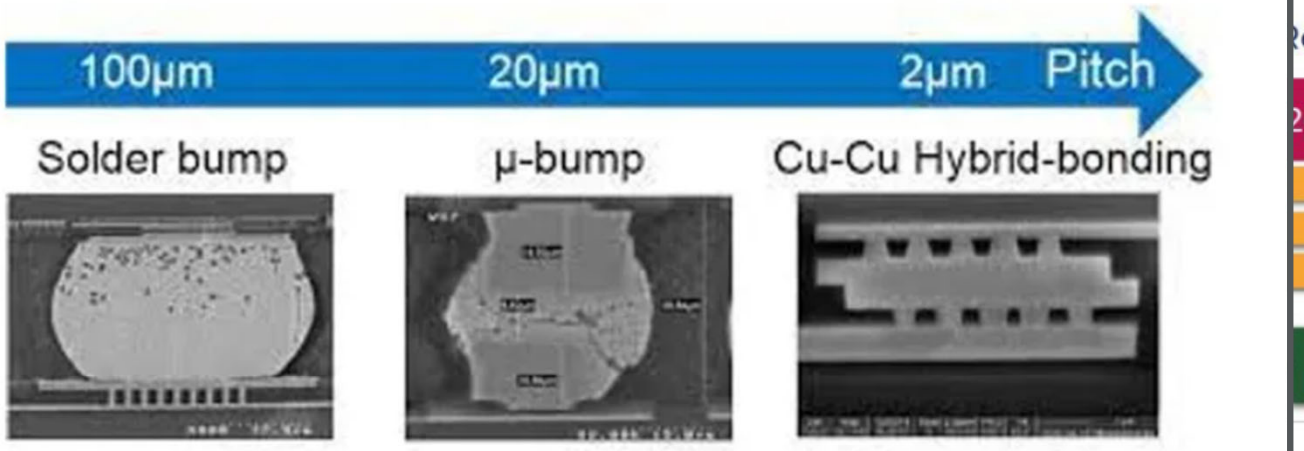


Image Credit: Imed Jani. Test and characterization of 3D high-density interconnects. Micro and Nanotechnologies/Microelectronics. Université Grenoble Alpes, 2019. English. NNT : 2019GREAT094 . tel-02634259

Roadmap

2023... ...2027

<0.5µm

< 10 µm

10 - 40 µm

50 to 40 µm

>2/2 µm

300 µm

nclude R&D capability.

Bump I/O pitch is scaling much faster than Ball I/O pitch which drives a finer RDL L/S at IC substrate package level.

https://semiengineering.com/the-rise-of-panel-level-packaging/

TERADYNE

Silicon Photonics and CPO Test Challenges

	Wafer	Optical Engine	Co-Package
The number of silicon photonics devices is growing – driving the need for higher throughput, automated production test solutions	✓	✓	✓
Test optical and electrical signals in the same insertion • Optical and electrical instrumentation integrated into the same tester • Laser sources, power meters, optical switches	✓	✓	✓
Align optical fiber to optical I/O on wafer • Repeatable sub-micrometer alignment of fiber to DUT • Various fiber coupling types: Grating coupling, edge coupling	✓		
"Double sided" Probing – Device architecture may require making electrical contact on one side of the wafer and optical measurements from opposite side	✓		
High Speed Digital Testing – 56 GHz → 112 Gbps → 224 Gbps • O2E, E2O, E2E w/ Optical loopback	✓	✓	✓
Customized Material Handling and optical connectors		✓	✓
Thermal Management • Optical engines co-packaged with 2000 W+ AI hardware			✓

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Optical Engine Device Trend and Product Needs

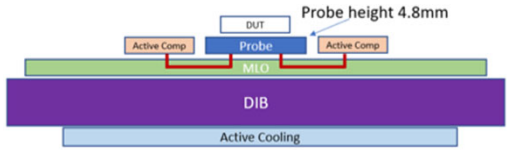
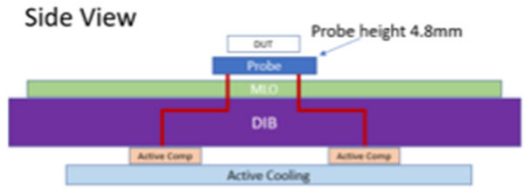
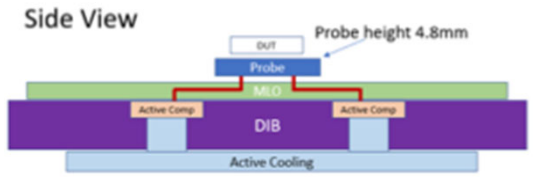
Product Test Needs

1. Provide high channel count laser sources and power meters with the flexibility to choose wavelengths and re-route lasers to DUT inputs without sacrificing power at the DUT because of switch and connector insertion loss
2. Provide flexibility to add tunable laser and polarization control if needed
3. Reduce test cell footprint impact from optical instrumentation – optical instrumentation should be another option that does not impact the size of the test cell

	Today	Future (1-5 years)	Future (5+ years)
Applications	Pluggable, CPO w/ Switch, CPO w/ XPU	Pluggable, CPO w/ Switch, CPO w/ XPU	Chip to chip
Optical Fibers	4-42	80-200	500-1000+
Fiber Type	SM/PM	SM/PM	In chip waveguides
Laser Source Channels	4-8	8-16	
TX/RX Channels	4-32	32-128	
Wavelength	Primarily O-band	O-band, L-band, C-band	
Multi-plexing	Primarily single wavelength	Multiple wavelengths, CWDM	
Data Rate	100-224 Gbps	448 Gbps	
Laser Source Power	>23 dBm	>23 dBm	23 dBM, Power requirement could be lower because distances are extremely short between chips
Modulation	NRZ PAM4	PAM4 PAM8	
OE per CPO	4-36	36 (higher bandwidth per OE)	Chip to chip optical interface through interposer
Tunable laser required for test	Yes – test at target wavelength plus alignment debug	Yes (may be required as wavelength spacing gets more-dense 10 nm today → 1-2 nm in future)	

Test Strategies for Chiplet I/O with low drive strength, ex: UCIe

Test Strategy: bring the test interface for a native chiplet, die-to-die high speed interface as close to the DUT as possible

Config 1: *on MLO*		***Distance from DUT***: 10 to 15 mm, similar to final application ***Signal Integrity***: *Lowest parasitic losses: short trace, near outer layers* ***Thermal Management***: Passive cooling ***Active Die Attach***: Flip chip, bare die attach for minimal probe height
Config 2: *under PCB*		***Distance from DUT***: 20 to 30 mm ***Signal Integrity***: *Parasitic loss through PCB (via transitions and materials)* ***Thermal Management***: Active cooling, extension of test head cooling ***Active Die Attach***: BGA, conventional package
Config 3: *"sandwich"*		***Distance from DUT***: 15 to 20 mm ***Signal Integrity***: *Parasitic loss through MLO* ***Thermal Management***: Active cooling, extension of test head cooling ***Active Die Attach***: BGA, conventional package in a PCB cavity

TERADYNE

2.5D/3D Advanced Packages Test Challenges *

- **Known Good Die (KGDs)**
  - Chiplets should see as much testing at wafer probe as possible.
  - Design-for-Test (DFT) solutions should enable high test coverage at wafer probe
  - **IEEE 1838** ***IEEE Standard for Test Access Architecture for 3D Stacked Integrated Circuits*** should be used to apply tests pre- and post-packaging.

- **Known Good Interposers (KGI)**
  - Interposer testing can be accomplished primarily by point-to-point continuity probing.
  - **Known good interposers (KGI)** are vital to ensure adequate yields for advanced packages.
  - For post-package assembly, IEEE P1838 primary and secondary TAP ports allow for testing the die-to-die test access and interconnect performance integrity.

* https://eps.ieee.org/images/files/HIR_2024/HIR_2024_ch17_Test_Technology.pdf, pages 75-79

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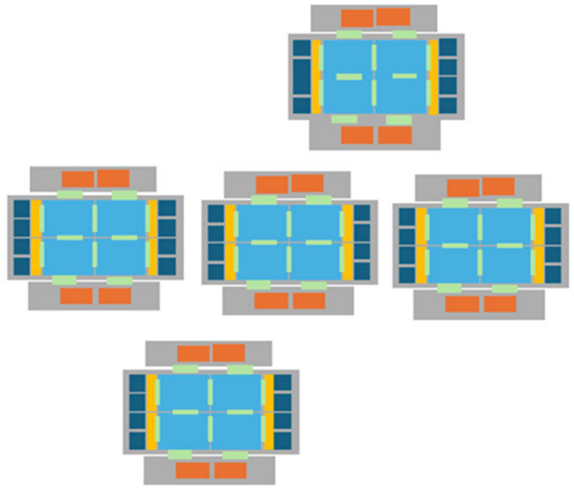
2.5D/3D Advanced Packages Test Challenges

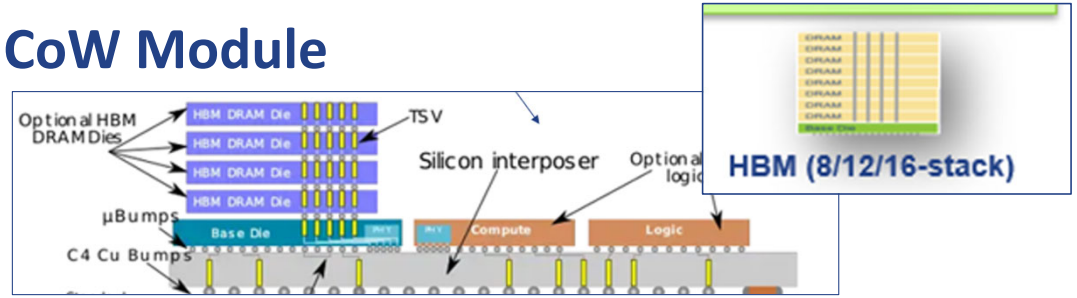
- **Known Good CoW and HBM-stack modules**
  - CoW needs a test insertion to verify the assembly integrity of the chiplet stack, uBumps, C4 Bumps interconnection before it is assembled into the final package substrate.
  - HBM-stack needs testing prior to CoW

4. Singulated CoW Module Test

Test Cell Prober Upgrade Required



CoW Module



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2.5D/3D Packages Test Challenges *

- **High speed interconnects and signal integrity**
  - **JTAG 1149.1 or 1149.6, SPI, J2C (JTAG to CPU), or PCIe** tests at wafer sort, package test and system test in characterization and production.
  - Need innovation on production test solutions for multiple optical port photonic devices.
  - 3D interconnects can exceed 100,000 and are becoming increasingly denser (< 3µm),
  - A future trend is for the industry to develop a standardized test and repair methodology that considers these trends in 3D interconnects

- **3D TSV Interconnect**
  - Silicon interposers include interconnect and through-silicon-via (TSV) structures.
  - Mechanical integrity of these structures during the manufacturing process ensures electrical performance.
  - **DC and AC transient pre-bond testing of interposers helps in screening micro-void and pinhole defects.**
  - Testing of interposers may require custom test fixture development and test insertion,
  - Custom implementations may require complex test techniques

* https://eps.ieee.org/images/files/HIR_2024/HIR_2024_ch17_Test_Technology.pdf, pages 75-79

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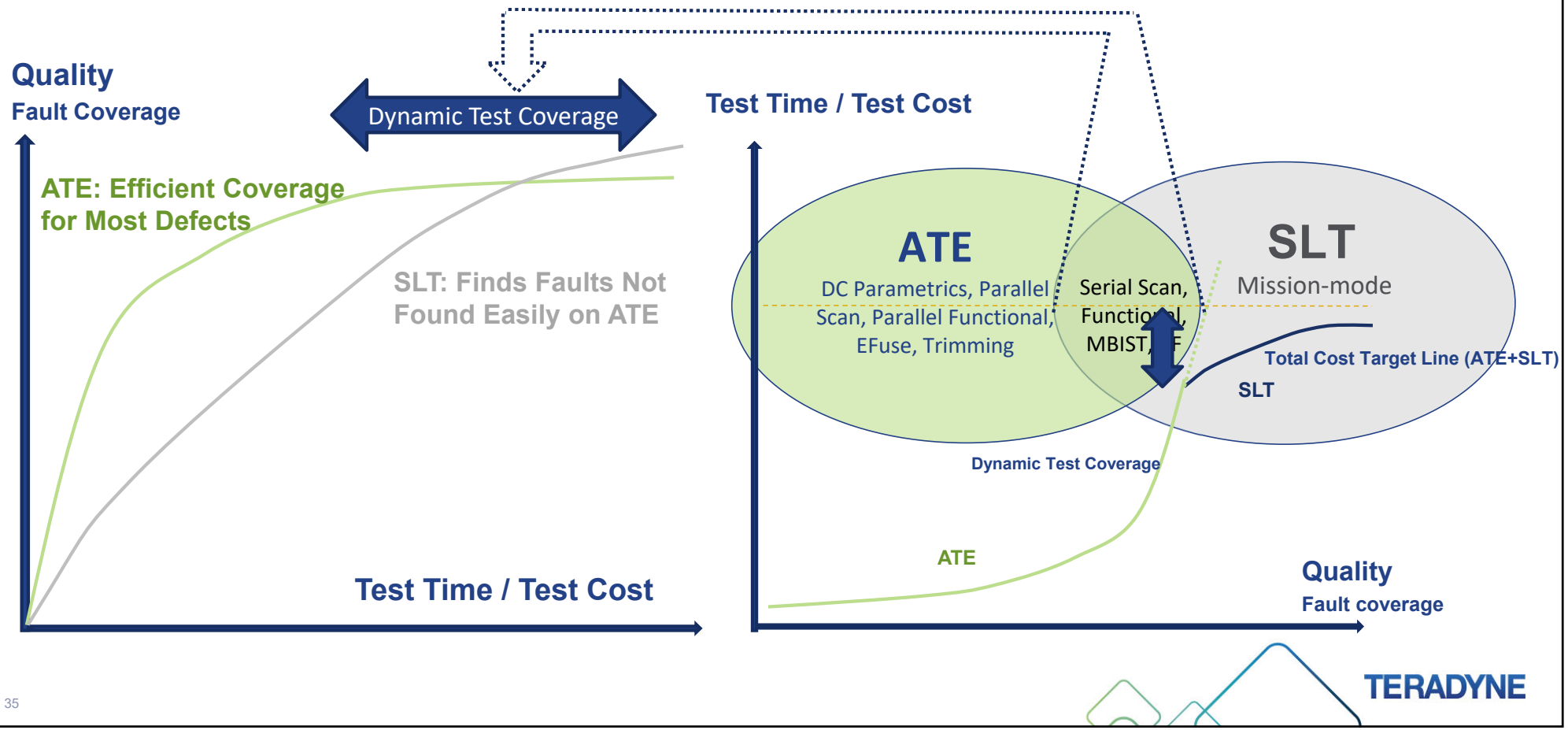
2.5D/3D Packages Test Challenges *

- **3D probing, 3D die stacks, 3D stack repair**
  - 3D die stacks metrology, testing, or AOI at pre-bond, mid-bond, post-bond, and final test.
  - Need a tool that models the cost and yields of wafer processing, stack assembly, testing, packaging, and logistics, to optimize the stack assembly and test flow.
  - Test access to the non-bottom dies is a key challenge with large arrays of fine-pitch micro-bumps 40-30 um).
  - **Need 3D-DFT** (i.e., DFT in addition to the conventional 2D DFT) to transport test stimuli up into the stack and test responses back down. Thus, need a stack-wide 3D-DFT test access architecture **in compliance with IEEE Std 1838-2019.**
  - The three major **EDA suppliers have started to provide support for IEEE 1838** insertion and usage.
    - Both INTEST (testing or re-testing the internal circuitry of the die) and EXTEST (testing inter-die interconnects).
  - Current-generation products include redundant interconnects for “self repair”.

* https://eps.ieee.org/images/files/HIR_2024/HIR_2024_ch17_Test_Technology.pdf, pages 75-79

TERADYNE

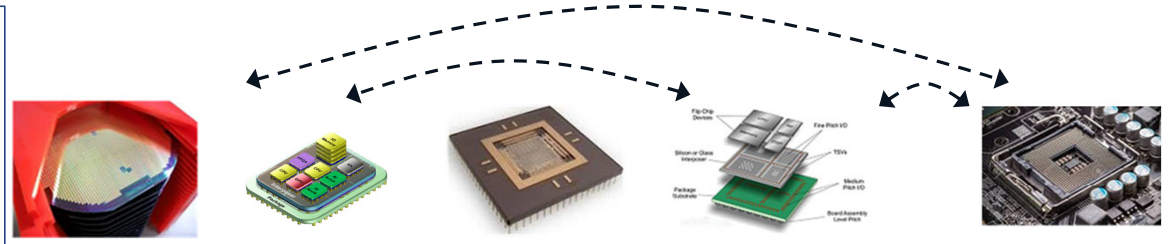
Dynamic Test Coverage: Optimizing Cost of Quality



"Shift Left" **AND** "Shift Right" to Optimize the Overall Cost of Quality

Balance Test Coverage Across the Manufacturing Flow for best mix of cost, quality, and yield

Minimize scrap cost *by reducing defect escapes during Wafer Sort*
Lower device CoT *by performing high-yield tests at the most cost-effective insertion*
Improve yield *by collecting high-volume test data that will drive manufacturing process improvements*

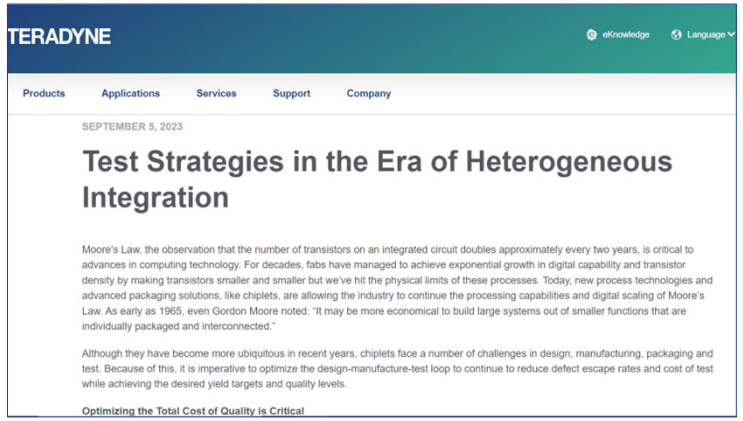


Minimizing defect escapes earlier reduces scrap

Cost Optimization Across Ecosystem

Lowest test time cost per second

Efficiently minimize defect escapes High Failure Rate Tests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Products Applications Services Support Company

SEPTEMBER 5, 2023

Test Strategies in the Era of Heterogeneous Integration

Moore's Law, the observation that the number of transistors on an integrated circuit doubles approximately every two years, is critical to advances in computing technology. For decades, fabs have managed to achieve exponential growth in digital capability and transistor density by making transistors smaller and smaller but we've hit the physical limits of these processes. Today, new process technologies and advanced packaging solutions, like chiplets, are allowing the industry to continue the processing capabilities and digital scaling of Moore's Law. As early as 1965, even Gordon Moore noted: "It may be more economical to build large systems out of smaller functions that are individually packaged and interconnected."

Although they have become more ubiquitous in recent years, chiplets face a number of challenges in design, manufacturing, packaging and test. Because of this, it is imperative to optimize the design-manufacture-test loop to continue to reduce defect escape rates and cost of test while achieving the desired yield targets and quality levels.

Optimizing the Total Cost of Quality is Critical

Economically Ensure Quality Low Failure Rate Tests

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Summary

- AI data center computing performance requirements has enabled heterogenous integration of chiplets in advanced packages (e.g., CoW[P]oS, CoWoP): GPUs + HBMs + I/Os + CPO, etc.

- CoW[P]oS assembly process complexity brings new opportunities and challenges in metrology and test:
  - Pre- and post-bonding metrology and automated optical inspection
  - New test insertions and challenges are emerging:
    - CoW module test
    - Singulated Die (SD) test
    - D2D and High Speed I/O testing
    - Mission mode test at WS, SD and CoW test insertions
    - Advanced Adaptive thermal control techniques for increased thermal requirements
    - Photonics-ready production ATE and SLT test cells
    - Flexible test flows to optimize overall cost of quality – “shift left” or “shift right

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Thanks!

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