# Load Boards: Challenges in Manufacturing for High-Performance Computing

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TestConX™

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R&D Altanova®

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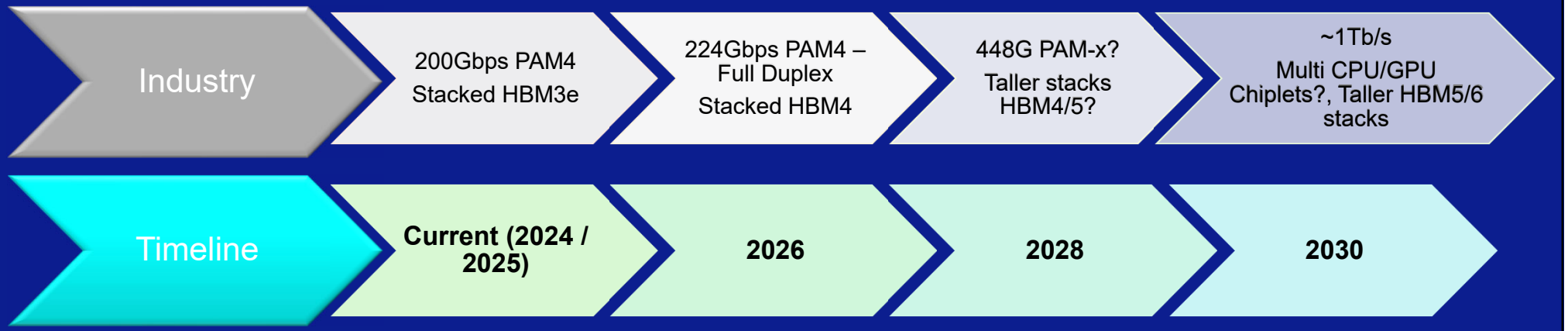
# For Discussion

- Market Drivers
  - The need for speed
  - And more power, too
  - Devices getting larger
- Manufacturing Infrastructure
- Back drilling
- Sequential Lamination
- HDI

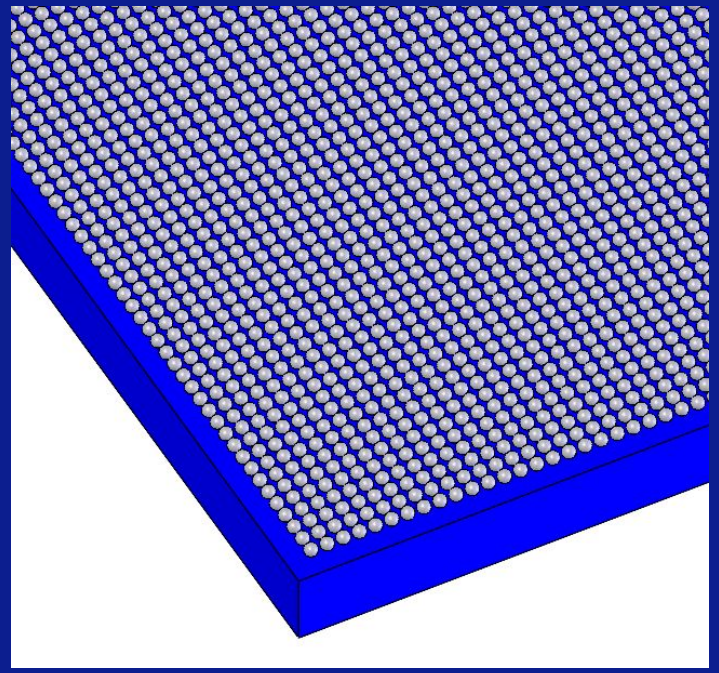
# HSIO PCB Roadmap Alignment

- Expected roadmap (constructed based on historical references)



# BGA's Are Getting Larger

- Today = 75mm x 75mm
- Near term roadmaps = 125mm x 125mm
- Long term (<3 years) 150mm x 150mm




HSIO Challenges
CHALLENGES
Impedance Control
Back-Drills
Drill Accuracy
Material Registration
Plating
Feature Control
Materials
Density
TECHNOLOGIES
Sintering
Premium Materials
Coaxial Vias
+/-2 % Impedance
CPO Integrated Sockets
HDI / Buildup
2 – 4 mil Stub Drill
Ultra Thick Boards
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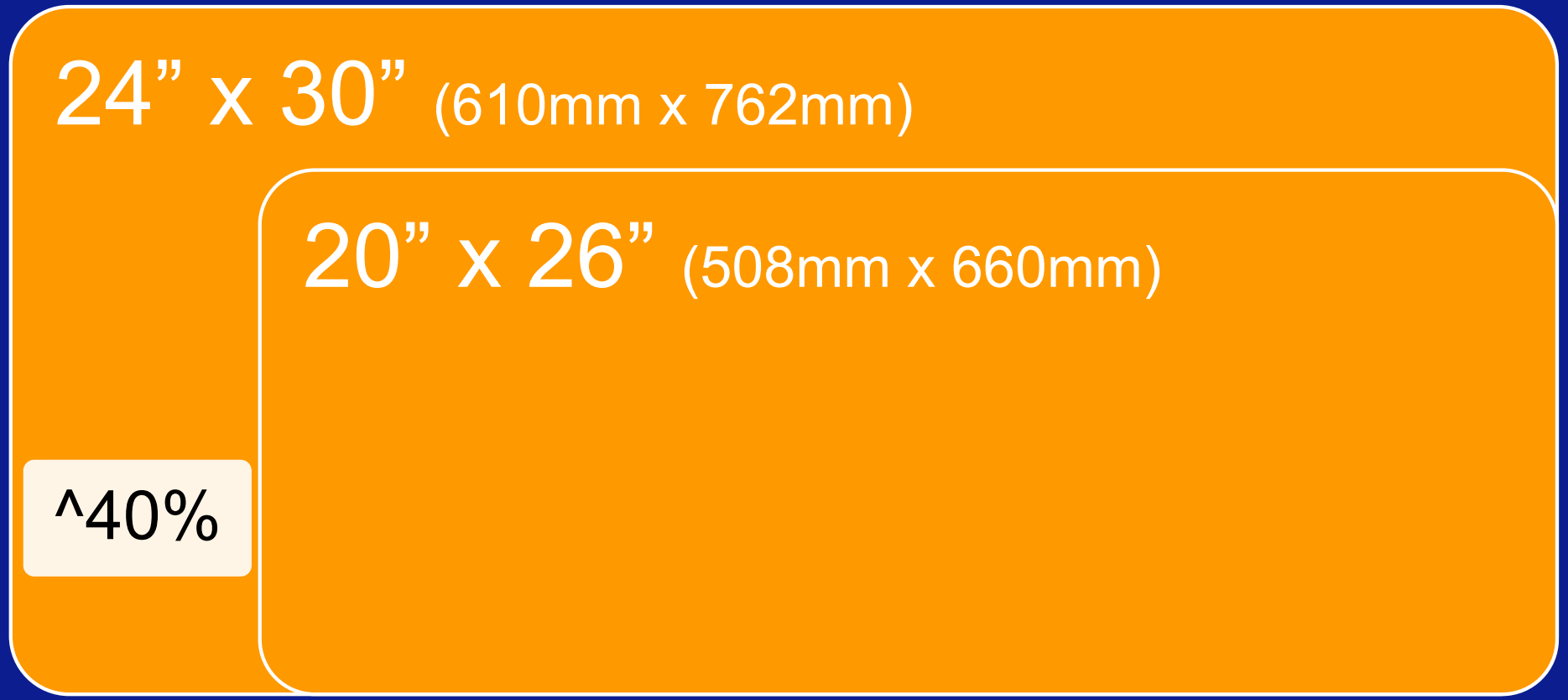
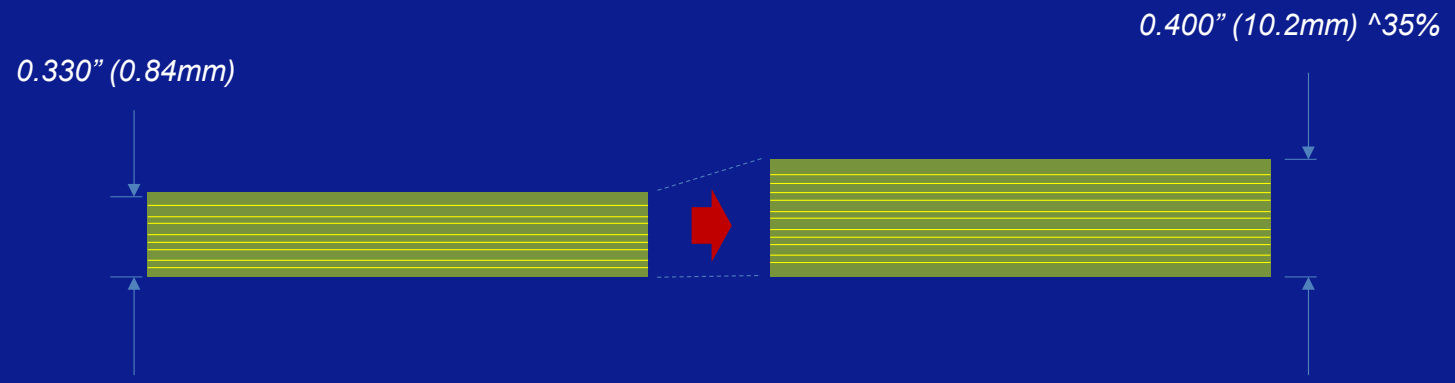
# PWB Manufacturing Panels Are Too



# Layer Counts Are Increasing

- As devices grow, layer counts increase, and panel thickness must also increase
- Layer counts have gone from ~50 layer to >70 and we'll see 100 layers in my lifetime



# PWB Infrastructure

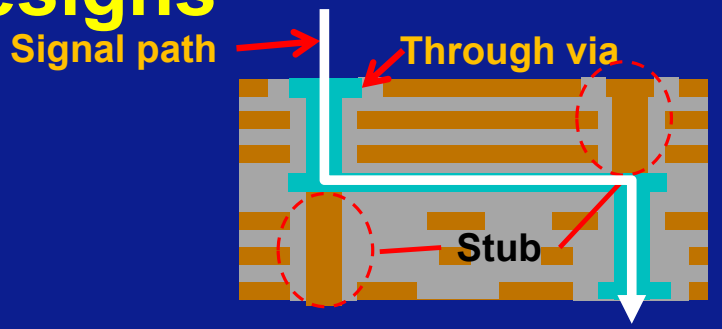
- Conveyorized equipment
  - Developer, Etcher
- Imaging equipment
  - Primary and secondary imaging
  - Solder mask exposure
  - LDI equipment has a limited focal range
- Drill machines & drill bits

# PWB Infrastructure

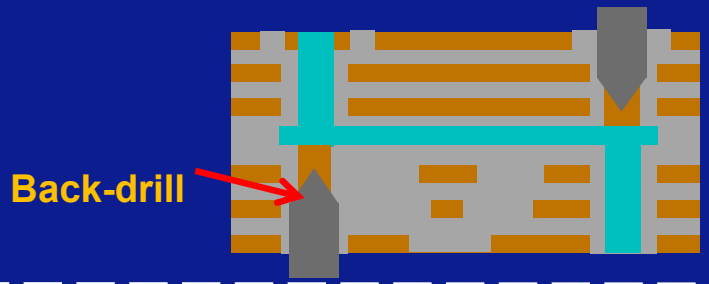
- Hole preparation and seed layer deposition
- High(er) aspect ratio plating
  - Copper, Nickel, Gold

# Back-Drill in HS Designs

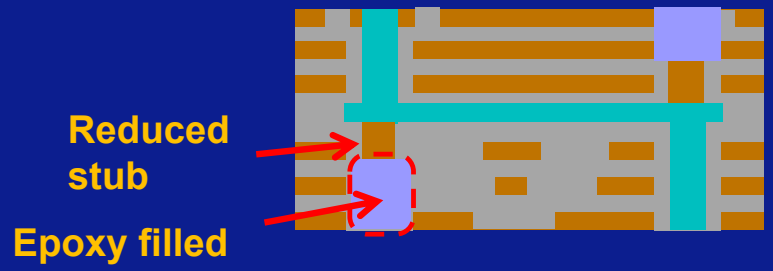
- Signal path has stubs → Causes reflections due to impedance mismatch




- Vias are back-drilled → reduced stub

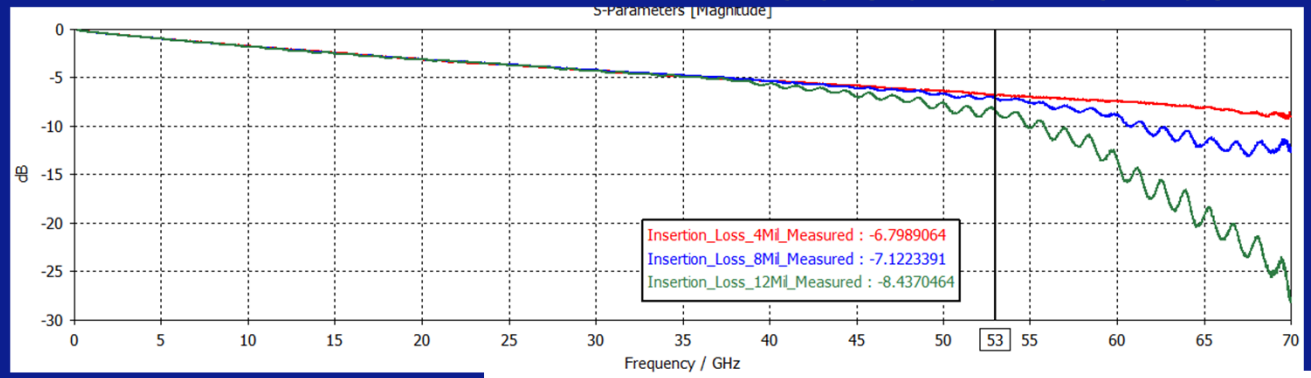



- Backdrill hole can be filled with non-conductive epoxy

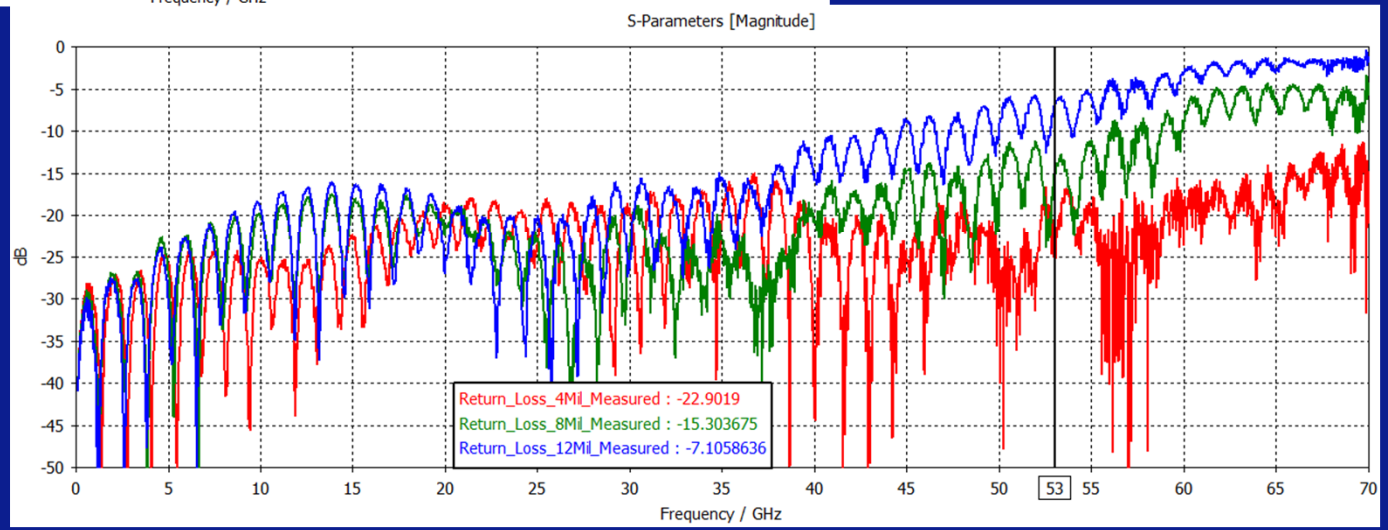


# Measurements

## Insertion Loss

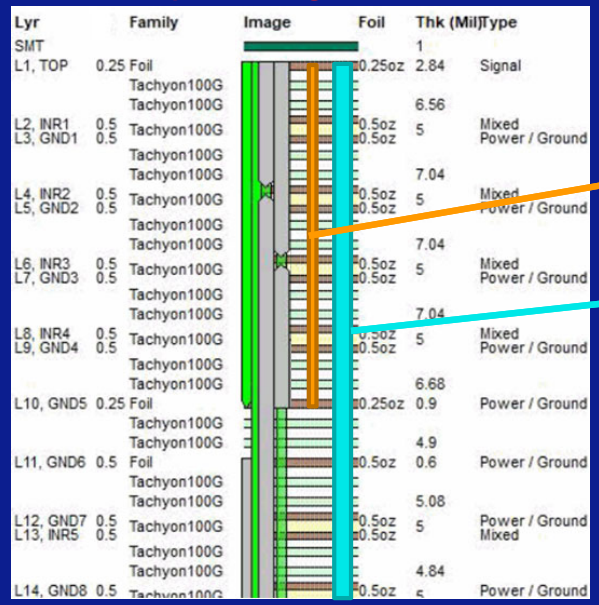


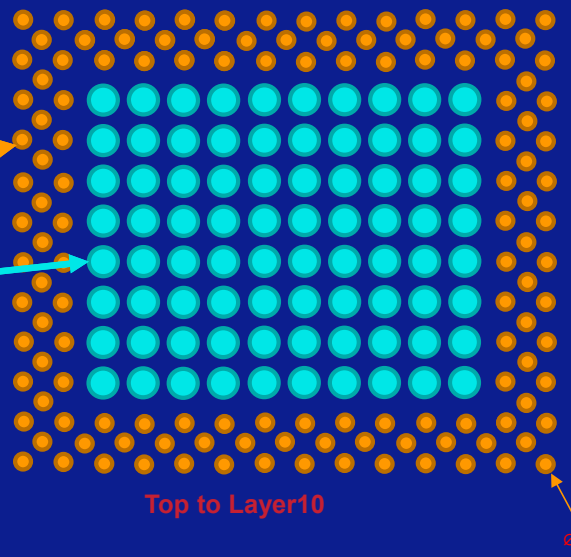

## Return Loss

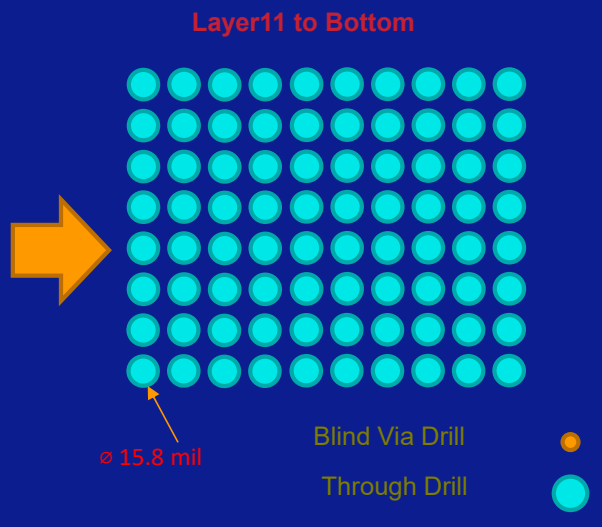


# An Alternate Strategy – Dual Lamination Stack

Example Stacking!




- ✓ Critical Signal of 5.9 or Smaller drills route on Top Book providing Good SI
  - ✓ Aspect ratio is greatly improved as finer drills are segregated on upper lamination only!
- ✓ All 2Oz Cu layers on bottom book with GND/PWR via uses bigger drills for better current capacity
- ✓ Upper book can host 0.5Oz power layers of certain critical supplies
- ✓ Improved power delivery to DUT core supplies

# But Tom, What About HDI?

- Not typically employed in ATE board manufacturing
- Involves advanced techniques and equipment
- Sequential lamination techniques
  - adding layers one at a time - $$ & lead time

# But Tom, What About HDI?

- HDI employs the use of microvia's, <= 150u diameter
- Material selection is challenging
  - those made to withstand the multiple lamination cycles are not the best from a signal performance standpoint
- High-Density Layout
  - often involving micro-vias, fine-pitch components, and smaller trace widths.

# Why not HDI?

- Loopbacks used on ATE boards will require similar number of layers, even with Micro vias and HDI design, not relieving much space around the DUT
- As the HDI will not use pitch transformation, the expected trace-widths/geometry will remain similar, thus not much benefit in layer reduction for high-speed signals
- As described earlier, HDI requires significantly more lead time and cost

# Our discussion today

- Market drivers
- Device size and the need for speed
- HSIO challenges & technologies to solve them
- PWB infrastructure
- Alternative PWB constructions
  - Thru-hole (w/ back drill), sequential lamination, HDI

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