HPC Test Challenges in the Era of Chiplet

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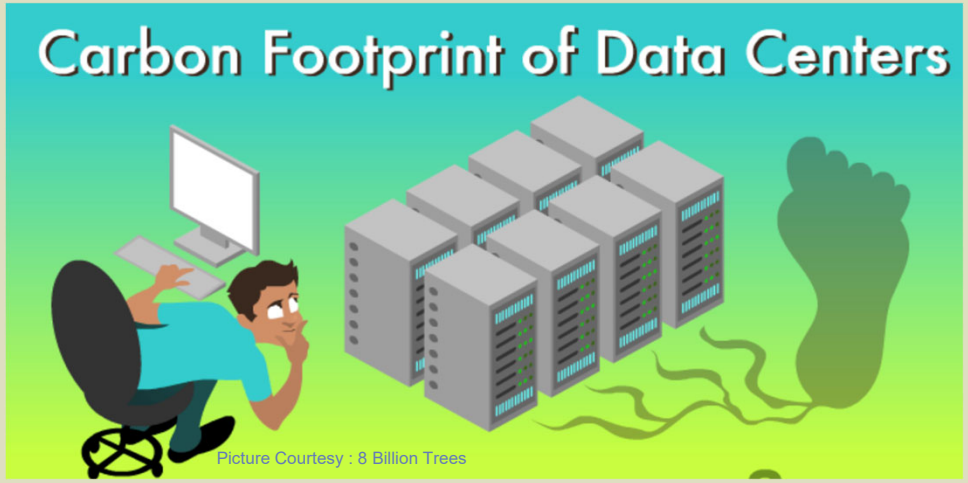
Agenda

- Trends in SOC Product Development
- Significance of KGD from Chiplet Perspective
- KGD Monitoring and Traceability in Heterogenous ICs
- Security concerns in era of Chiplet
- System Level Test – Key Differentiation
- Summary

Trends in SOC Product Development

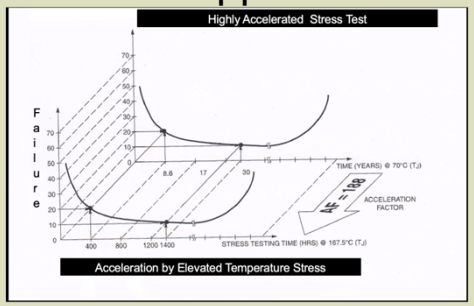
- Data centre offers massive computing resources, typically in the form of an elastic cloud platform
- Carbon Footprint
  - Electricity Consumption
  - Water Consumption
  - Lifetime of the Equipment
- Needs of Diverse Domain Specific Architectures
  - Machine Learning, Deep Learning, Block Chain and NLP
  - Dedicated Memory
  - More / Scalable ALU
  - Host of Interfaces, etc.
- Chiplets
  - Reduce Product Development time
  - Integrating Pre-Developed Die (KGD)
  - Different Process Node in the Same Package
  - Substrate a key element in System Performance



Data centres are responsible for 2% of overall U.S. greenhouse gas emissions

Trends in SOC Product Development

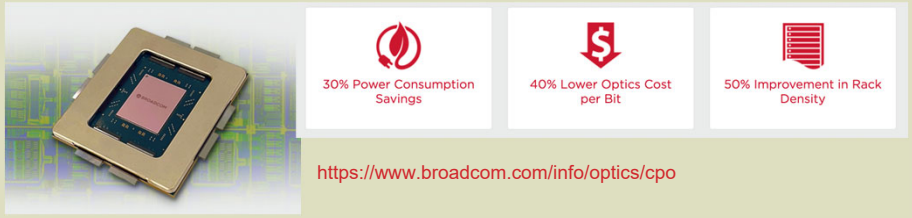
- Adoption of smaller process nodes in Mission Critical applications like Automotive
  - Reliability
  - TDP v/s Operating Temp



- Connected Vehicles
  - Latency (100 µs for 6G)

- Hi-speed Interconnect standards (PCIE, CXL …)

- Co-Packaged Optics



Trends in SOC Product Development

Key Essence	
Product Development	**Importance for Test**
• Carbon Footprint - Electricity Consumption - Water Consumption - Lifetime of the Equipment	• Every mW of power optimization saves M$ - Substrate Design optimized for PDN - Thermal Management - Silicon Monitoring
• Reduce Product Development time - Chiplets - Integrating Pre-Developed Die (KGD) - Different Process Node in the Same Package - Substrate influence in System Performance	- Chiplets designed considering “Off Die DFT” - KGD could be from many different vendors - Test / Validation of Substrate Performance - Traceability and Security

Significance of KGD from Chiplet Perspective

KGD in Monolithic

Assembly defects and functionality at speed are tested at package level.

Functional requirements of the packaged parts do not change drastically from the die level.

DPPM target is with in the product company control.

KGD in Heterogenous

Assembly defects after package of a particular KGD many not be 100% directly detectable – Additional test.

Individual Die not necessarily define the full functionality of the Packaged IC .. could be only partial.

Third party Die could be integrated .. such as HBM.

Individual Die DPPM comes into picture .. The over all package level DPPM becomes an addition of individual KGD DPPM

Significance of KGD from Chiplet Perspective

Die to die interconnect within the package only going to be in millimeters

- This will help to optimize the drive strength which will help to optimize the power consumption
- Testing them as an individual die poses a challenge.

Loop back test might be very much applicable for Hi-speed Interface

Reality of SI Simulation on Substrate interconnect actual manufactured substrate cannot be assumed to match

- Tight manufacturing tolerance of line width, space etc. is critical.
- Net list Open/Short test data of substrate + critical hi-speed substrate trace testing on sampling would help to improve packed IC yield. Possibility of critical signal trace coupon can be explored.

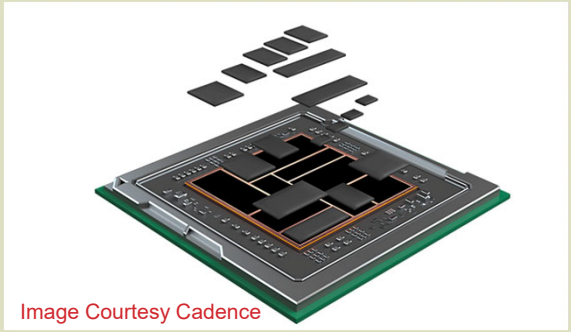


Image Courtesy Cadence

With Chiplet PPA is not just for Chip Design – now to Substrate Level

Thermal Consideration – Influence of Chiplet just few mm apart

Substrate material – Laminate / Silicon-Passive / Silicon-Active

Power Plane impedance inside the Package

Significance of KGD from Chiplet Perspective

ATE Test and COT for Chiplet – Bumped Die

Every type of Chiplet considered for Heterogenous integration needs to tested

C4 bumped pitch (say 140 µm) needs advanced probe cards such as Vertical Probe

While Multi Die testing on a Single touch down key for COT

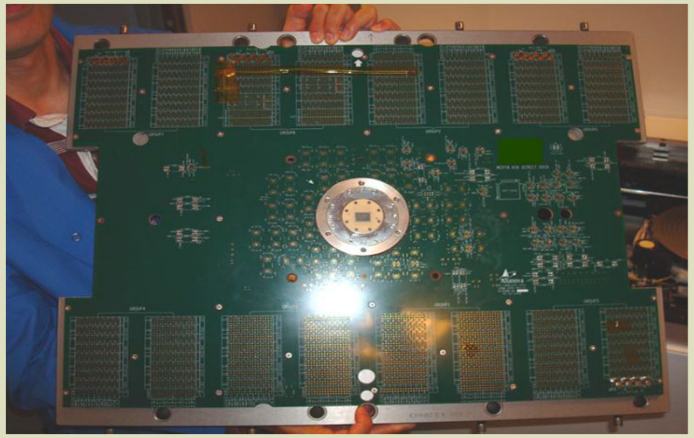


Image Courtesy Advantest

Stack up will exceed 40 Layers .. Achieving a manufacturable Aspect ratio is a challenge as the PCB thickness in the range of 4 mm app.

HW fab complexity increases for Multi Site and hence the PCB Fab yield and reliability – A compromised balance of FAB Yield and NRE cost needs to be arrived at.

HW price including MLC and Vertical Probe Head would exceed $100K for each type of Chiplet being Integrated

Significance of KGD from Chiplet Perspective

ATE Test and COT for IC using Chiplet – Heterogenous Package Test

Parallel testing of packaged part limitation could come from Power supply as well (apart from ATE digital channels)

Hi-speed interface lines length budget, tolerance across all test site.

ATE instrument specific rules – Violation could result in inaccurate measurements.

ATE HW Diagnostics and Calibration offset for onboard components

PI and SI simulations are crucial for avoiding expensive HW design re-spin.

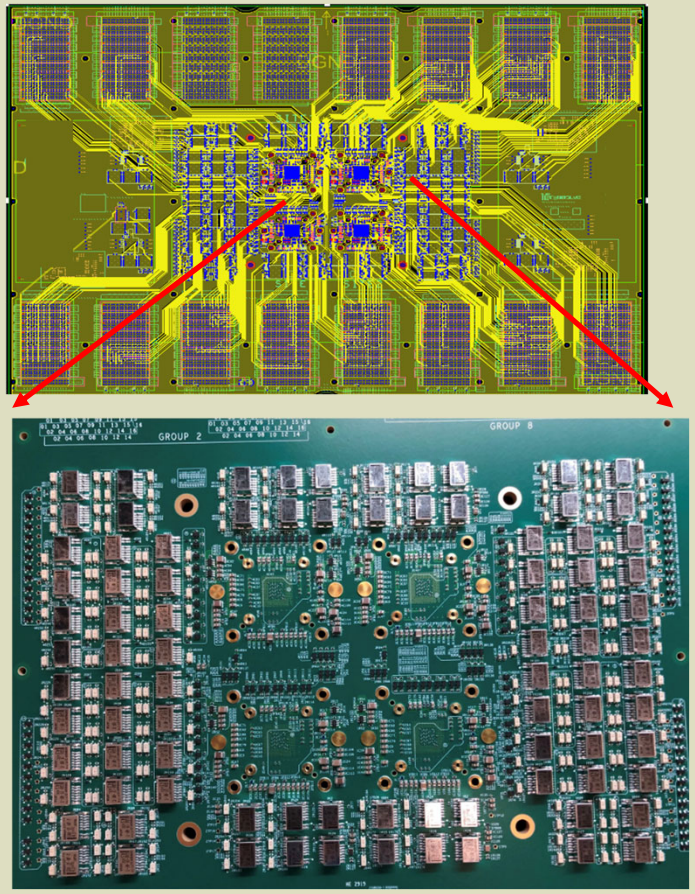
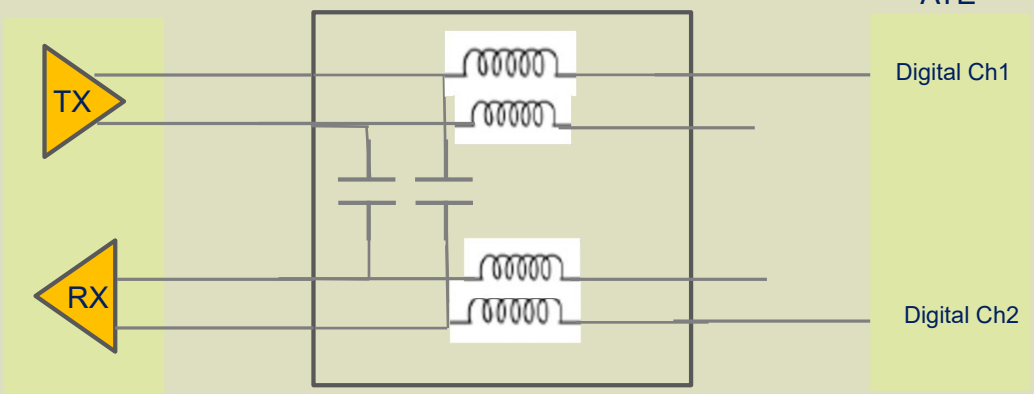


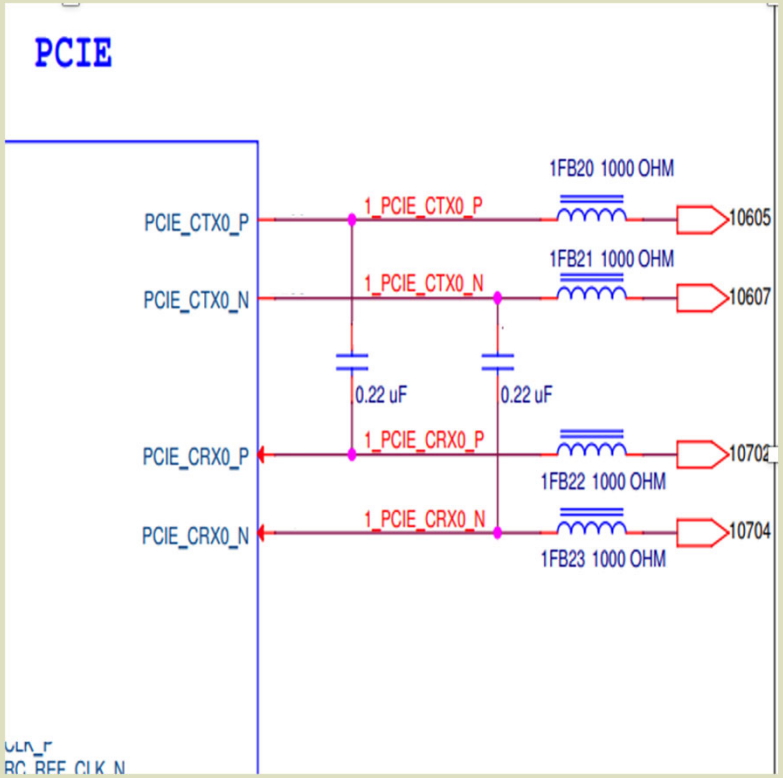
Image Courtesy Tessolve

Significance of KGD from Chiplet Perspective

Chiplet I/O Drive strength / Loop back test .



- Number of Layers : 44
- Power Layers : 7
- Signal Layers : 13
- Material type : MEG6
- Target Impedance : 50 ohm
- Board size : 16.9” x 22.9”
- Board Thickness : 5.10 mm (200.90 mils)



MEMS based loopback

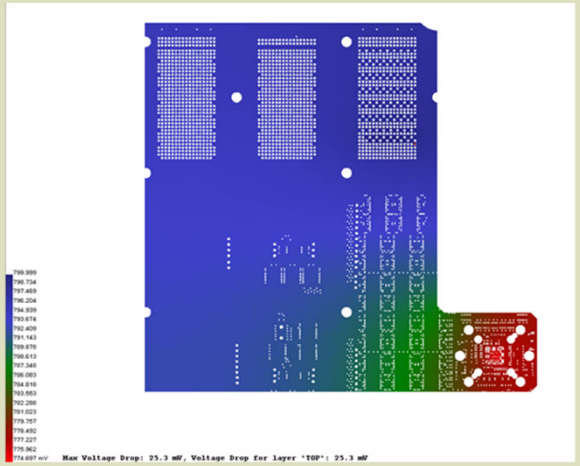
Image Courtesy Tessolve

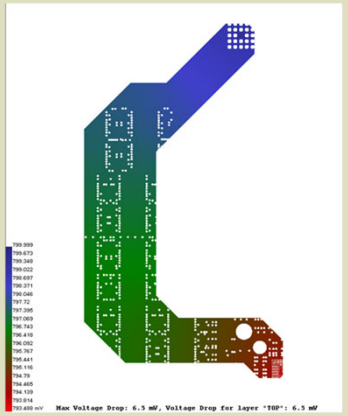
PI and SI simulations : Avoiding HW design re-spin

DC drop analysis

Inputs considered for PI analysis:

- Stack up
- Layout Database
- Schematic
- Power net list
- Source Voltage, and Load current values





Note : In the DC drop analysis, the DC characteristics of the power plane shape are analysed by simulating for the amount of DC voltage drop from source to the load caused due to the DC resistance of the power plane shape.

For Example : One of the power supply rail (VDD core supply) 0.8 V (15 A current requirement). The maximum voltage drop observed is **25.3 mV.** Similarly **6.5 mV** on DDR core 0.8 V supply.

Plane Impedance: Need to be optimized for the critical switching Freq .. Low ESR cap banks selections

PI and SI simulations : Avoiding HW design re-spin

MIPI Interface

Inputs considered for SI analysis:

- Layout files
- Stack up
- IBIS models
- Schematic and critical signals list
- Max. Transfer Rate : 2.5 Gbps

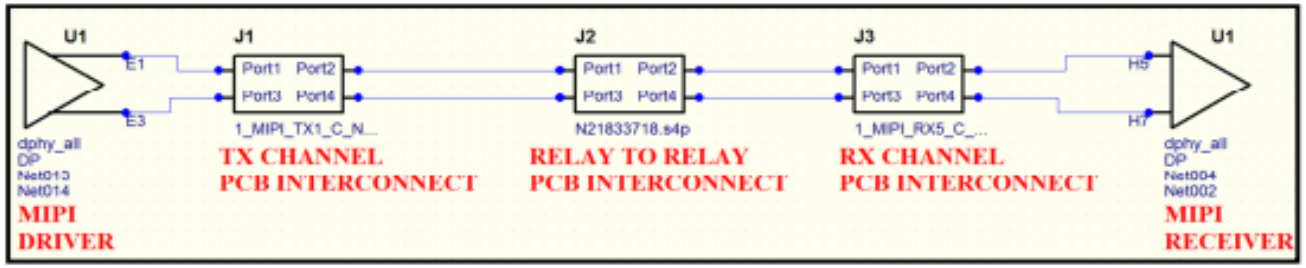
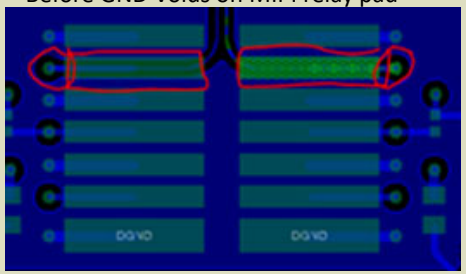
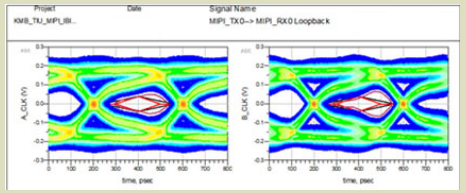


Image Courtesy Tessolve

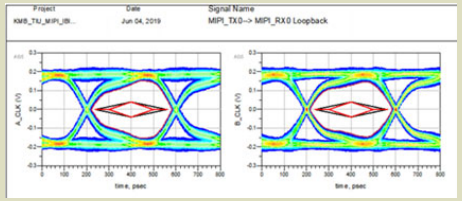
Topology of MIPI net with U1 as load and U1 as the driver

Before GND Voids on MIPI relay pad





After GND Voids on MIPI relay pad

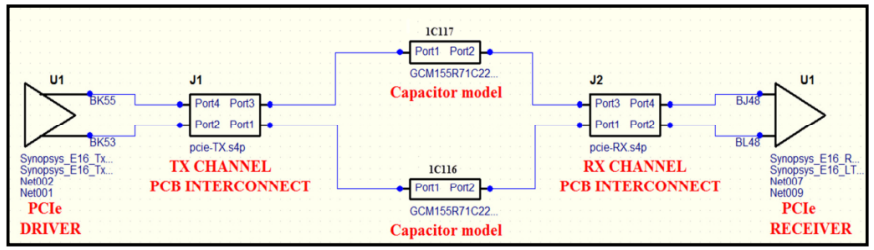


PI and SI simulations : Avoiding HW design re-spin

PCIe critical ATE routing guidelines followed:

1. Max loopback length to be matched across sites.(PCIE_TX*_P/N,PCIE_RX*_P/N)
2. Voiding of ground plane directly beneath the Loop back capacitor pads.
3. 85 Ω differential routing.
4. Void size must be at least same dimension as the pad's size.

- **For PCIe 4.0 interface max transfer rate is 16 Gbps**
- **Topology as shown below:**



Topology of PCIe net with U1 as load and U1 as the driver

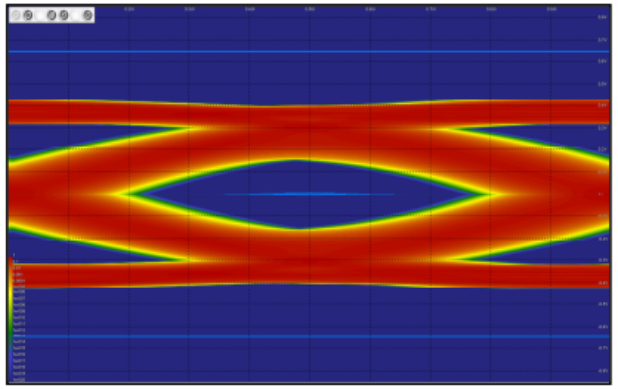
Bit rate : 16 Gbps

Bit interval (Unit interval) : 0.0625 ns

Bit Pattern : PRBS order 11

Total # of bits simulated : 1 million

From the eye diagram we can observe that eye at the receiver meets the eye mask specifications



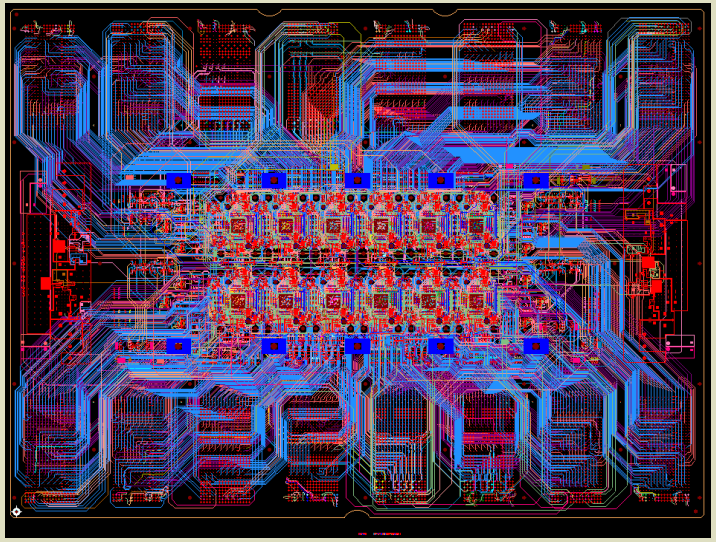
Eye diagram for PCIe net with U1 as load and U1 as the driver

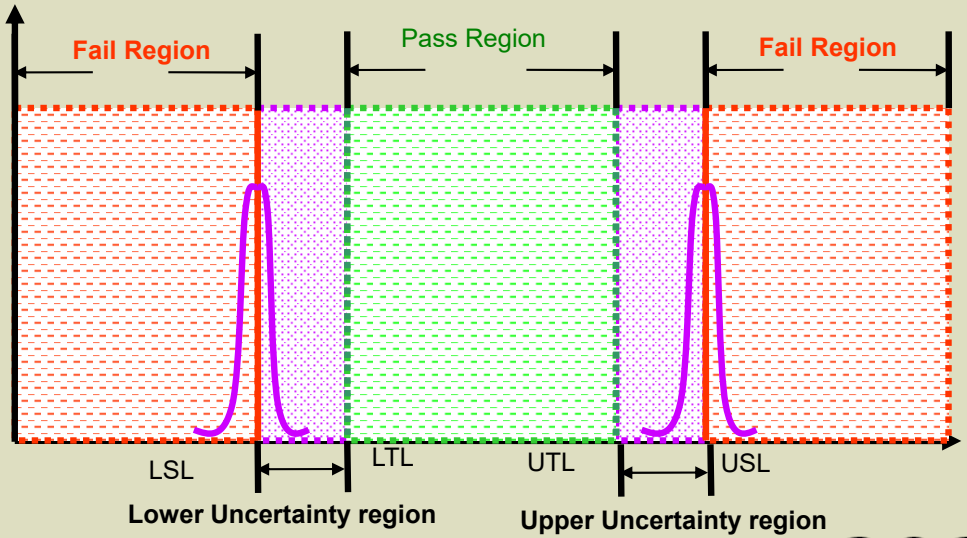
Eye Measurements		
Eye Height @0.5 UI (V)	Eye Width (UI)	Eye Width (ps)
0.304	0.594	43.37

Correlation and Guard-banding

Bench Measurement to ATE Measurement
Board to Board Correlation
Site to Site Correlation
ATE to ATE Correlation as part of Acceptance
Same ATE to Same ATE (Test Time Reduction)

Upper Test Limit = Upper Specification Limit - 3σ
Lower Test Limit = Lower Specification Limit + 3σ





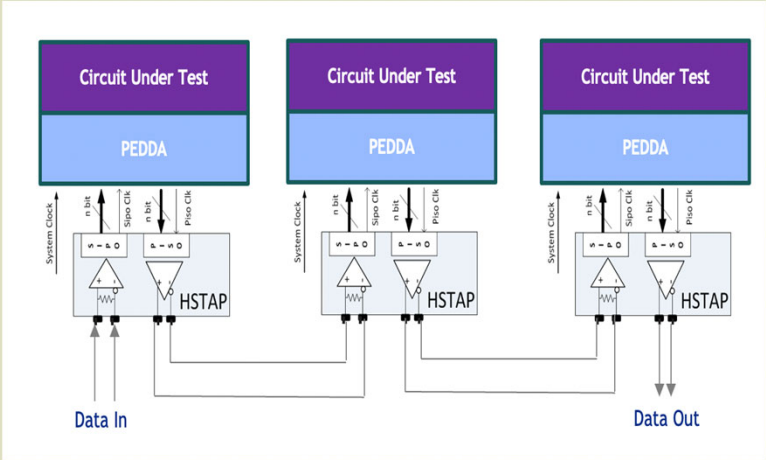
DFT Considerations for Chiplet

Package level failure that points to a specific Chiplet.

DFT architecture need to be implemented as sub-block approach.

Scan vectors could be still run by isolating the faulty sub-block/chiplet and able to verify the remaining integration.

SSN/1149.10 based DFT architecture need to be explored.



Has the industry evolved to openly give DFT vectors of the chiplet to external companies?

- **LBIST and MBIST** enablement and result registry access.

Would the robust good old boundary scan IEEE-1149.1 be a fallback solution?

- Chiplet to chiplet interconnect on the substrate can be thought of multiple ICs on the PCB
- Ride on HSTAP / JTAG interface if available.

KGD Monitoring

What is happening inside the Chip? – Monitor (Design , Volume Test and In-Field)

In-Chip-Monitor – Instantaneous Environmental Monitor.

- Process Monitor.
- Power Rail Voltage Monitor.
- Temperature Monitor.

Dynamic Voltage and Frequency Scaling (DVFS)

Process Monitor

- Decision making before classify the Die a KGD
- Behavioral understanding of Wafer Level and Lot Level

On Die / Active Silicon Interposer

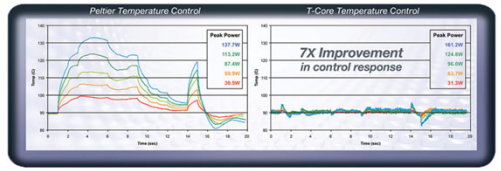
Power Rail Voltage Monitor

- Compute Performance optimization by monitoring Voltage
- Alarm / Interrupt Signal activation to other subsystem and bring the device to safe state
- Could be considered as a part of POST

Temperature Monitor

- Compute Performance optimization by monitoring Temperature
- Alarm / Interrupt Signal activation to other subsystem and bring the device to safe state
- Could be considered as a part of POST and for Mission Mode Test.

KGD Monitoring



Picture courtesy Cohu, Inc.

Thermal Management - Requirements

Active Thermal Control (ATC) for products requiring near 1 KW power dissipation

High speed, 1 ms closed-loop ATC for applications in Engineering Development, Test, Burn-In and System-Level Test

Control loop to interface with Device Diode Temperature sensor

Architecture to support multiple sites with multiple RTD sensors per site

Fast temperature ramp up/ Ramp Down in the range of 100 °C/s

Closed-loop Automatic Flow Control (AFC) for liquid-cooled, air-cooled or phase-change (refrigerant-cooled) thermal heads

Support for tri-temp testing with single insertion during Char routines / System Level Test

Multi-site Handler that has a capability to interface with ATC for volume test

Picture courtesy Cohu, Inc.

KGD Monitoring

In-Chip-Monitor – Structural Monitor

- Semiconductor do have ageing as inherent property as it is influenced by NBTI (Negative Bias Temperature Instability), HCI (Hot Carrier Injection) and TDDB (Time dependent dielectric breakdown).
- Aging affecting Propagation Delay

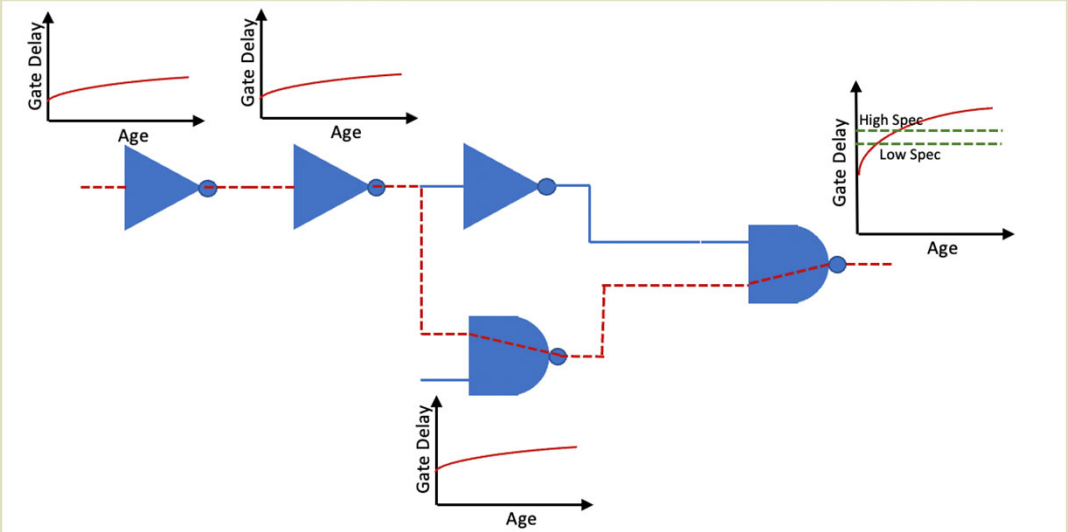


Figure 1: Foundry provides aging model of the transistors to do timing analysis of the circuit. As the transistor ages over period, it increase the gate delay. This could violate the timing spec that is required for the proper function of the circuit during its expected operating lifetime.

KGD Monitoring

In-Chip-Monitor – Structural Monitor

↓

Path Margin Monitoring

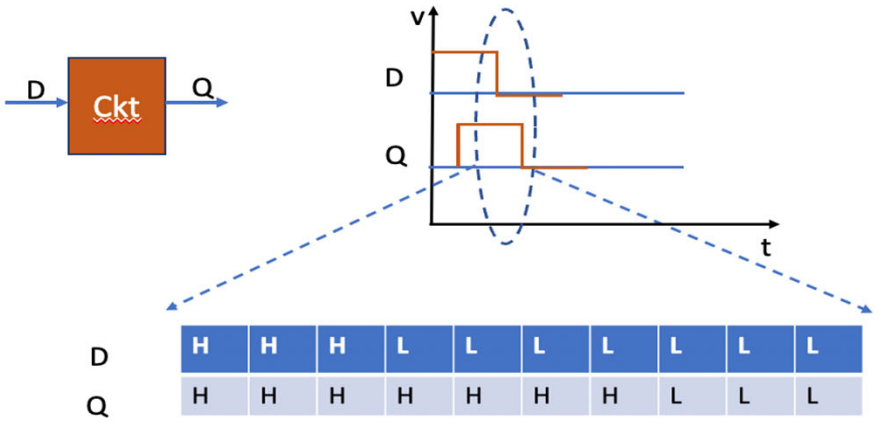
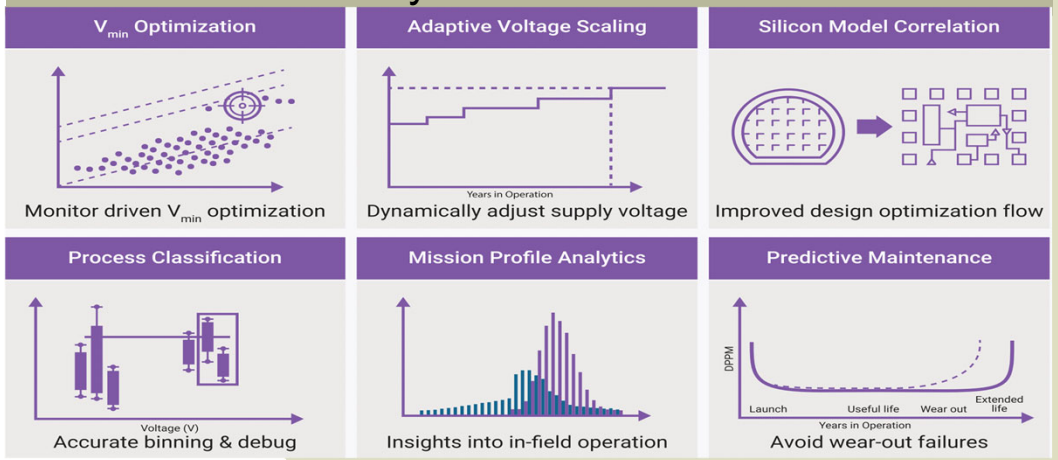


Figure 2 : Response of a digital path in a circuit constituting a Delay and its time domain response. The dotted line captures the state of the input D and out put Q, which are sampled faster.
In this illustration 10 logic states are collected from D and Q to form a Signature

SLM Use Case : EDA Vendors now provide Silicon Life Management Tool (SLM) for end-to-end Visibility.. Right from Design, Product Ramp, Volume Production and finally In-Field

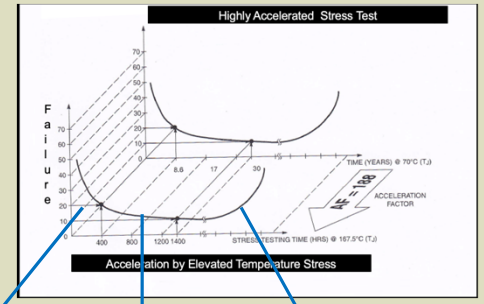


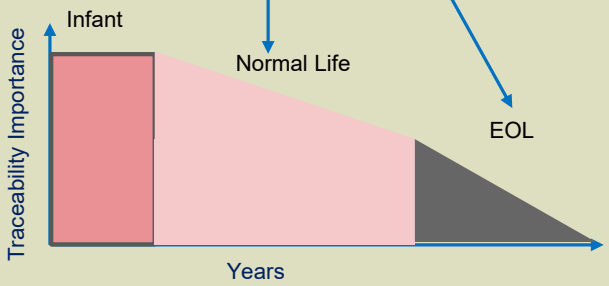
Courtesy : Synopsys https://www.synopsys.com/solutions/silicon-lifecycle-management.html

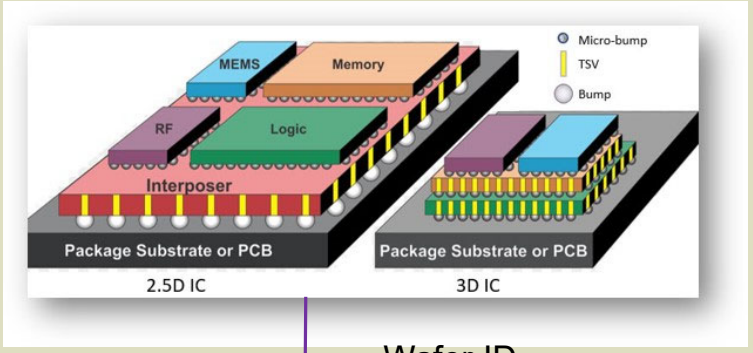
Seems no SLM Standards established yet !!

Traceability of KGD

What happens when the Heterogenous packaged IC Fails in the Field?







- Wafer ID
- Die ID
- Assembly Data
- Test Data

Traceability of Chiplet to Individual Die level info form the Packaged IC on a established protocol Interface for quicker retrieval .. Thus, enabling Datal Analytics need to considered of Importance

OSAT provide Unit Level Traceability (ULT) by 2d Barcode on a Packed Device. Commercial Device may need about 5 years of traceability but for Automotive it would extend to 15 Years

Identifying root cause sooner would be important for Automotive Grade IC (especially for ADAS Levels 4 and 5) and probably for high end HPC ICs

SEMI Traceability Standards committee SEMI T23

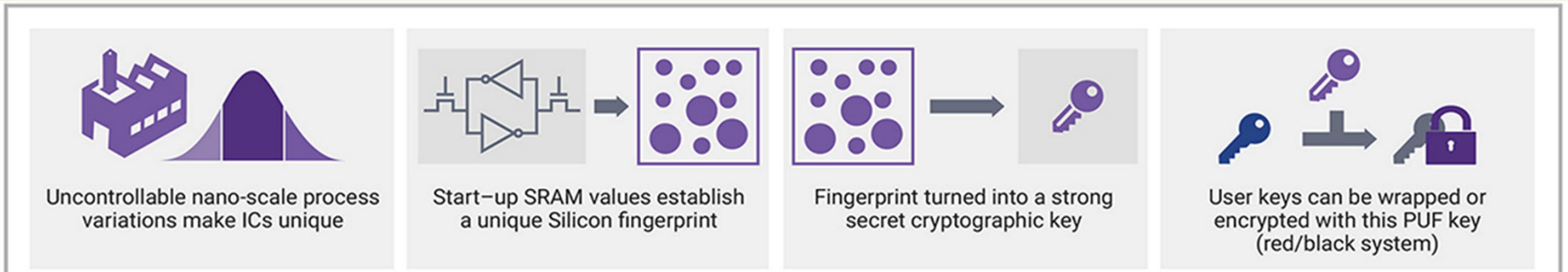
Security for the Chiplets Based Integration

Integrating multiple chiplets into a heterogeneous package opens the door for security breaches and potential risks for cyber attack

Companies that has own chiplets, which minimizes supply chain threats of clone. But companies assembling and integrating commercially developed chiplets will have a much tougher time.

SRAM PUF (Physical Unclonable Functions)

The behaviour of an SRAM cell depends on the difference of the threshold voltages of its transistors. Even the smallest differences will be amplified and push the SRAM cell into one of two stable states. Its PUF behaviour is therefore much more stable than the underlying threshold voltages, making it the most straightforward and most stable way to use transistor threshold voltages to build an identifier.

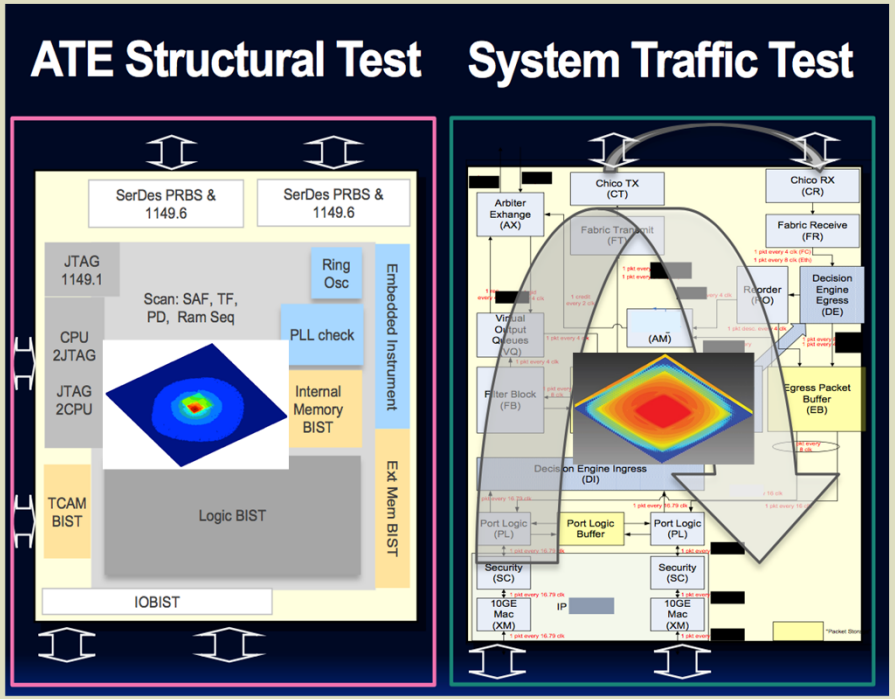


Source : https://www.synopsys.com/designware-ip/technical-bulletin/sram-puf-secure-silicon-fingerprint.html

System Level Test – Key Differentiation

System-level test is the ability to test a chip, or multiple chips in a package, in the context of how it ultimately will be used.

*Source: Semiconductor Engineering 9 Oct 2017



In ATE based test, the focus is more on getting the various blocks of the IC in for a pass and fail

HPC, Automotive IC needs to be tested along with the other supportive ICs such as PMIC, External Memory, Display, running on a customer-specific firmware. It is important to mention that the external support ICs mentioned may not be from the same manufacturer.

Testing for customer-specific Use Case is becoming a key need for the devices that are used for mission-critical applications such as Automotive and Data Centers (Silent Data Corruption) along with the need for DPPM quality levels… Drives SLT requirement

System Level Test – Key Differentiation

System Level Test - Facts

Compared to ATE test time, usually in seconds .. SLT test time could run to several minutes

Number of parallel device tested in ATE is limited by ATE available resource and hence usually 4 to 8 device tested in parallel for high pin count device

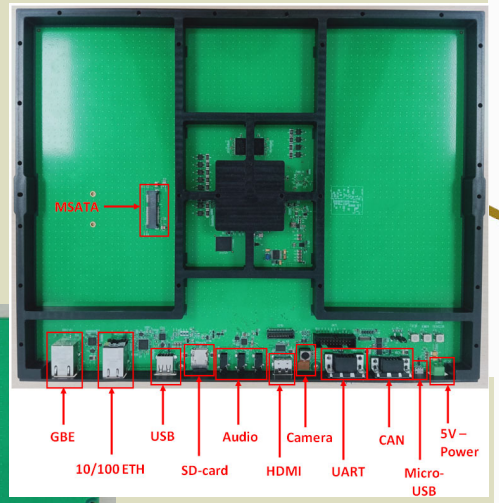
SLT's massive parallel test brings the opportunity to move SCAN / BIST from ATE to SLT

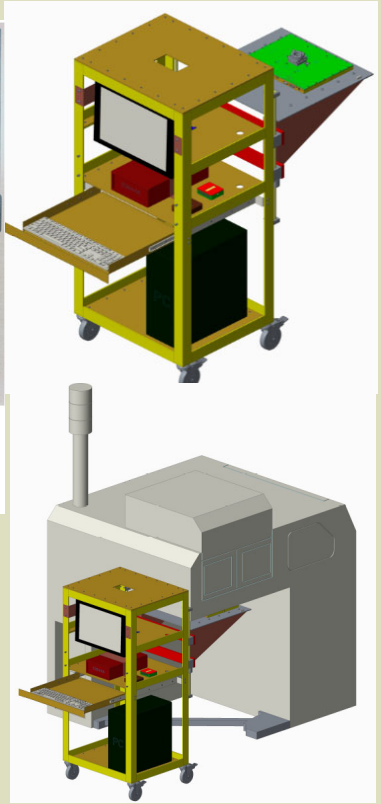
SLT is performed in massive parallelism and hence a specialized SLT Handler Equipment needed .. Additional CapEx

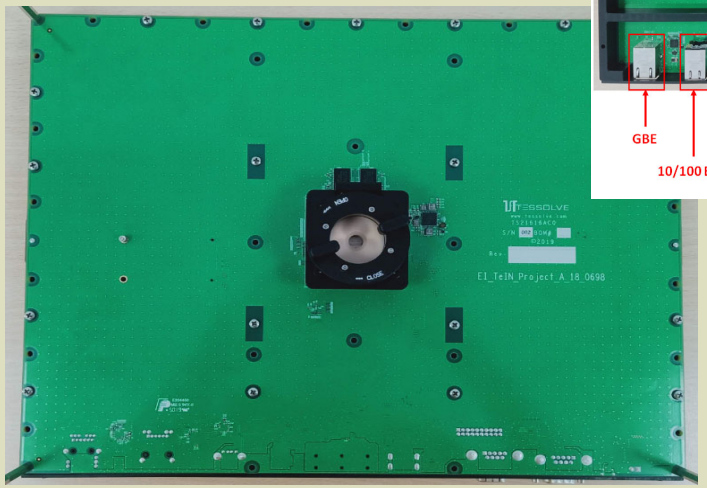
SLT as a strategy for NPI Safe launch

A typical Test Engineer with ATE experience may not have the knowledge of writing Test Use Case on the Operating Systems such as Linux, Android etc. and hence a collaborative approach of Embedded expert along with experience of volume Test is required to enable a SLT solution to production.

Example Single Site SLT Quad Arm®Cortex®-A9 core Processor



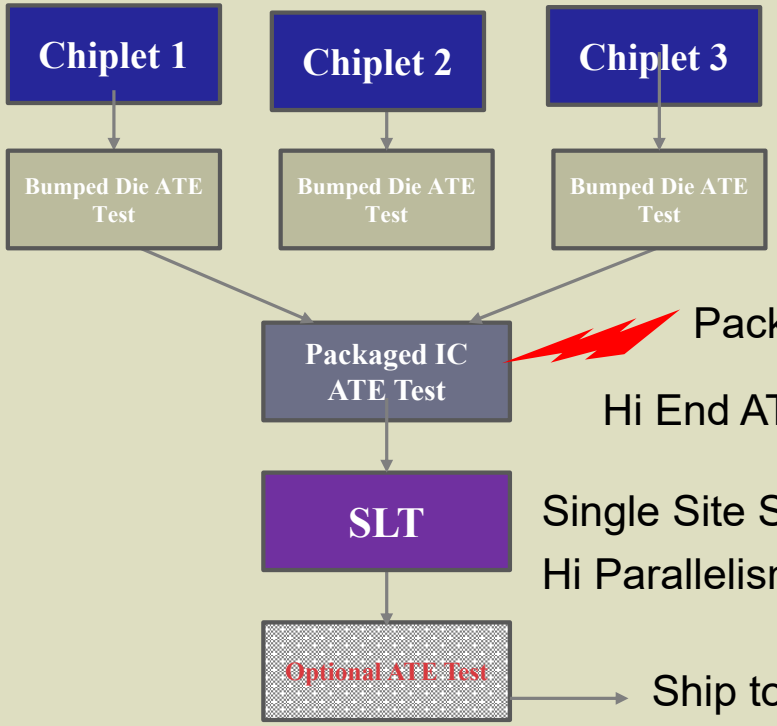




Picture Courtesy: Tessolve Semiconductor

Single Site SLT to run small volume for NPI safe launch

Test Flow for Chiplet Based IC with SLT



Low Cost ATE - Parallelism more than 8

Package Substrate performance

Hi End ATE – Parallelism 4 to 8

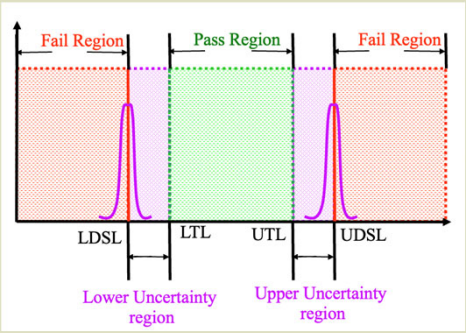
Single Site SLT for NPI - Use existing Handler

Hi Parallelism SLT for Volume – SLT Handler

Ship to customer

Summary

Chiplet I/O optimized for required drive strength for few mm D2D interconnect … Loop back test might very much applicable for testing Hi-speed Interface



Chiplet being from different vendor need "**Off Die DFT**" considerations.

KGD Test Limit Guard band keeping in account of Heterogeneous IC Package

The over all package level DPPM in the Heterogeneous IC Package

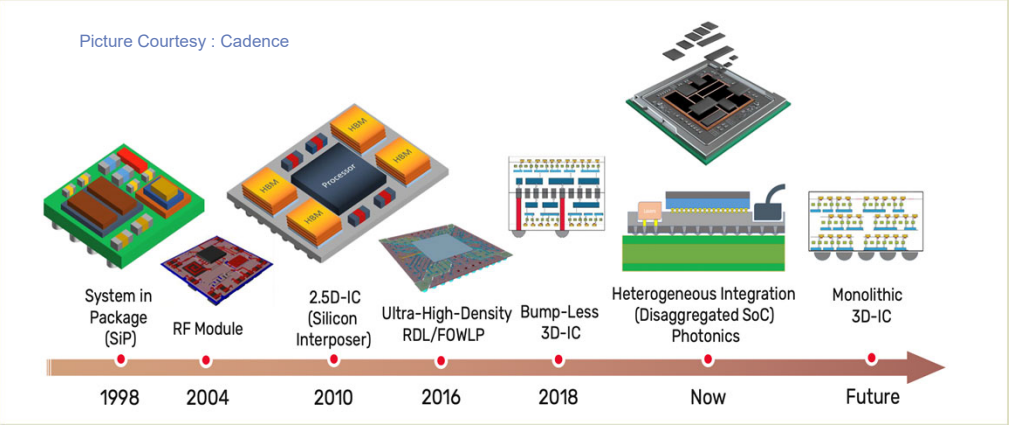
Embedded Expertise step into Test (Semi Test and Embedded Software Expertise would be a Boon)

System Level Test – Running actual Use Case Test

In Chip Monitoring and Die level traceability

Known Good Chiplet -- KGC

Known Good Substrate -- KGS



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