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# **Al for Test:** The New Frontier

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March 3, 2025





TestConX Workshop

www.testconx.org

March 2-5, 2025

AGENDA

#### Outline

- 01. Industry trends
- 02. <u>Technical challenges</u>
- 03. <u>Innovation opportunities, with one example</u>
- 04. <u>Remaining challenges, and the journey ahead</u>

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TREND

#### Important Shifts in the Industry



TREND

#### (Incomplete List of) Hot Test Topics

## Quality vs. Cost

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As the semiconductor industry continues to evolve, the importance of **highquality testing** will only increase. Advanced and flexible testing strategies, will be crucial in meeting the growing demand for chip performance and reliability in the AI era and beyond.

- SemiEngineering

#### **Rise of SLT**

"

It is only through **SLT testing** of devices, peripherals, and software together, under real-world conditions, that companies can drive down escape rates to acceptable DPPM) levels.

- Laura Peters, SemiEngineering

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#### ATPG / SLT (mis)correlation

Number of transistors doubles with each new node, yet the "percent coverage" of static ATPG (typically 99.5%) and at-speed ATPG (typically 85%) remains constant. This can create situations where emerging lower nodes can drive the number of untested transistors to unacceptable levels.

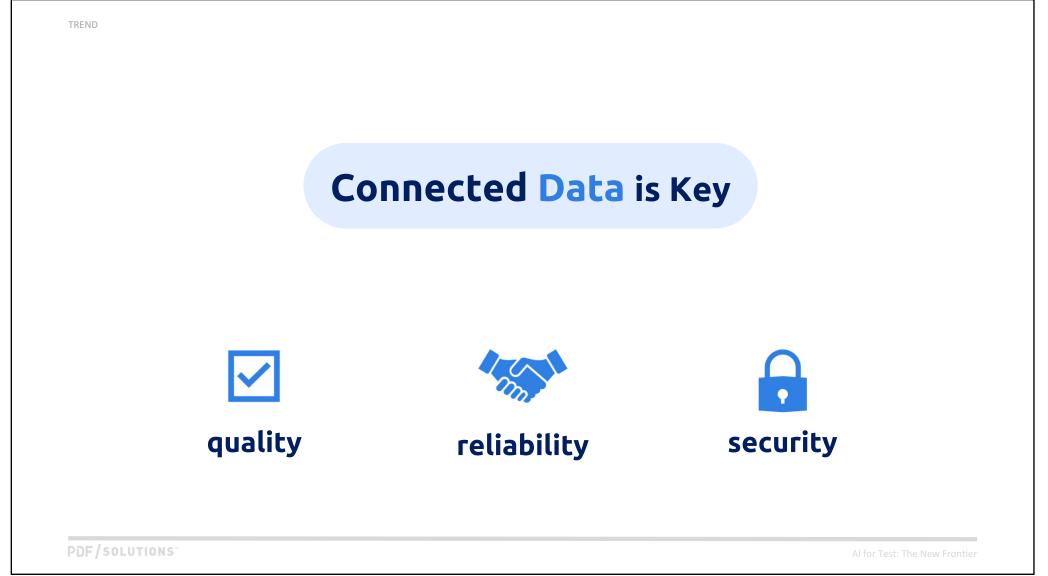
In system in package devices, even if each IP from different vendors provides 100% yield, combining different IP into a single package does not guarantee 100% coverage.

- Anil Bhalla, Electronic Design

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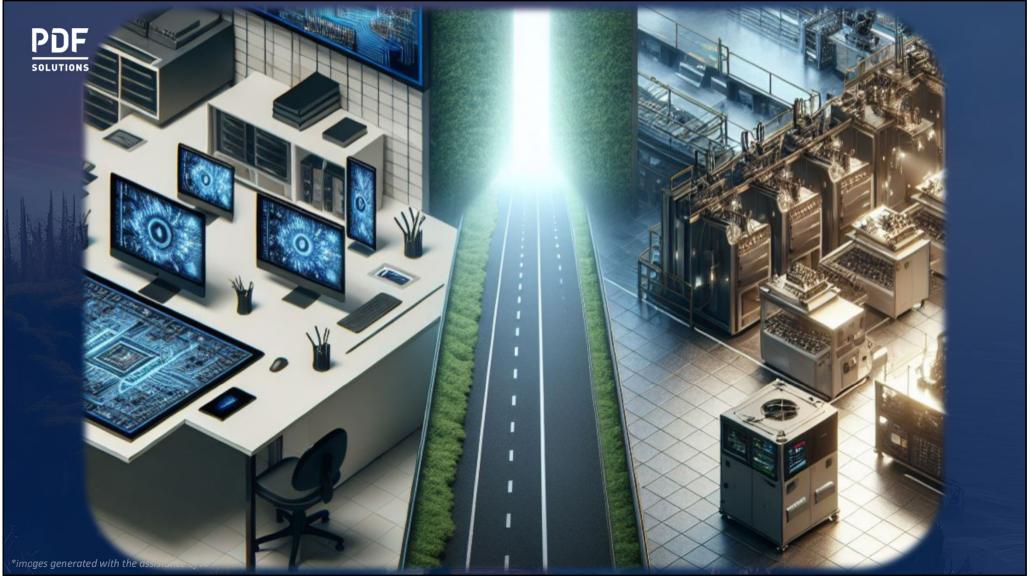




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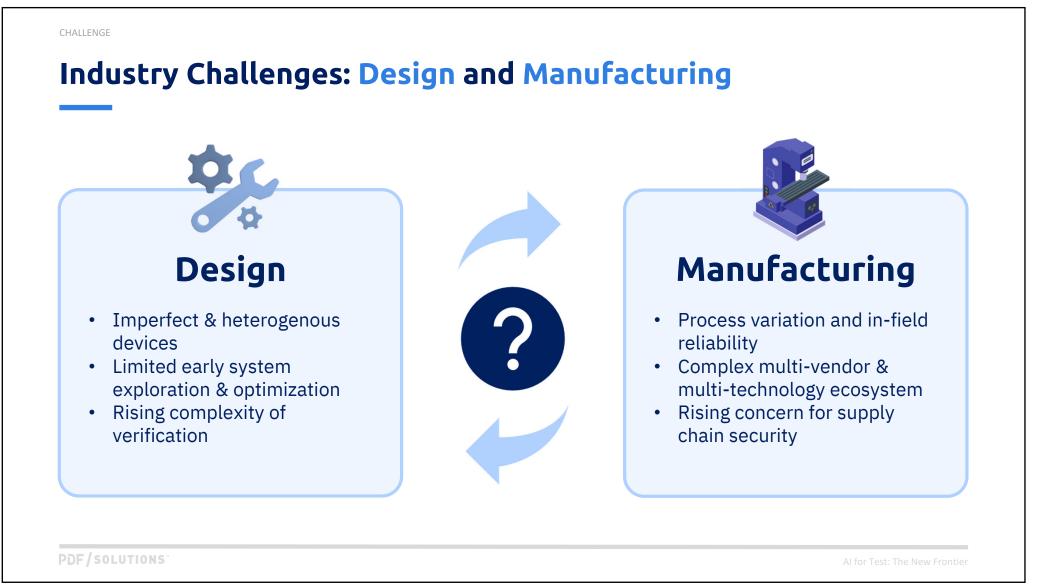
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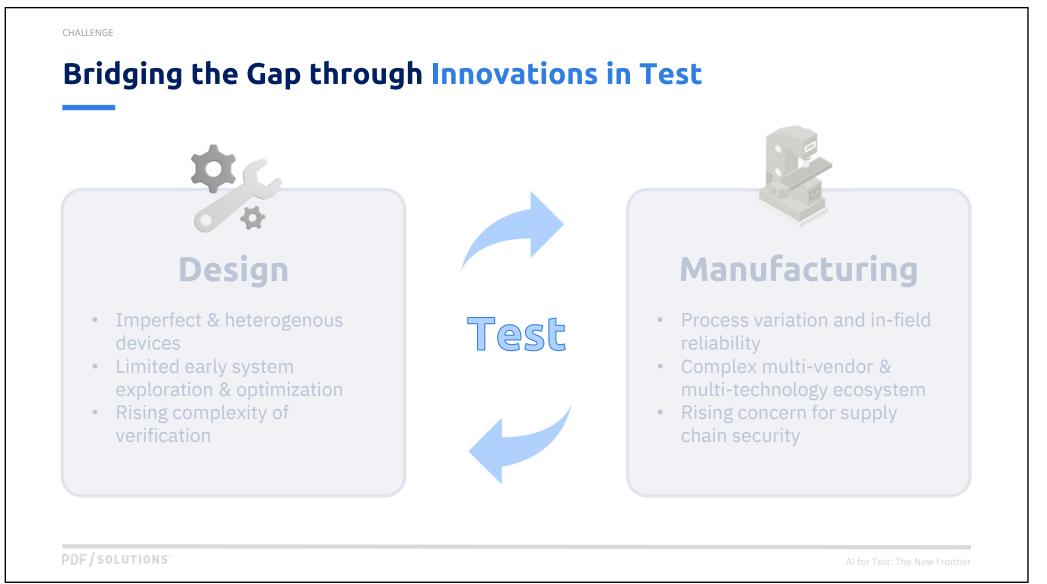


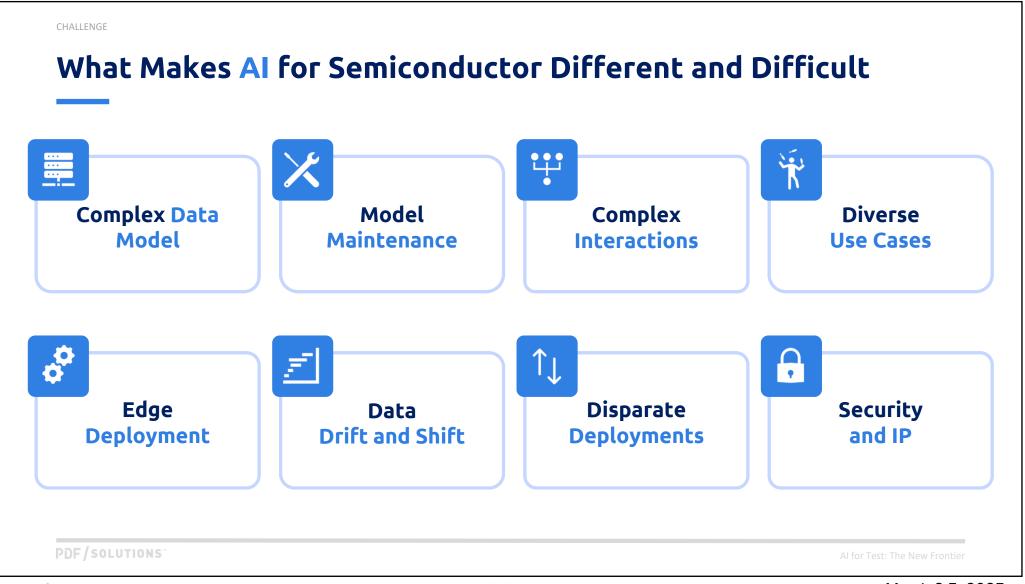
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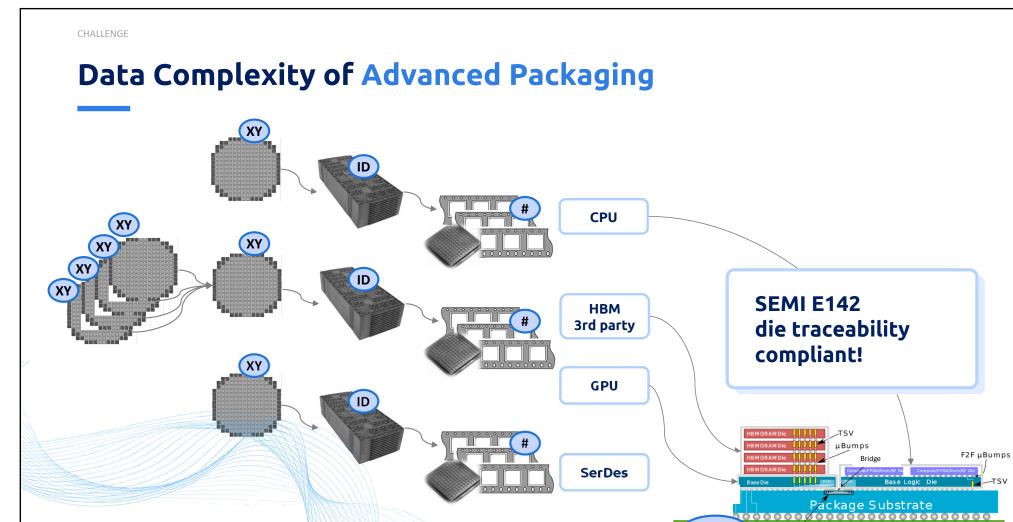
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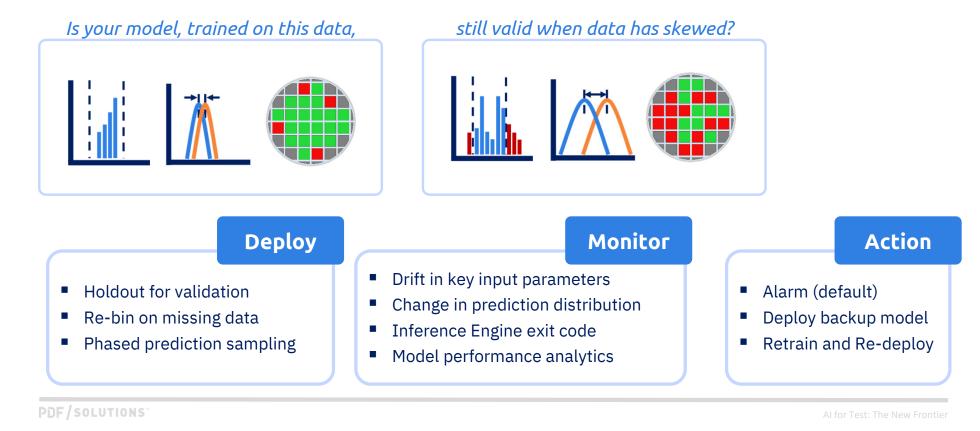
PART #

**Circuit Board** 

CHALLENGE

#### **The Interface Variation Problem**

ATE equipment, probe card, test socket, manufacturing sites





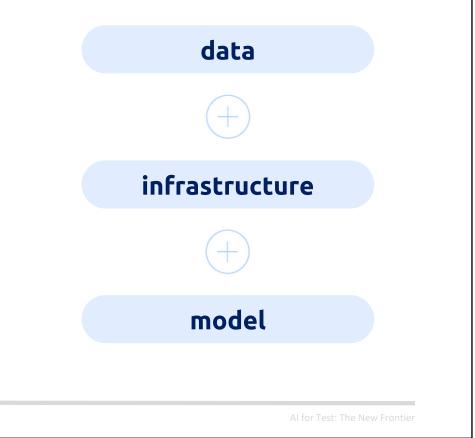
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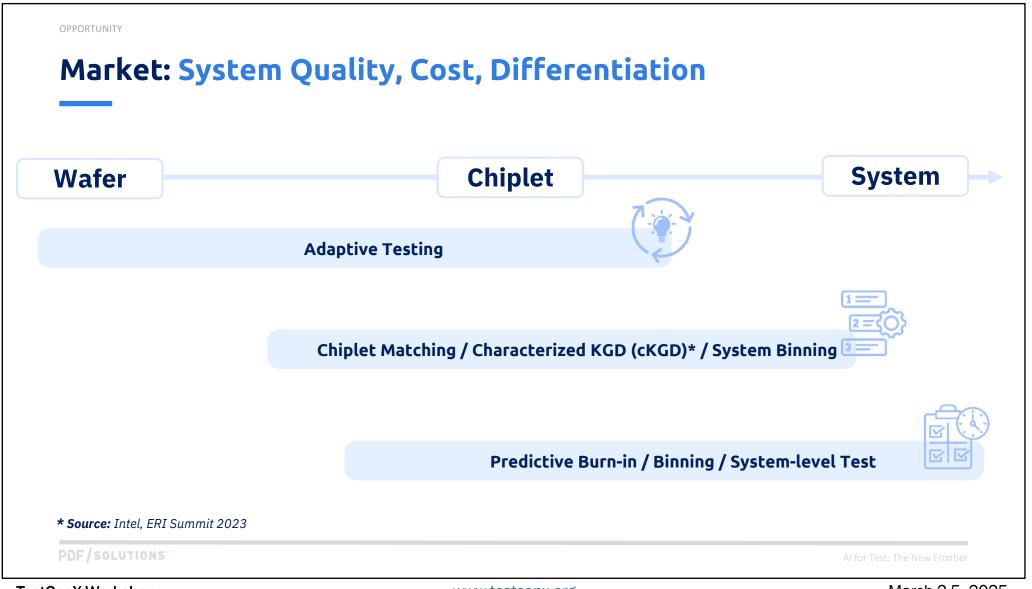
OPPORTUNITY

#### **Opportunity: Al for Test**

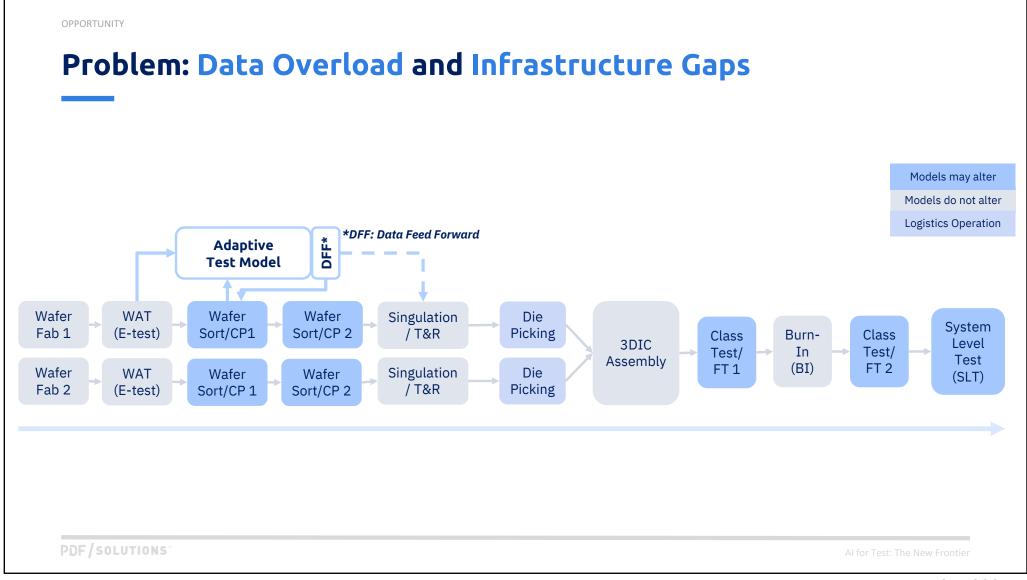


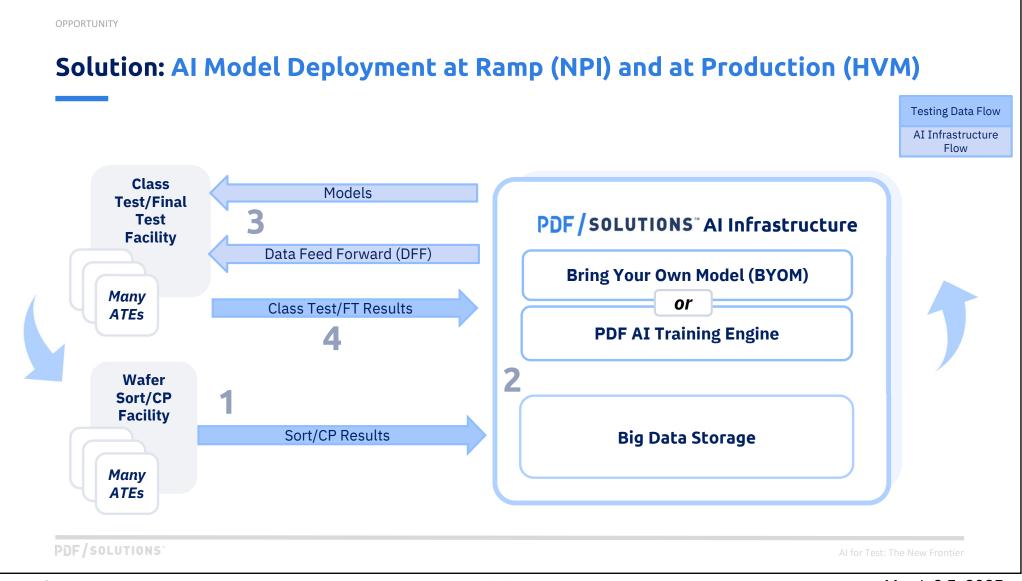


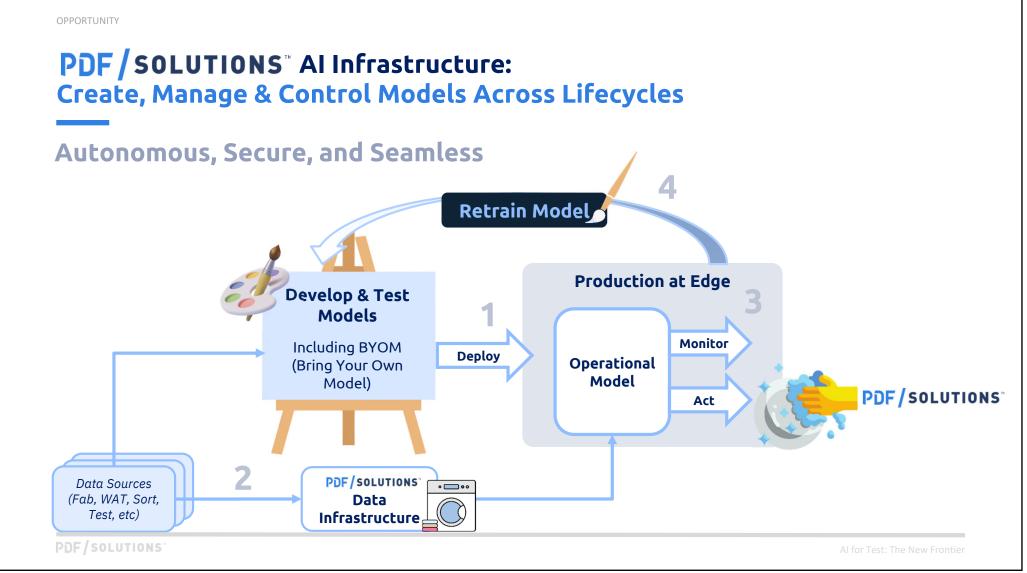
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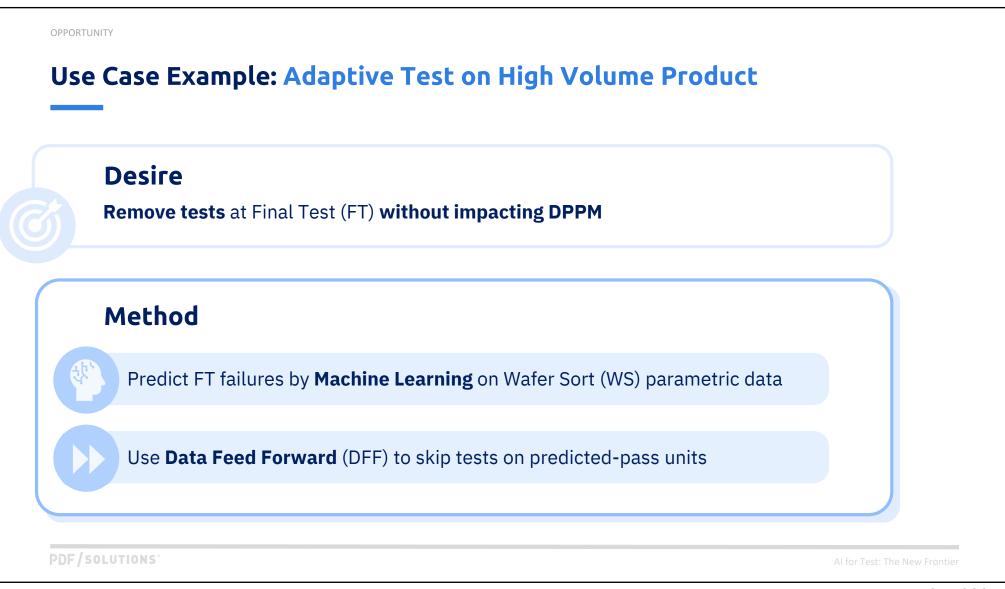


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OPPORTUNITY

#### Use Case: Results Summary

#### Results

- **5 / 7 tests** can be skipped with **0 DPPM**
- **Product decision needed** for the other 2 tests with **near-zero DPPM impact**
- Skip rates (fraction of units where test can be skipped) **above 88%**

| Target    | Current Failure<br>Rate (PPM) | DPPM (with ML) | ML Fail Captured% | ML Skip % |
|-----------|-------------------------------|----------------|-------------------|-----------|
| FT_Test_A | 82                            | 0.0            | 100.00%           | 99.26%    |
| FT_Test_B | 88                            | 0.0            | 100.00%           | 98.49%    |
| FT_Test_C | 220                           | 0.0            | 100.00%           | 96.63%    |
| FT_Test_D | 839                           | 0.0            | 100.00%           | 95.98%    |
| FT_Test_E | 540                           | 2.9            | 99.43%            | 95.25%    |
| FT_Test_F | 584                           | 0.0            | 100.00%           | 94.64%    |
| FT_Test_G | 255                           | 0.9            | 99.60%            | 88.14%    |

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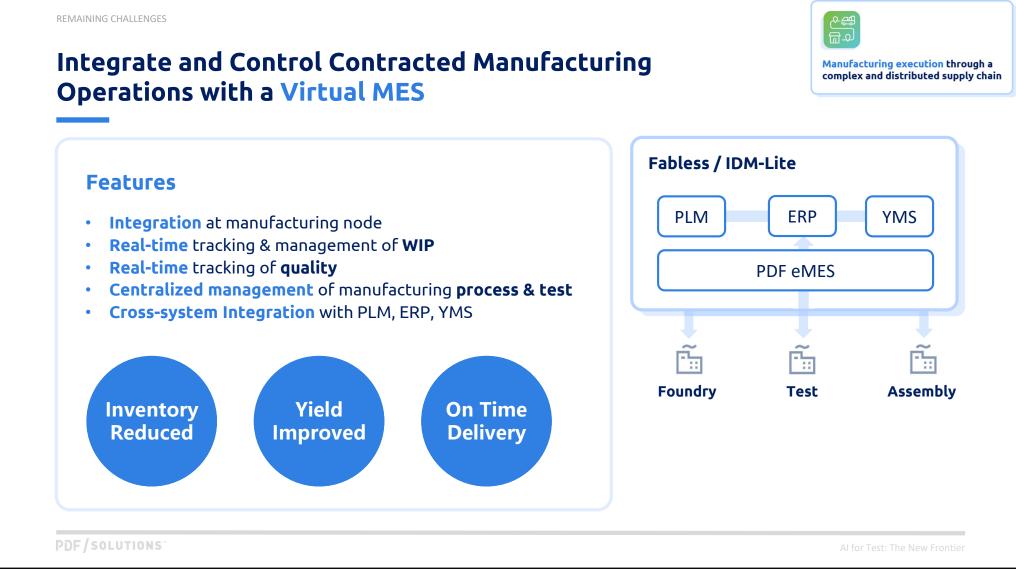
# PDF SOLUTIONS The Remaining Challenges

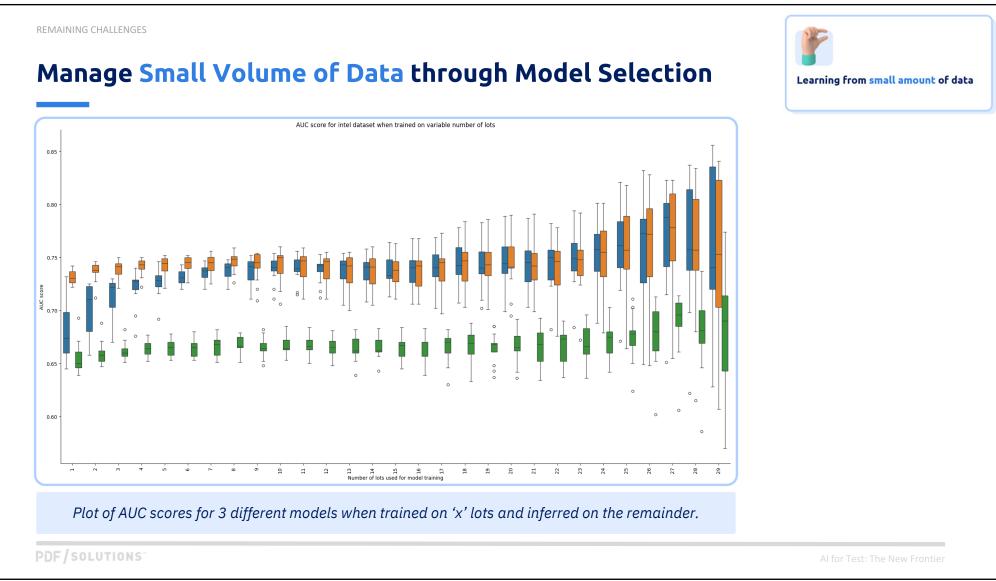
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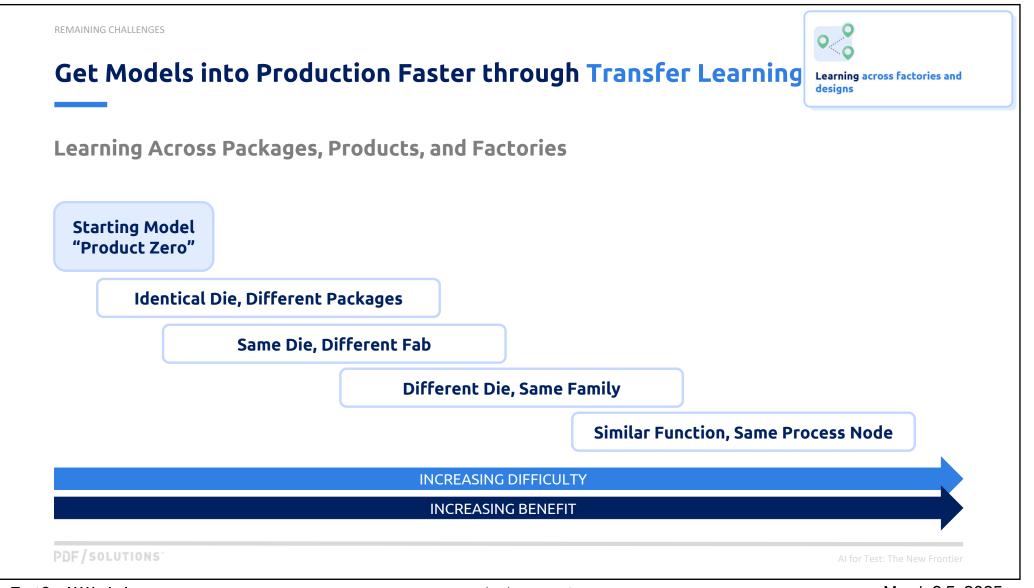
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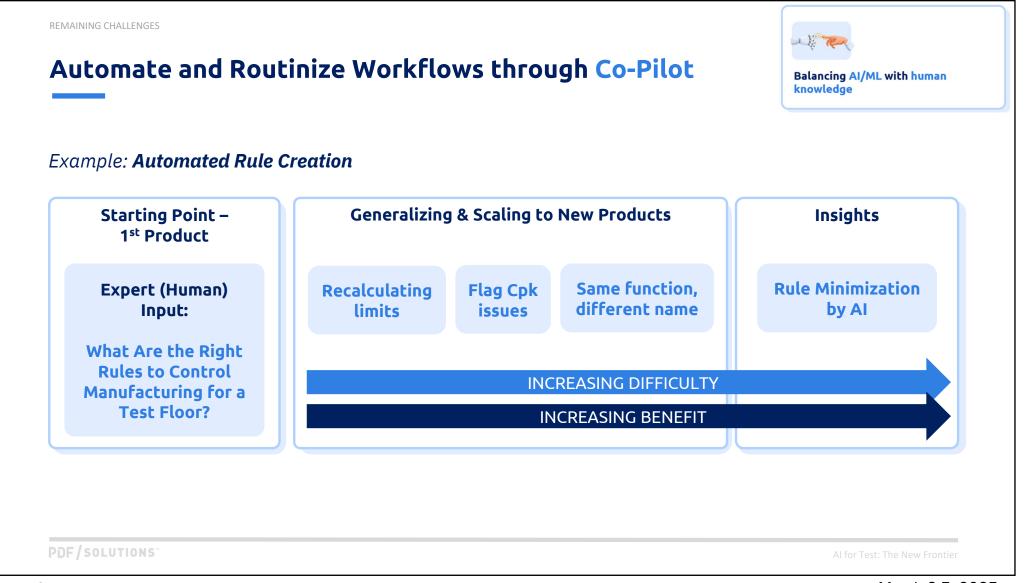
REMAINING CHALLENGES や追 ᠋ᢅᡆᠫ Manufacturing execution through a Learning from small amount of data complex and distributed supply chain Learning across factories and Balancing AI/ML with human knowledge designs PDF/SOLUTIONS

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REMAINING CHALLENGES

#### Key Takeaways

#### Al for test is a continuum of data, model, and infrastructure



Semiconductorspecific data, over space and time

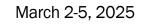


Connected view of a globally distributed supply chain Al across the design, manufacturing, and test lifecycles

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REMAINING CHALLENGES

#### PDF in the News

#### PDF Solutions to Acquire secureWISE to Expand the Reach of its Semiconductor Manufacturing Data Platform

POSTED ON FEBRUARY 19, 2025 BY PDF SOLUTIONS

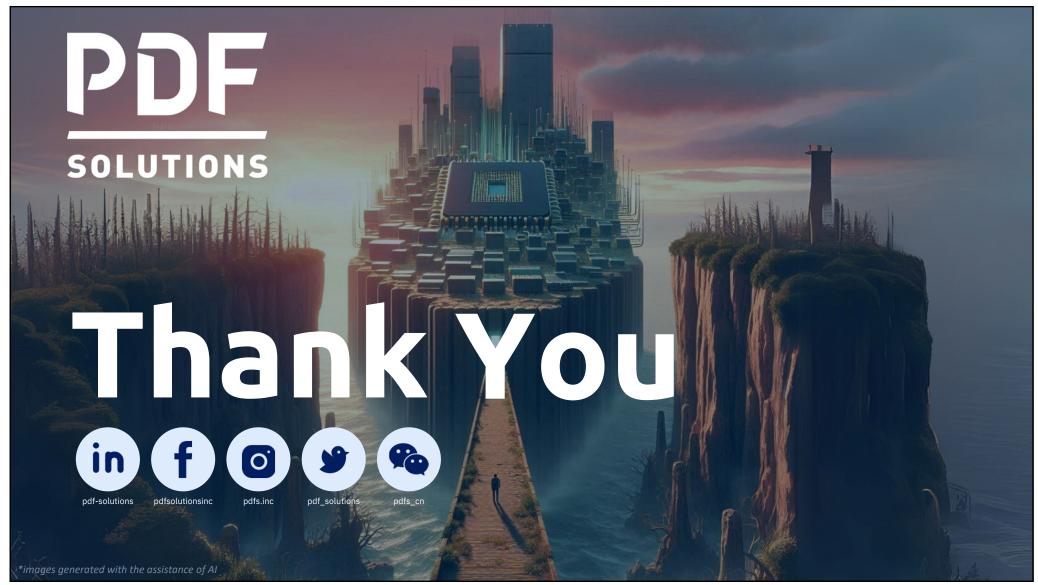
SECURE, REMOTE ACCESS, MONITORING, AND CONTROL FOR MANUFACTURING EQUIPMENT AT NEARLY 200 SEMICONDUCTOR FACTORIES WILL BE ADDED TO THE PDF SOLUTIONS DATA NETWORK

> As the semiconductor industry becomes more **globally distributed**, and as advanced devices rely on the integration of multiple chiplets into a single package, **more collaboration and integration are required** across the semiconductor industry. This collaboration needs to be executed securely with each participant controlling access to its intellectual property.

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