

Diagnostic plan for ATE production test board of large-scale chip

Jiang Lei
UNISOC



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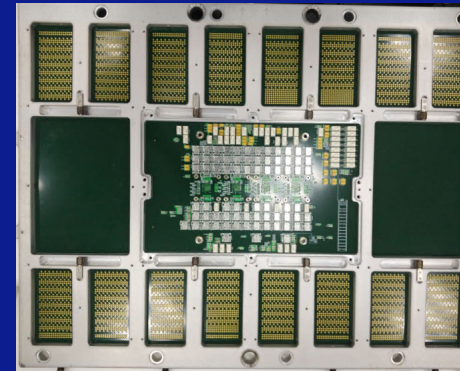


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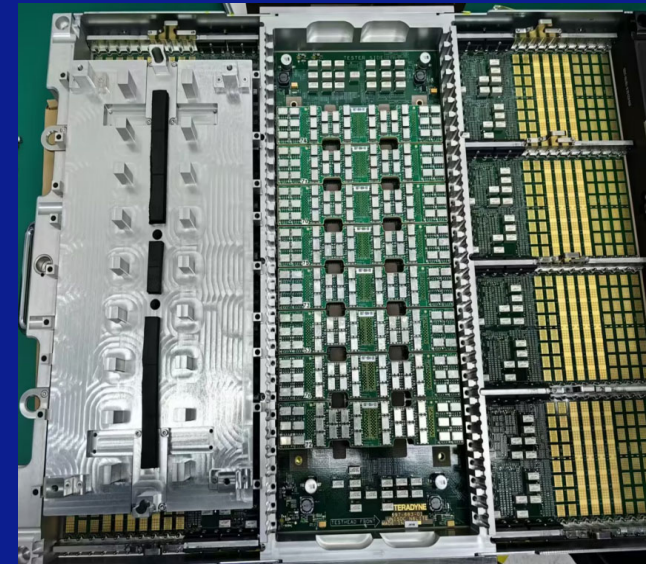
- Current situation of ATE board
- Diagnostic method of ATE board
- Dummy Device design & fabrication
- Dummy Device reference case
- Diagnostic program of ATE board
- Summary of diagnostic plan

Current situation of ATE board

- High Site Count, 12 or 16 Sites
- Large Size
- Too many devices
- Difficulty in Design & Fab
- Long delivery cycle
- High Cost
- Difficulty in Debug & Maintenance



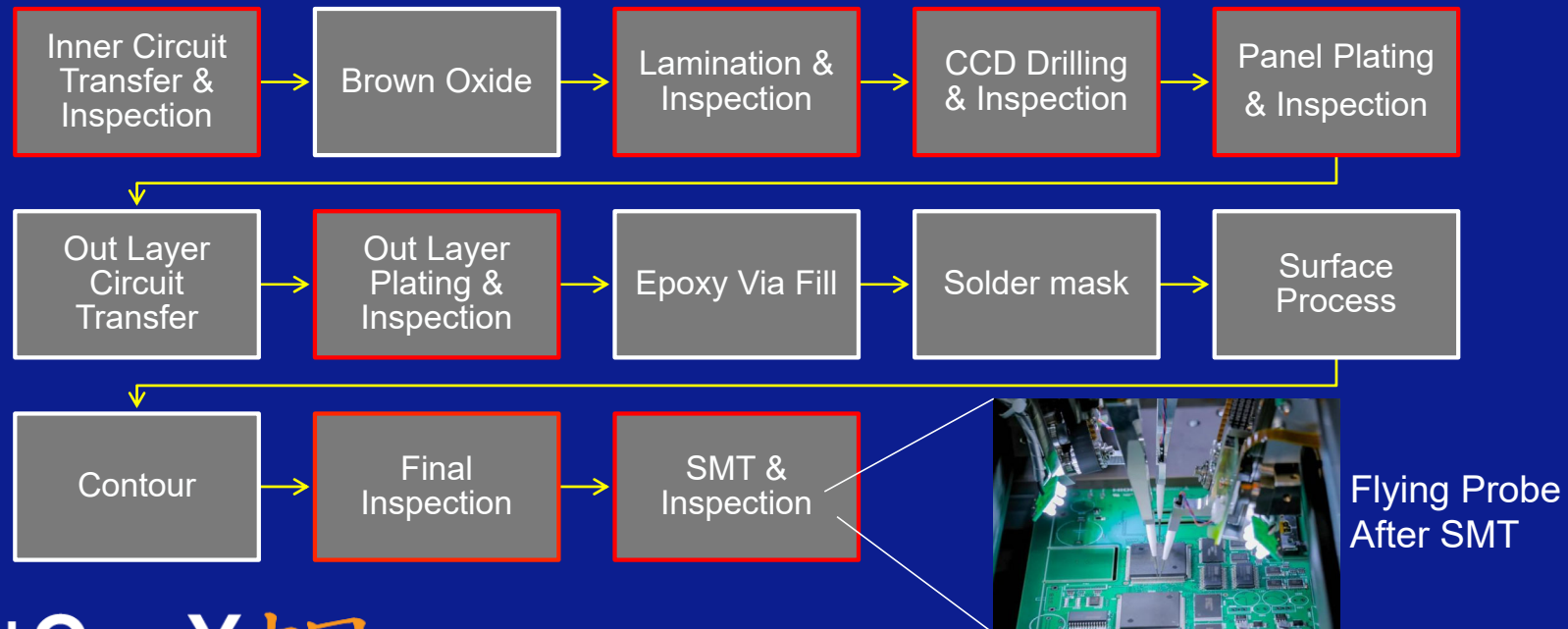
few years ago



Currently

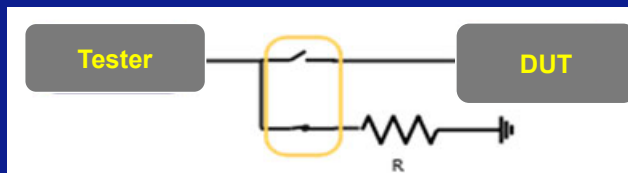
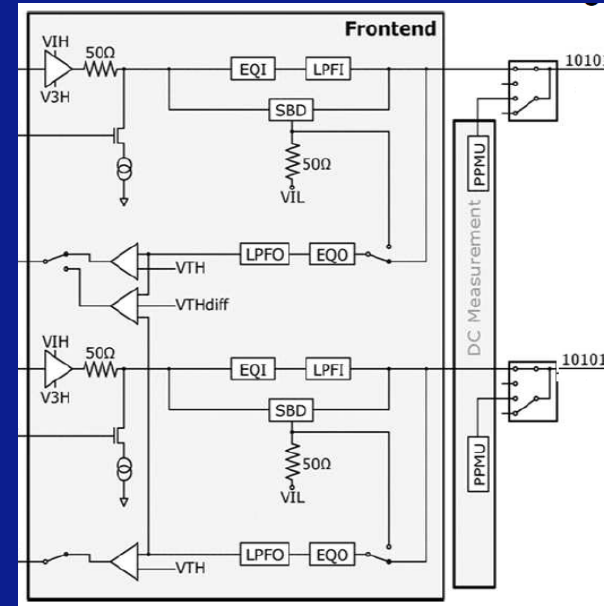
Current situation of ATE board

- Only PCB testing was completed during the fab process.
- The components have not been tested.

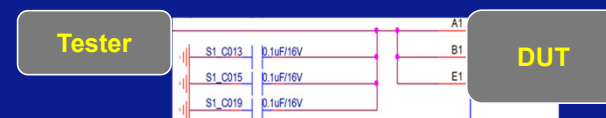


Diagnostic method of ATE board

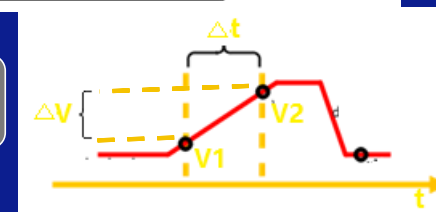
- Tester pin function:
 - Pin Parametric Measurement Units(PPMU)
 - Arbitrary Waveform Generator (AWG)
 - Driver
 - Digitizer
 - Comparator
 - Active Load



$$V = I * R$$

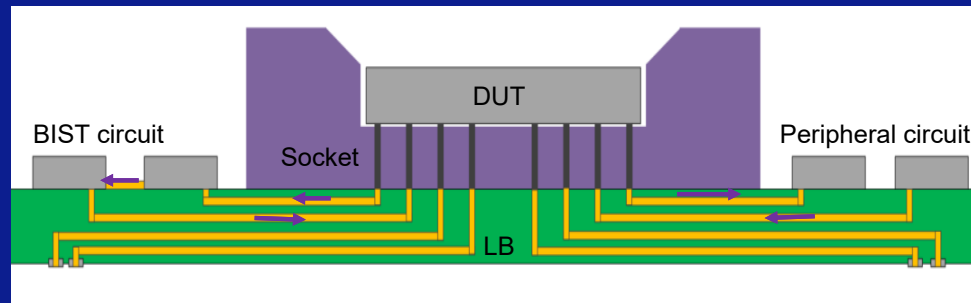


$$\Delta T = C * \Delta V / I$$



Diagnostic method of ATE board

- Large proportion of components are not connected to the tester
- Dummy Device or additional design is needed to improve test coverage

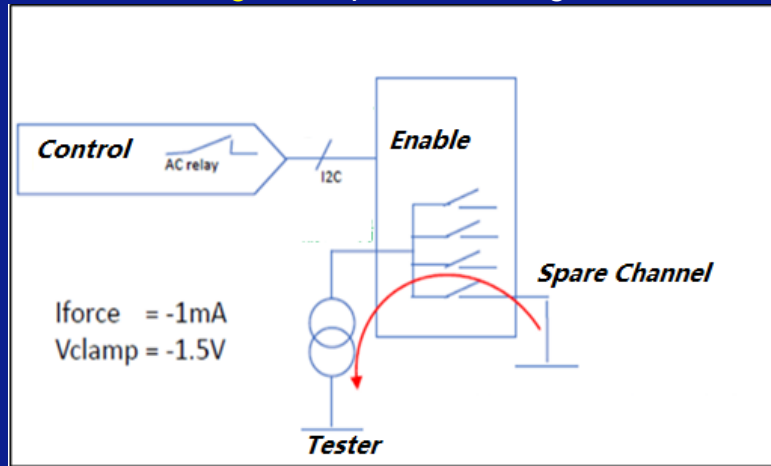


General ATE Test Circuit

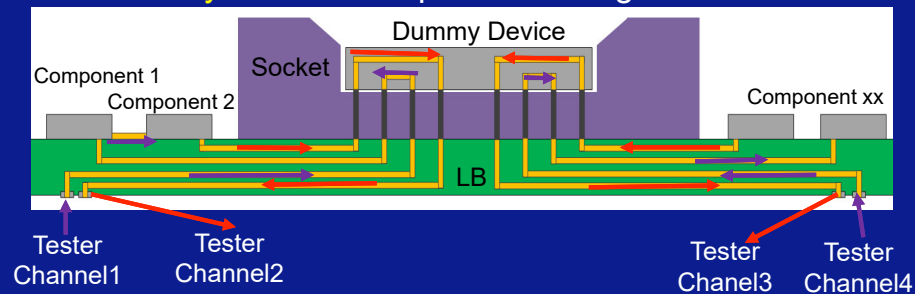
Module	Circuit on ATE board	Testability of Components
High Speed BIST	DUT → Switch → DUT	No
Resistance /Voltage Trim	DUT → Peripheral circuit → Tester	Partial Yes
RF Circuit	DUT → RF Matching Network → Tester	No
ADC/DAC	DUT → Op-Amp Circuit → Tester	No
Clock Input	TCXO/CLK IC → DUT	No

Diagnostic method of ATE board

Additional Design to improve coverage



With Dummy Device to improve coverage



Original Coverage 44%

Test Items	Total Qty	Additional Design		With Dummy Device		
		Testable Qty	%	Testable Qty	%	
Path	IO Leakage	4080	3664	0.898	3664	0.898
	IO Connectivity	4080	3632	0.8902	3632	0.8902
	Power Leakage	496	496	1	496	1
	Path Resistance	4576	0	0	0	0
	Path Functionality	0	0	0	0	0
Relay	Coil Status	240	220	0.9167	240	1
Cap	Capacitor	413	121	0.293	329	0.6804
	Cap Bank	424	336	0.7925	368	0.8679
Resistor		1319	571	0.4329	1109	0.724
Diode		233	229	0.9828	229	0.9828
IC	xc6219a182mr	16	0	0	16	1
	wl2820d18-4/tr	16	0	0	16	1
	tmuxhs4412iruut	160	80	0.5	160	1
	tmp451aqdqwrq1	16	0	0	16	1
	mic39102ym	16	0	0	16	1
	adg1606bruz	64	64	1	64	1
	52mhz	16	0	0	16	1
	mt25ql128	1	1	1	1	1
	mc33063ad	4	0	0	4	1
Component Overall		2938	1622	55.21%	2584	87.95%

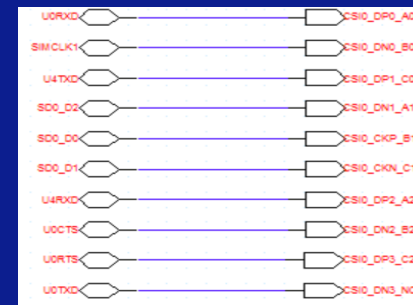


Diagnostic plan for ATE production test board of large-scale chip

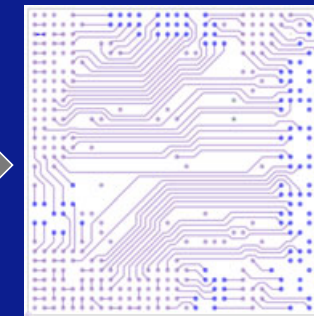


Dummy Device design & fabrication

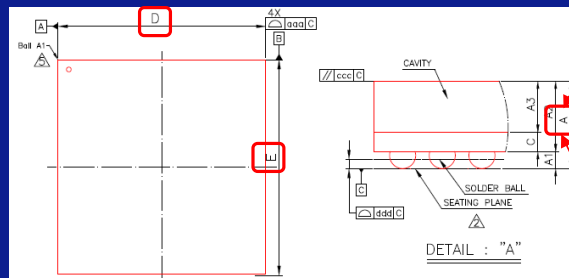
- Easy to design
- Same Size with chip POD
- PCB PTH(Plated through hole) Process
- With Solder Ball or NiPdAu PAD
- Panel Fab



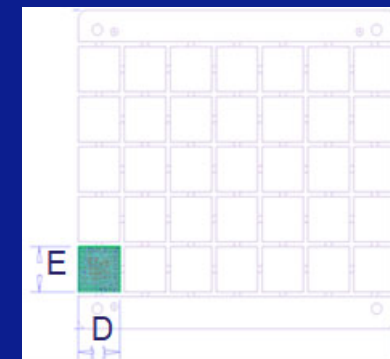
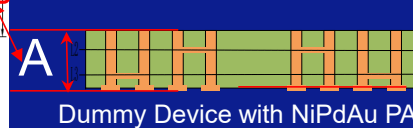
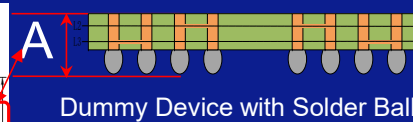
Schematic Design



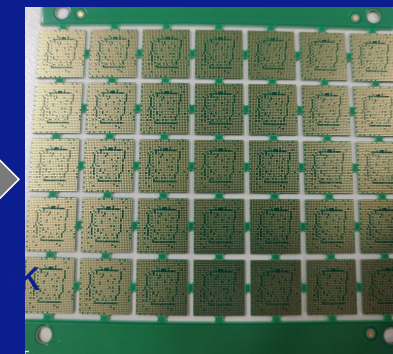
PCB Design



Chip POD



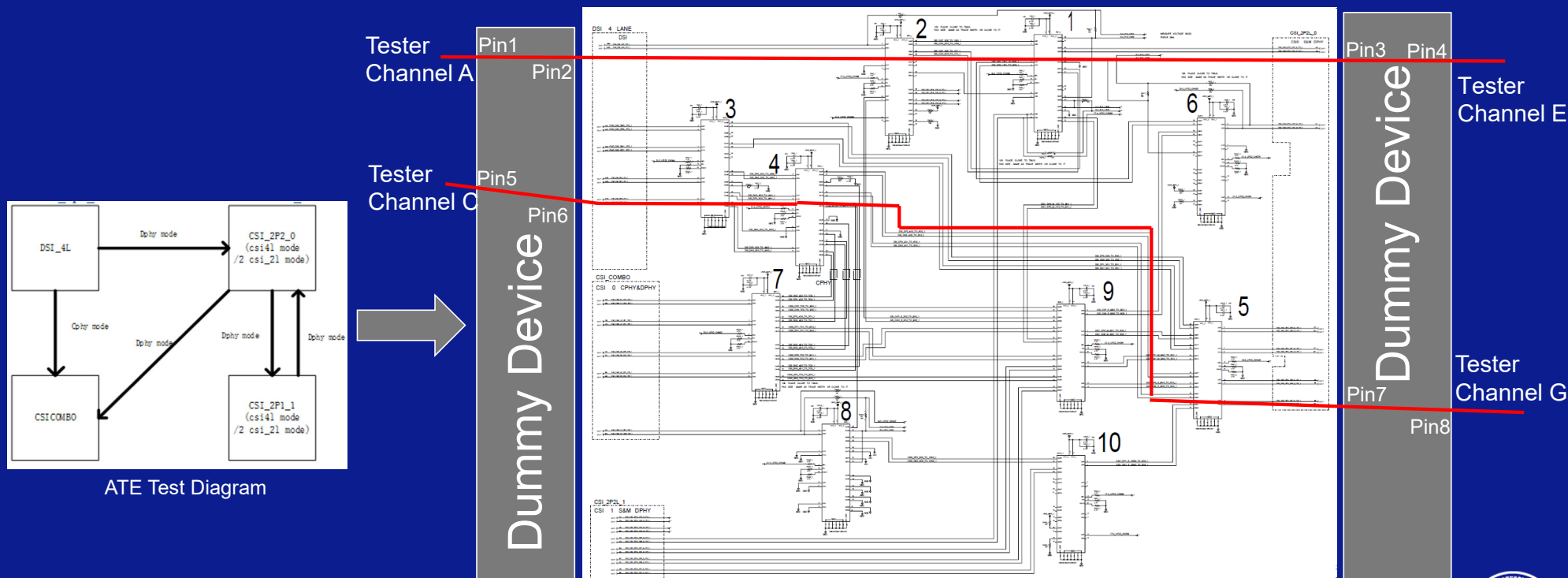
Panel Drawing



PCB with NiPdAu PAD

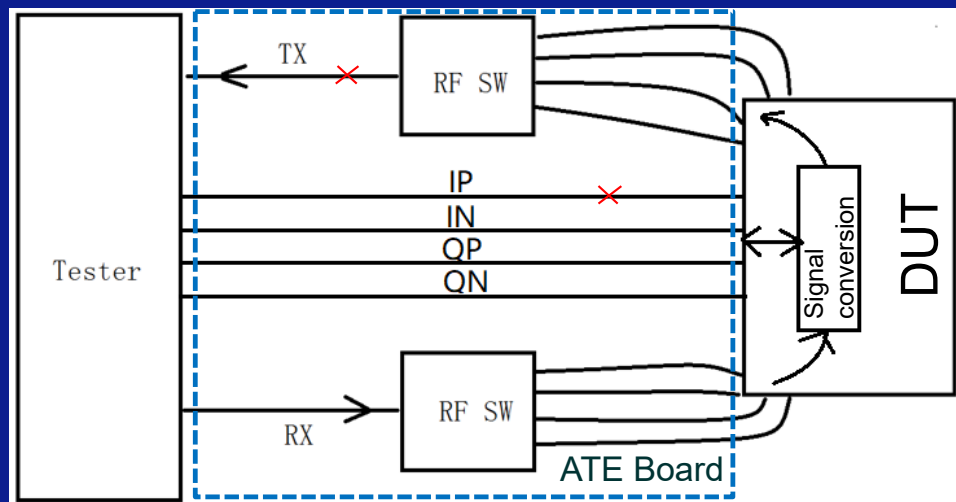
Reference case1 – High Speed BIST

- With Dummy Device, we can test all the high speed analog switch

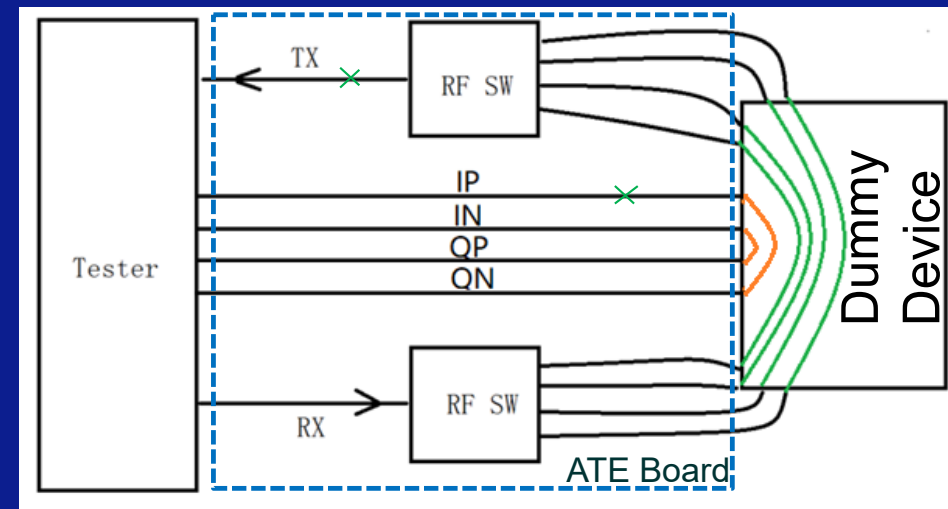


Reference case2 – RF Chip

- With Dummy Device, we can test both the RF Path and IQ Path



RF Chip ATE Test Diagram



Dummy Device Test ATE Board

Diagnostic Program of ATE board

- Open Socket Flow(Without Dummy Device)

- IO Path
- Power Path
- UDB Path
- User Power

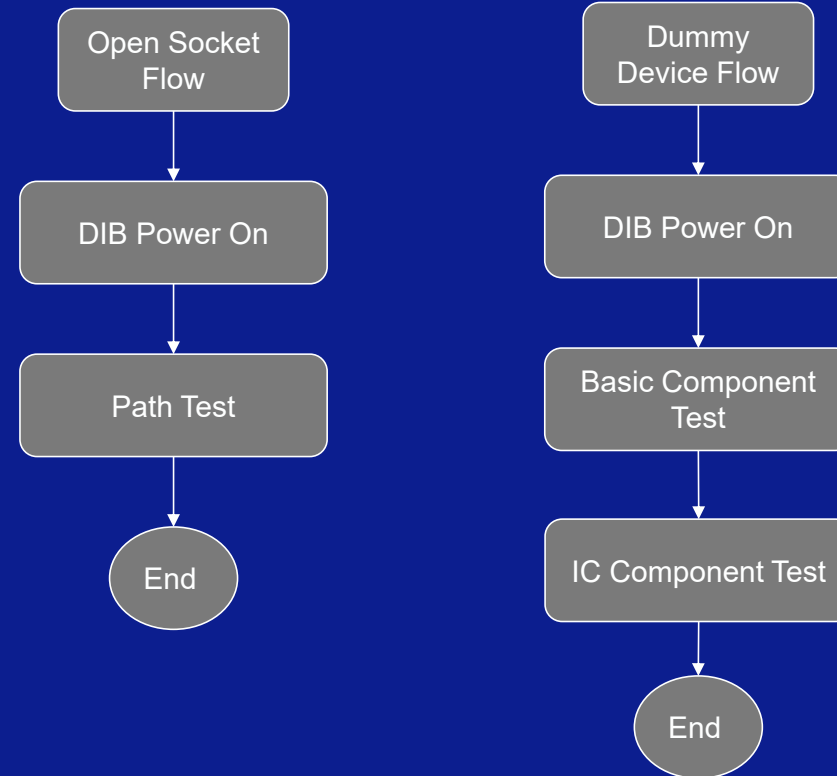
- Dummy Device Flow

Basic Component

- Res
- Cap
- Relay

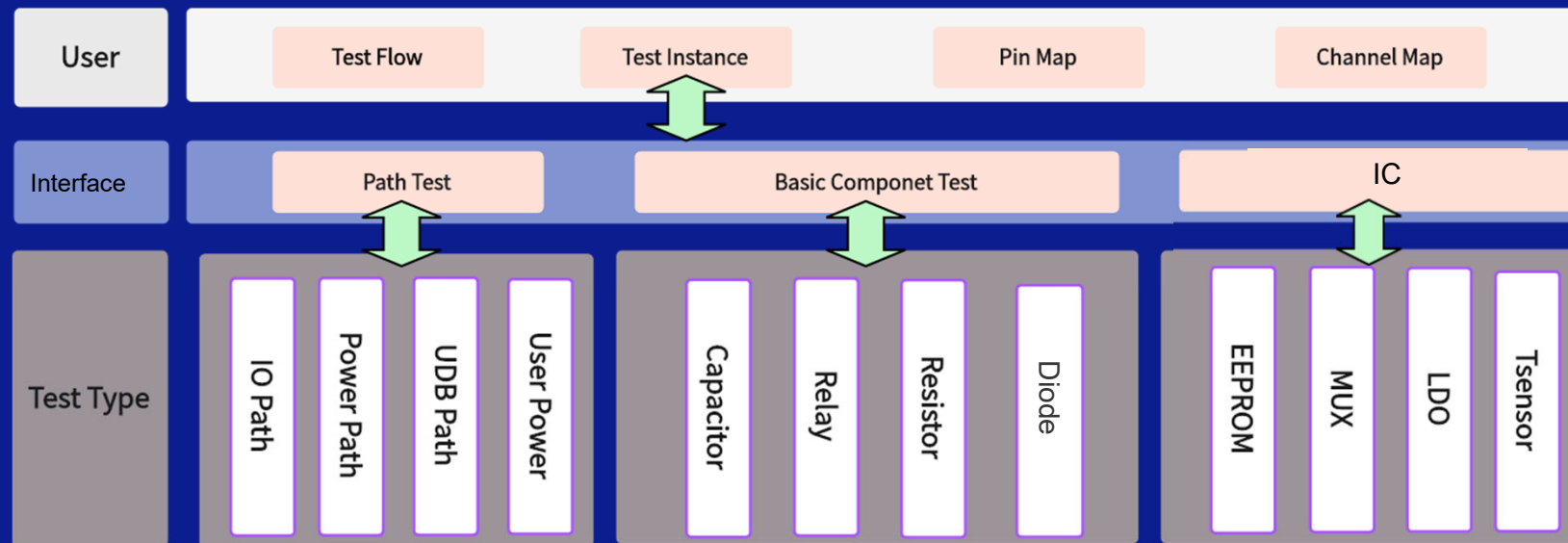
IC Component

- Analog Switch
- Clock IC
- Op-Amp....



Diagnostic Program of ATE board

- Hierarchical Modular Design For Program

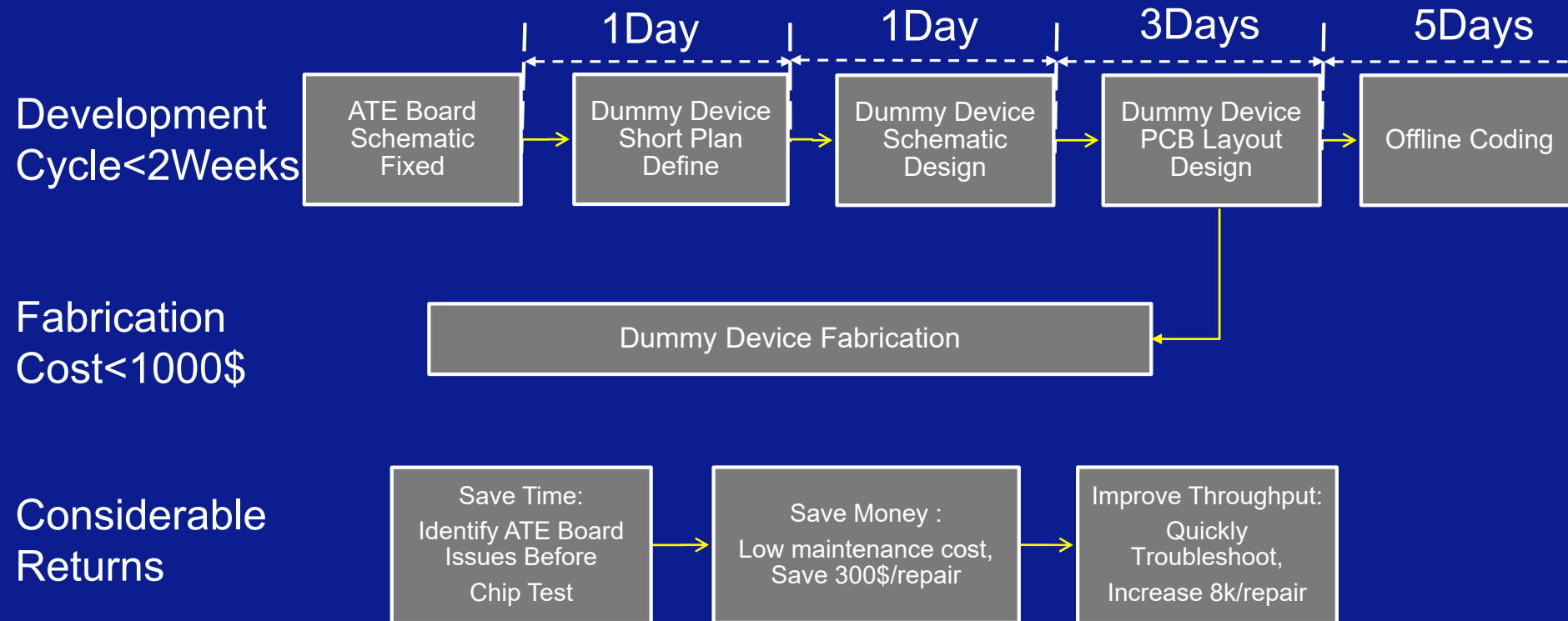


Diagnostic Program of ATE board

- Easy to develop programs

TestType	Test Pin Parameters			Initial Pin Parameter	Relay Control Setup Parameters			Datalog Results Parameters				Datalog Results	
	TestPin	Force Value	Clamp Value	Initial Value	UDB CtrlOn	UDB CtrlOff	PPMU Ctrl Pin Volt	Limit Hi	Limit Lo	Expect Value	Unit	Setup Time	Coms On Path
RES_FIM V	Pin1	I_value	H:1;L:0	Pin2=0V	Utility Pin1	Utility Pin5	CtrlPin1=0; CtrlPin2=3.3	R_limitHi	R_limitLo	R_Value	Ohm	Waiting Time	Rxx; Kxx;
CAP_FI MV	Pin3	I_value	H:1;L:0	Pin4=0V	Utility Pin2	Utility Pin6	CtrlPin3=0; CtrlPin4=3.3	C_limitHi	C_limitLo	C_Value	F	Waiting Time	Cxx; Kxx
RLY_FIM V	Pin5	I_value	H:1;L:0	Pin6=0V	Utility Pin3	Utility Pin7	CtrlPin5=0; CtrlPin6=3.3	V_limitHi	V_limitLo	/	V	Waiting Time	Kxx; Kxx

Summary of Diagnostic Plan



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