

The trend of technology convergence between RF test and high-speed digital signal test in emerging fields

Daniel Xiao

MET TECHNOLOGY CO., LTD.



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Outline

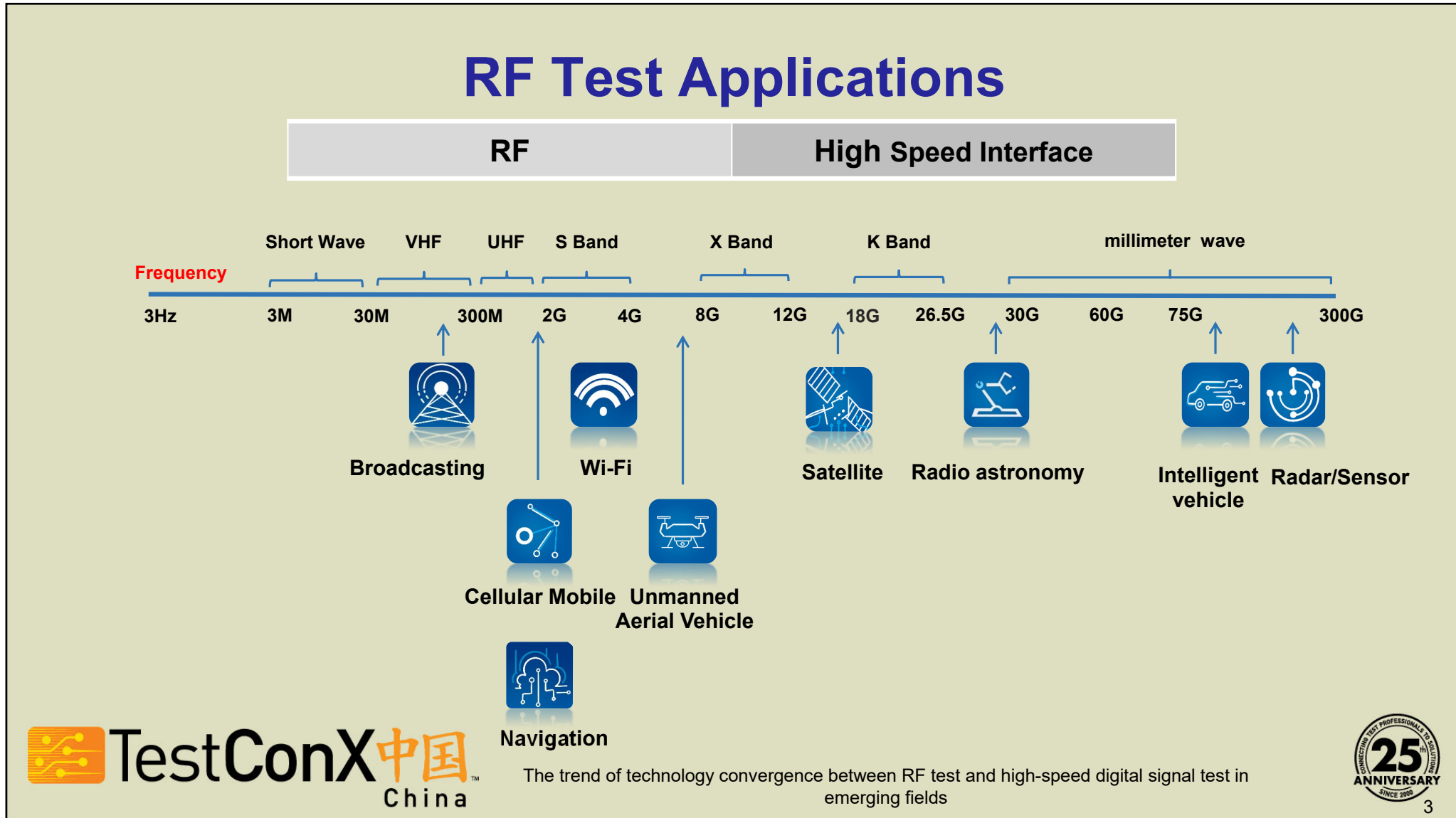
- **Applications for RF and high-speed devices**
- The convergence trend of DUTs in emerging fields
- The convergence trend reflected in the technological evolution of the tester itself
- Some typical cases

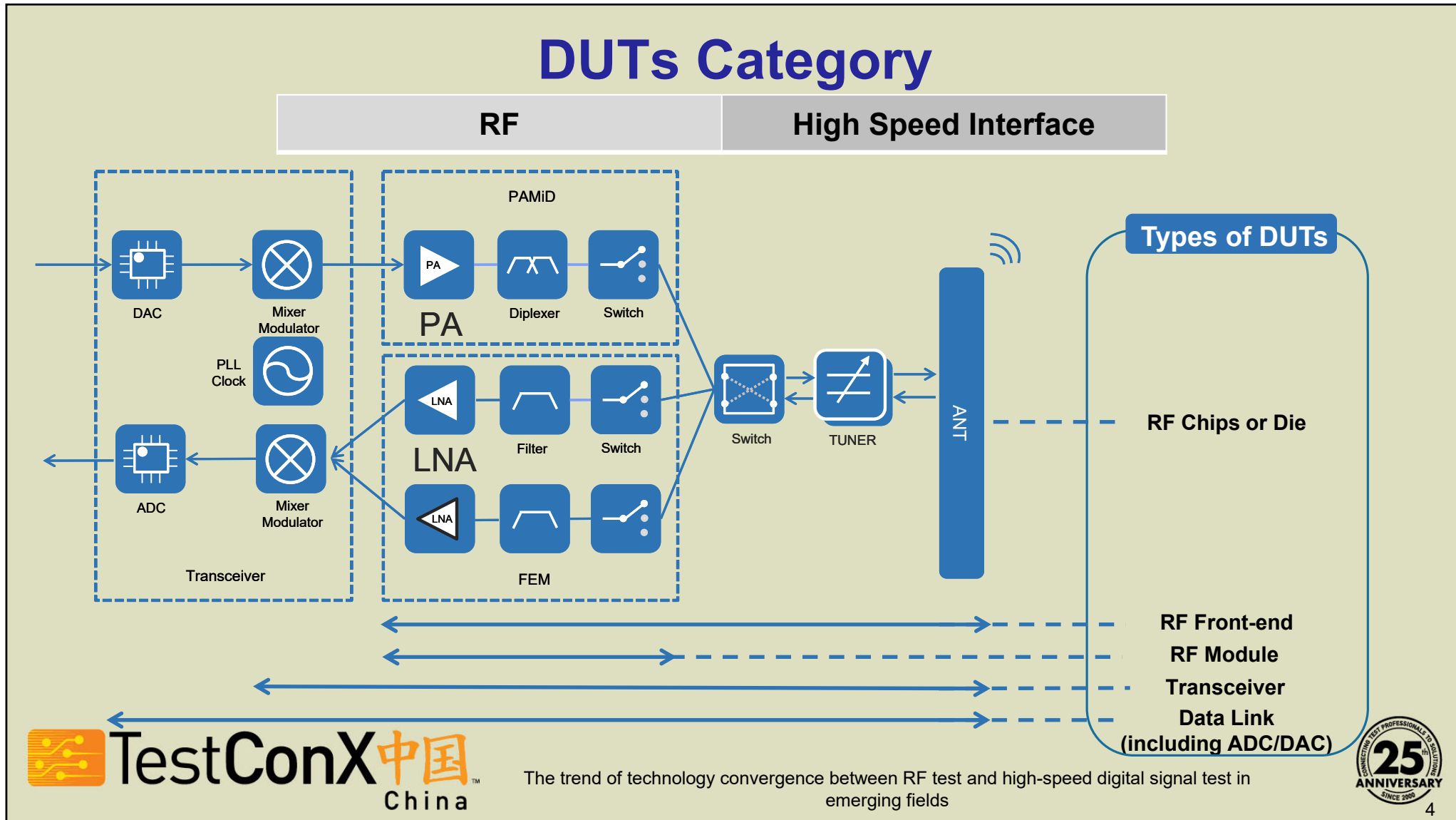


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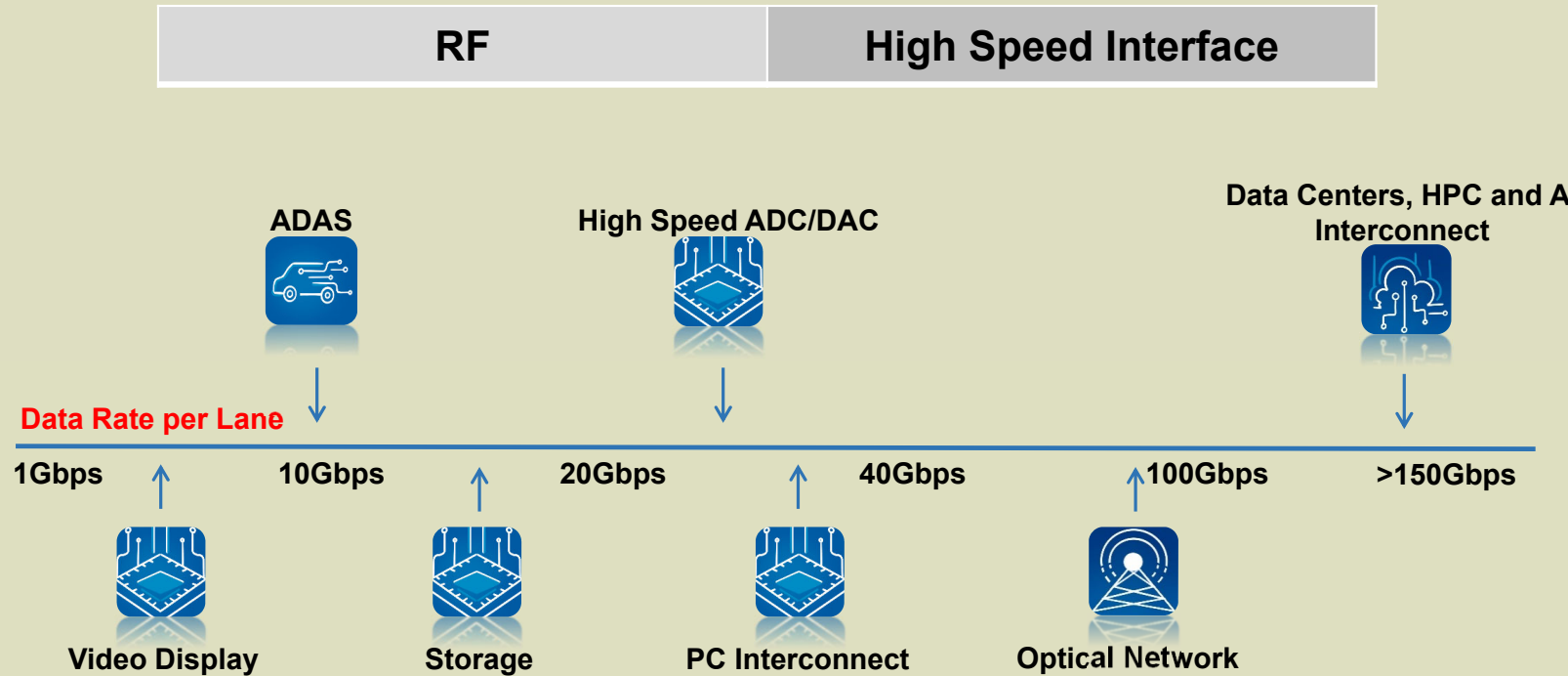


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High Speed Test Applications



DUTs Category

RF

High Speed Interface

Data bus for AI

PCIe gen3/4/5/6
NVME 1.4/2.0
DDR 5



Automotive

IEEE 802.3bw(100BASE-T1), IEEE
802.3bp(1000BASE-T1), FPD LINK III(5Gbps)



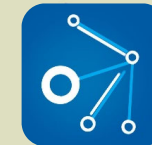
Peripheral Interconnect

USB 3.0/3.1/3.1/3.2/4.0



Data Centers

802.3bs/802.3ck (400G Ethernet)



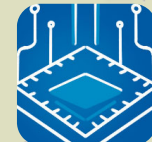
Display Port

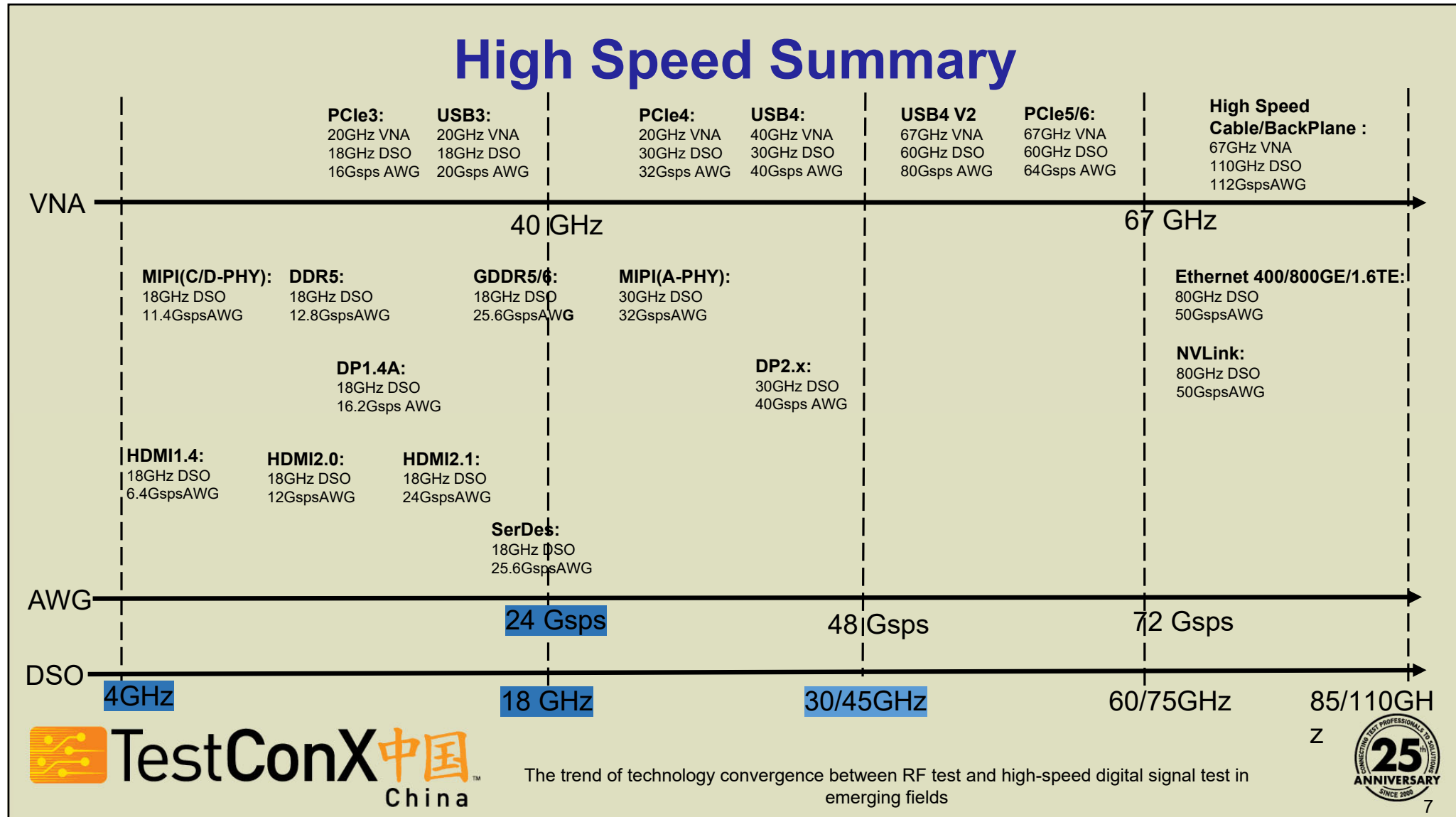
HDMI 1.4/2.0/2.1, display port 1.4/2.0



Optical fiber communication

IEEE 802.3ab





TECHNOLOGY and INNOVATION



RF Tester for

- WiFi Chips/Devices
- 5G NR Chips/Devices
- Satcom Chips/Devices
- Radar(mmW) Chips
- GNSS Chips.



High Speed Interface Tester for

- USB4/USB4 V2
- PCIe
- DDR5
- HDMI/DP/MIPI
- Serdes(Automotive)
- Data Center Interconnection
- AI Interface
- Backplane
- High Speed Ethernet



Test Cards

- DSO
- AWG
- VST
- VSA
- HSIO
- VNA
- VSG



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- The convergence trend reflected in the technological evolution of the tester itself
- Some typical cases



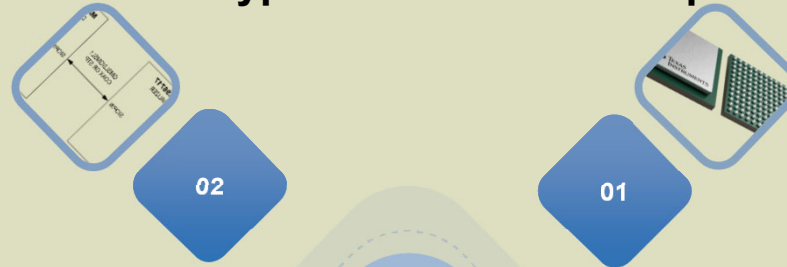
The trend of technology convergence between RF test and high-speed digital signal test in emerging fields



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Covergence trends in DUTs in emerging fields

Take two types of DUTs as examples



High speed serial interface

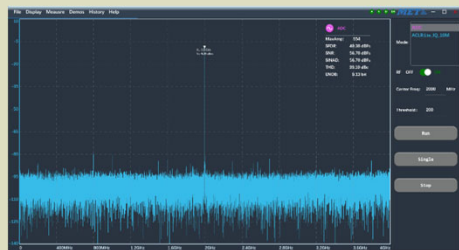
- PCIe
- USB V4
- HDMI/DP
- MIPI
- Automotive SerDes
- High-speed Ethernet

RF sampling ADC/DAC

- WiFi SoC
- Cellular base stations
- radar
- UAV broadband data link
- Optoelectronic interface
- Test equipment

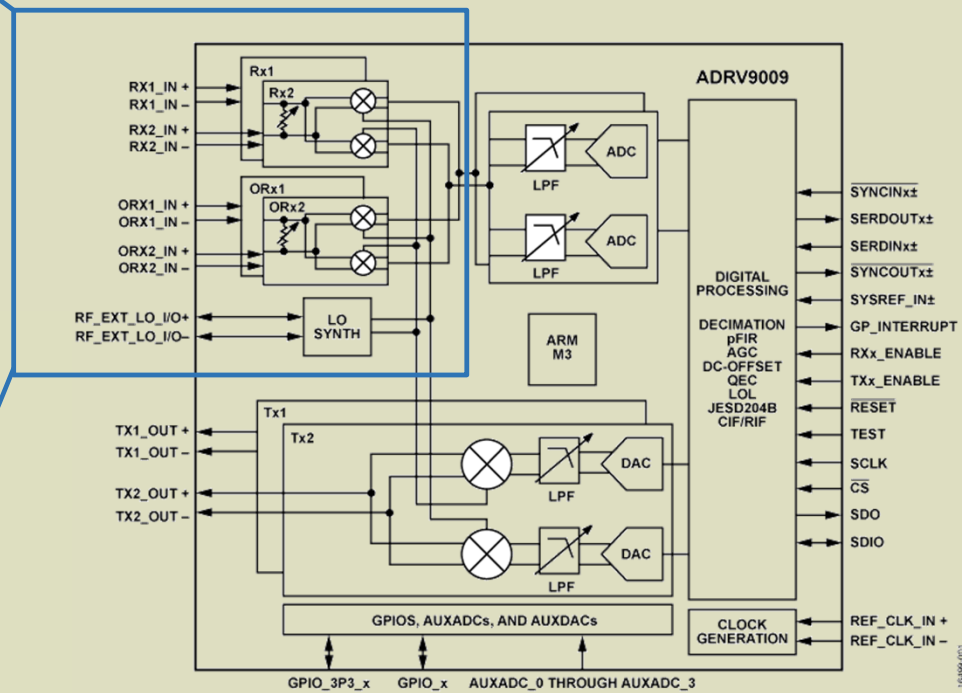
Typical applications

Example A: RF Transceiver



Rx RF spec.

- Channel
 - Center Frequency
 - ORx Bandwidth
 - Flatness @ any xM BW
 - Phase linearity
- ORx Gain
 - Gain Control Range
 - Gain Resolution
- Distortion
 - Alias Band Rejection
 - 2/3rd Input Intermodulation Intercept Point (IIP2/3)
 - 3rd/5th/7th-order Intermodulation Product (IM3/5/7)
 - Receiver Band Spurs
 - 2nd/3rd Harmonic Distortion (HD2/3)
 - Image Rejection (IRR)
 - LO Leakage (LOL)
 - Tx-to-ORx Isolation
 - ORx-to-ORx Isolation



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Example A: RF Transceiver

Tx RF spec.

Channel

- Center Frequency
- Tx Synthesis Bandwidth
- Tx Large Signal Bandwidth
- Flatness @ any xM BW
- Phase linearity

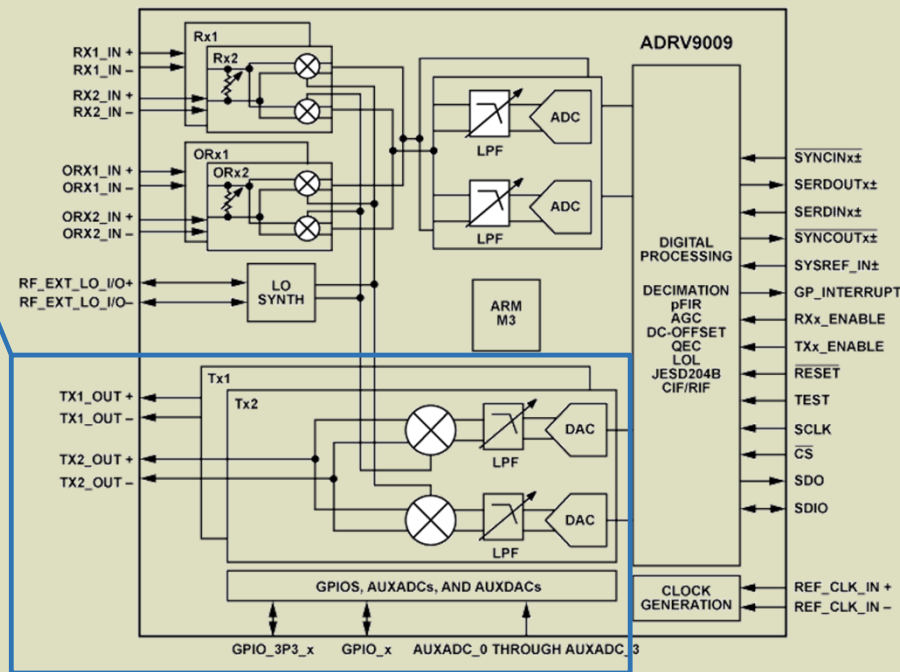
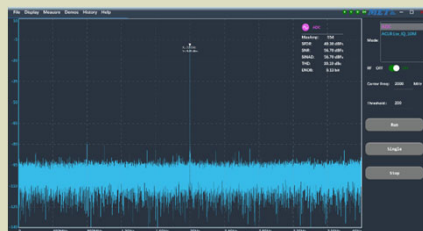
Tx Attenuation

- Atten. Control Range/ Resolution
- Atten. INL/DNL
- SPI to Atten. timing

Distortion

- Adjacent Channel Leakage Ratio (ACLR)
- In Band Noise Floor
- Out of Band Noise Floor
- Interpolation Images
- Tx-to-Tx Isolation
- Image Rejection (IRR)
- 3rd Output Intermodulation Intercept Point (OIP3)
- LO Leakage (LOL)
- Error Vector Magnitude (EVM)

Maximum Output Power



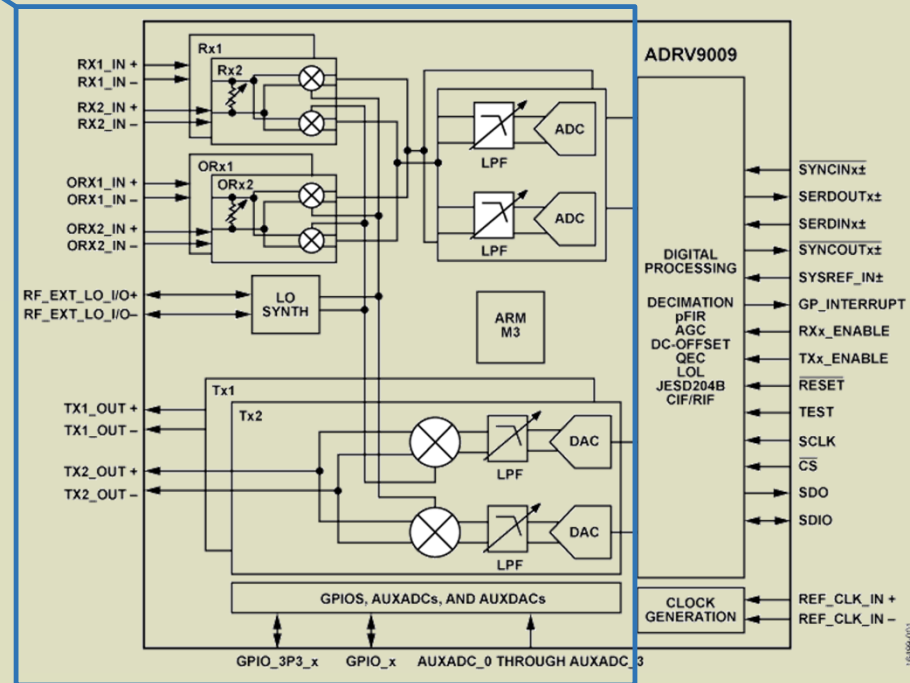
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Example A: RF Transceiver

State of the art

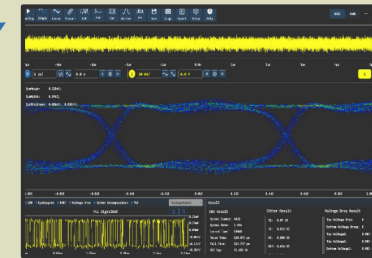
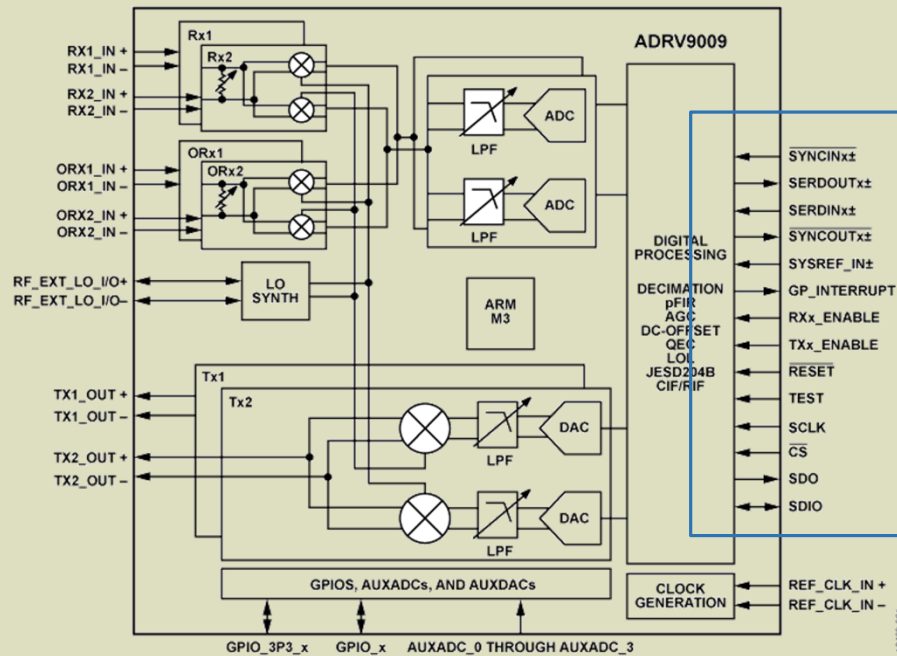
- ☀ RF Frequency: 18GHz
- ☀ Bandwidth: up to 12GHz
- ☀ SFDR: over 70dB
- ☀ PN: -140dBc @1GHz @1kHz
- ☀ EVM: over -50dB @WiFi 7



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Example A: RF Transceiver



JESD204B/JESD204C

Supports **0.3125 - 32 GBaud** output with 1 Baud symbol rate stepping.

capability of **jitter and noise injection**.

Supports fixture and channel embedding/de-embedding functions

Supports clock data recovery (**CDR**)

Eye diagram test: automatically measures eye height, eye width, eye thickness and jitter, supports user-defined eye diagram templates;

Jitter analysis: support for RJ/PJ/DDJ/DCD and other jitter term decomposition

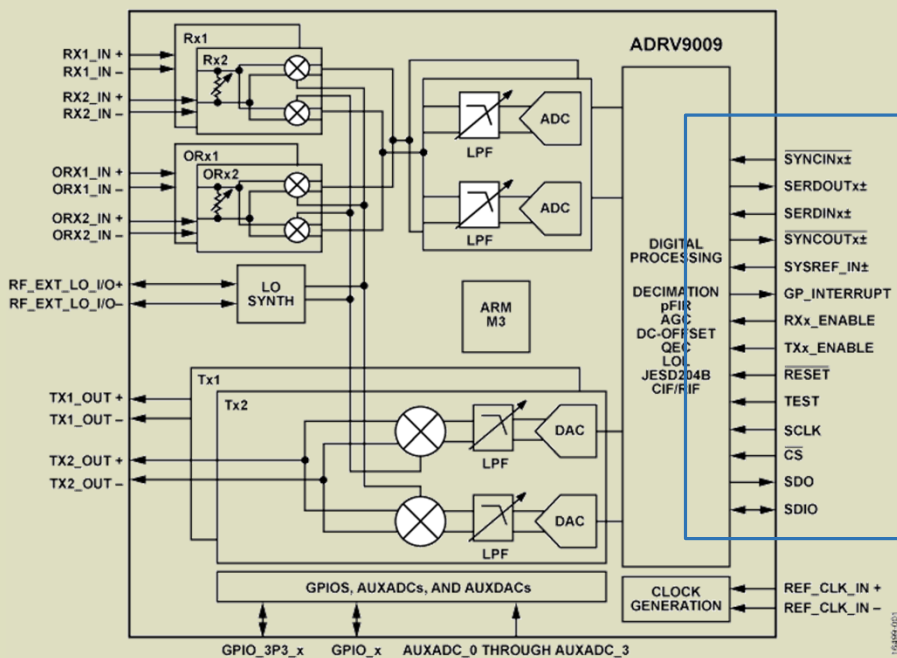
Equalizer simulation: Built-in CTLE/FFE/DFE/Bessel Thomson and other common digital equalizers in the data path.



The trend of technology convergence between RF test and high-speed digital signal test in emerging fields



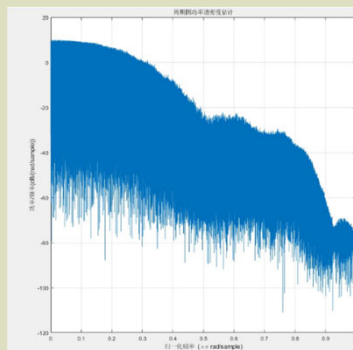
Example A: RF Transceiver



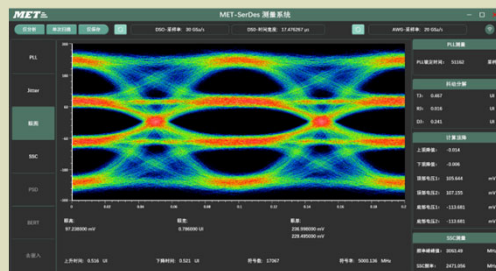
State of the art

- ☀ Data Rate per Lane: up to 32Gbps
- ☀ Tx FFE (Min.) : 9.5dB
- ☀ Rx CTLE (Min.) : 12dB
- ☀ Num. of Rx DFE taps (Min.) : 14
- ☀ Encoding : 8b/10b、64b/66b、64b/80b

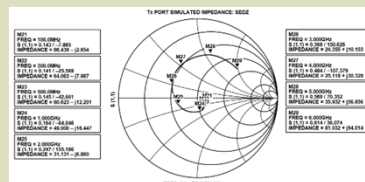
Example B: Automotive SerDes



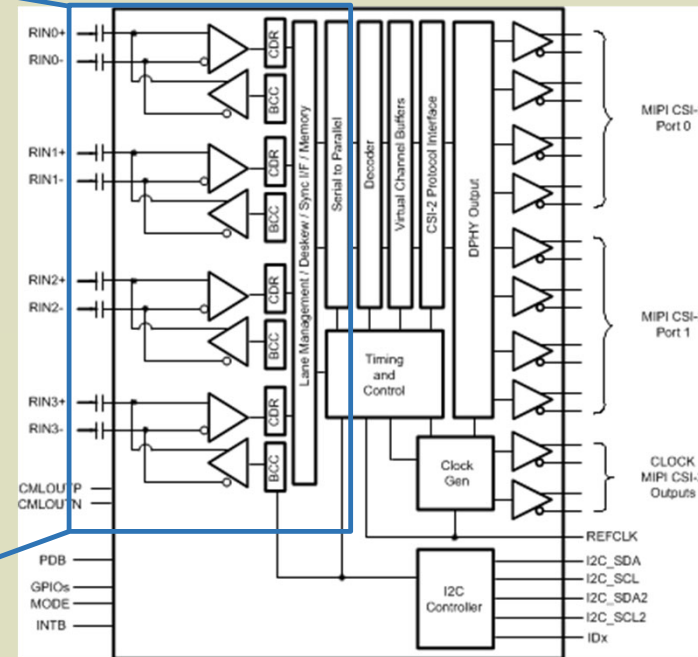
Frequency domain: DC-RF PSD



Time domain: PAM4 eye diagram



Port impedance



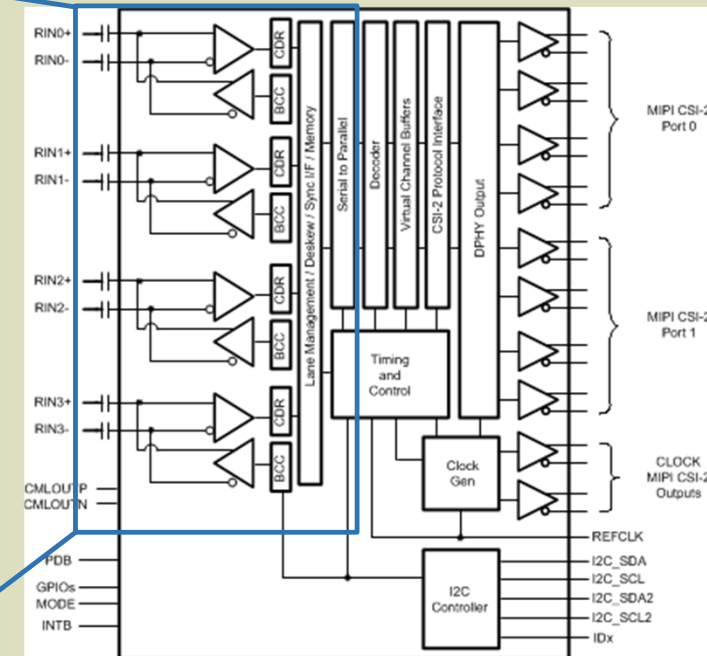
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Example B: Automotive SerDes

State of the art

Version	Player	Application	DataRate per Lane
GSML	Maxim	U.S.,China	2-12Gbps
FPD-link	TI	U.S.,China	2-6Gbps
AHDL	AIM	China	Gen2:6Gbps NG:13-15Gbps
Norelsys	HSMT	China	2-12.8Gbps
APIX	Inova	EU	12Gbps
GVIF	SONY	JP(TOYOTA)	~8.63Gbps
Clockless Link	ROHM		2.7Gbps
	ON Semiconductor		
	Rambus		
	Automotive SerDes Alliance		2/4/8/12/16Gbps
A-PHY	MIPI		16Gbps



Traditional digital tests and high-speed digital tests

Comparison of Loopback Test and PHY Test Capabilities

Test Categories	Symbol	Description	Loopback Test	PHY compliance test
Level Test	V_{OH}/V_{OL}	Output Level Voltage	✗	✓
	V_{IH}/V_{IL}	Input Level Voltage	✗	✓
	V_{IDTH}/V_{IDTL}	Differential Input Threshold	✗	✓
	V_{OD}	Differential Voltages	✗	✓
	V_{CM}	Common-Mode Voltages	✗	✓
Timing Test	T_{Rise}/T_{Fall}	Rise/Fall Time	✗	✓
	δV	Slew Rate	✗	✓
	T_{Skew}	Data-to-Clock Skew	✗	✓
Clock Test	PN	PLL Phase Noise	✗	✓
	t_{RJ}	PLL Random Jitter	✗	✓
	JTF	PLL Jitter Transfer	✗	✓
Tolerance	J_{tol}	Jitter Tolerance	✗	✓
		Error Injection by Ratio/by Index	✓	✓
		Frequency Offset	✗	✓
		Noise/Sine Injection	✗	✓
		Channel Injection	✗	✓
		Channel De-embedding	✗	✓
	SSC	Spread Spectrum Clocking	✗	✓
		Eye Diagram Tolerance	✗	✓
	EQ	Equalization	✗	✓
ΔV_{CMF}	Common-Mode Interference	✗	✓	
Measurement		CDR + Eye diagram Measurement	✗	✓
		Jitter Measurement	✗	✓
		Frequency Offset Measurement	✗	✓
		BER Measurement	✓	✓
		Voltage Droop Measurement	✗	✓

- In high-speed transmission scenarios:
- ★ Loopback tests alone cannot characterize the actual **interconnection** capability.
 - ★ Harsh scenarios require **stress tests** such as jitter-tolerance.
 - ★ Single defective device can cause more serious **quality cost** consequences.
 - ★ There is no accurate **quality control** without accurate test results.
 - ★ Adequate FT can **simplify** subsequent costly system-level testing.



The trend of technology convergence between RF test and high-speed digital signal test in emerging fields



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- **The convergence trend reflected in the technological evolution of the tester itself**
- Some typical cases



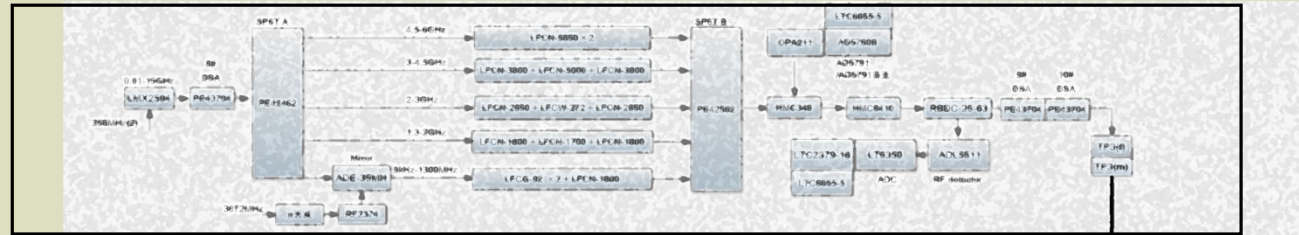
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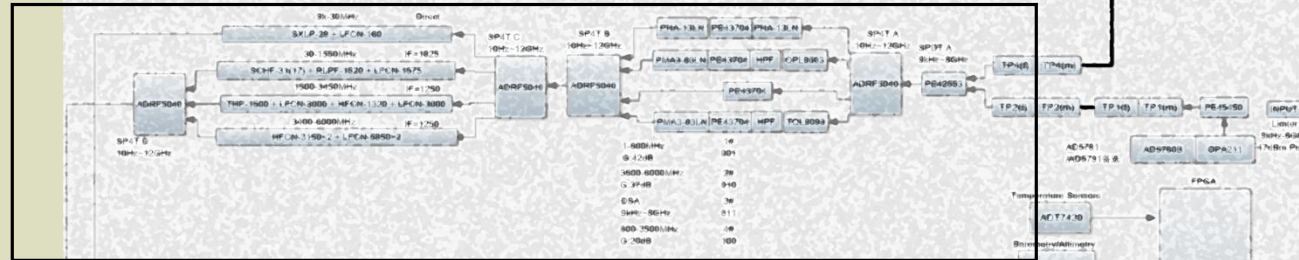
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Iteration of the tester architecture itself

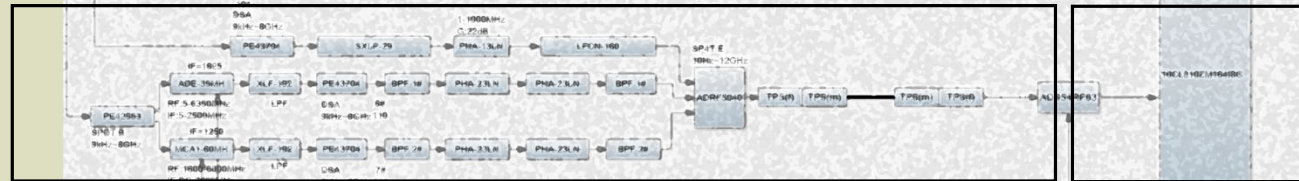
Reference source for calibration



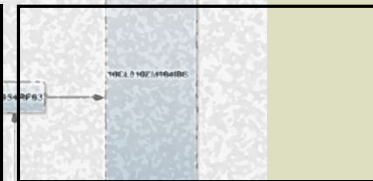
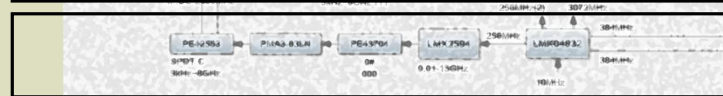
Pre-processing and frequency conversion



IF filter banks



Clock management



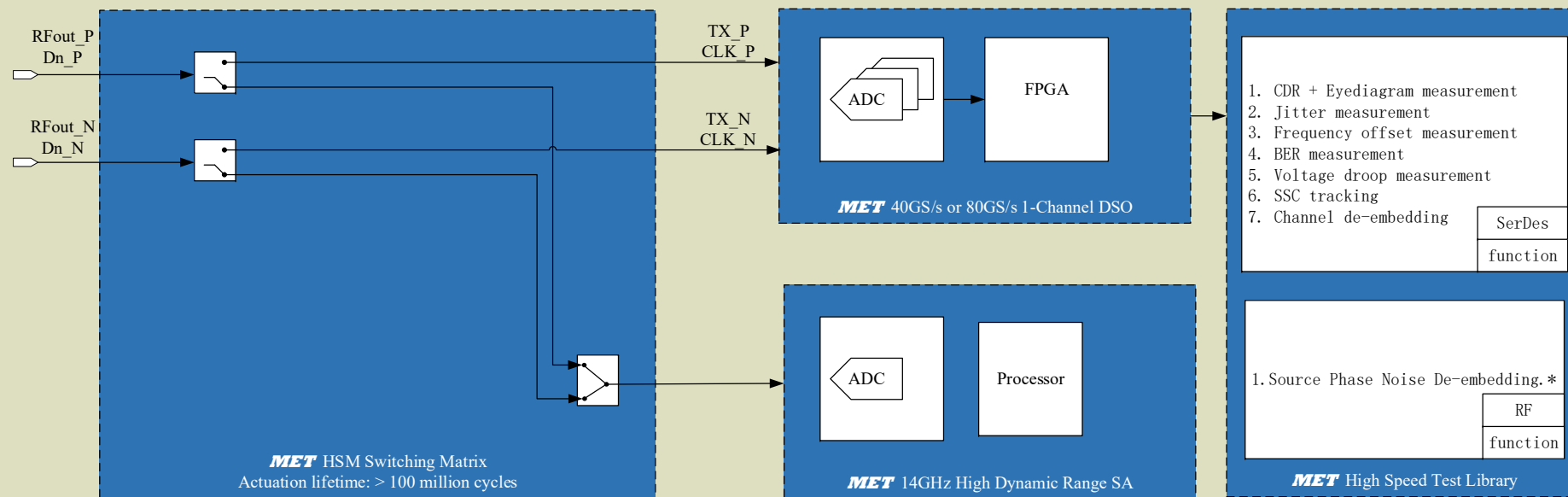
Architecture diagram of the 6 GHz vector signal analyzer of the previous PXIe productions



The trend of technology convergence between RF test and high-speed digital signal test in emerging fields
Iteration of the tester architecture itself



An iteration of the tester architecture on RF-AD/DA



Architecture diagram of the 8 GHz vector signal analyzer of the current PXIe productions

Iteration of the tester architecture itself

01 Simplified transceiver structure:

- Lower costs
- More stability
- Better test repeatability
- Longer calibration intervals

☀ Higher speed digital signal processing

☀ Requirement for System-level calibration

☀ Dynamic range is still insufficient

02 Lower noise figure and better signal quality

03 Higher bandwidth

04 More flexible features



The trend of technology convergence between RF test and high-speed digital signal test in emerging fields
Iteration of the tester architecture itself



Traditional digital tests and high-speed digital tests

Test Categories	Symbol	Description	Loopback Test	PHY compliance test
Level Test	V_{OH}/V_{OL}	Output Level Voltage	×	√
	V_{IH}/V_{IL}	Input Level Voltage	×	√
	V_{IDTH}/V_{IDTL}	Differential Input Threshold	×	√
	V_{OD}	Differential Voltages	×	√
	V_{CM}	Common-Mode Voltages	×	√
Timing Test	T_{Rise}/T_{Fall}	Rise/Fall Time	×	√
	δV	Slew Rate	×	√
	T_{Skew}	Data-to-Clock Skew	×	√
Clock Test	PN	PLL Phase Noise	×	√
	t_{RJ}	PLL Random Jitter	×	√
	JTF	PLL Jitter Transfer	×	√
Tolerance	J_{tol}	Jitter Tolerance	×	√
		Error Injection by Ratio/by Index	√	√
		Frequency Offset	×	√
		Noise/Sine Injection	×	√
		Channel Injection	×	√
		Channel De-embedding	×	√
	SSC	Spread Spectrum Clocking	×	√
		Eye Diagram Tolerance	×	√
	EQ	Equalization	×	√
	ΔV_{CMF}	Common-Mode Interference	×	√
Measurement		CDR + Eye diagram Measurement	×	√
		Jitter Measurement	×	√
		Frequency Offset Measurement	×	√
		BER Measurement	√	√
		Voltage Droop Measurement	×	√

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- Applications for RF and high-speed devices
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Products Serials Positioning

1. RF Integrated test/analyze System



Type-Code	Testing Capability			Applications
ARGOSY	<ul style="list-style-type: none"> S Parameter Linearity Noise Figure 	<ul style="list-style-type: none"> Phase Noise RF Timing Seq. Power Source 	<ul style="list-style-type: none"> Vector Signal Analysis temperature-related 	<ul style="list-style-type: none"> RF Semiconductor Device Screening RF Semiconductor Device Analysis
Type-Code	Testing Capability			Applications
CARAVAN	<ul style="list-style-type: none"> Transmitter Receiver 			<ul style="list-style-type: none"> Navigation Test Avionics Test Satellite Test Radar Test

2. RF Mass Production Test System



Type-Code	Applications
KNOX-F/M	RF front-end chips
KNOX-PA	RF PA/LNA
KNOX-PM	RF front-end module

3. High-speed Test System



Type-Code	Applications
Avatar-MS	ADC/DAC
Avatar-HS	<ul style="list-style-type: none"> SerDes PCIe/USB/NVME IEEE 802.3

4. Customized Test System



Products Serials Positioning



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Typical Products and Applications

ARGOSY-2000

Up to 40 GHz RF Integrated Tester & Analyzer



advantages

1

Complete **all** the required RF test in one tester without experienced engineer.



advantages

2

Reduce the test **costs** by adopting software defined hardware.



advantages

3

Accelerate the test **speed** by various featured test algorithm.



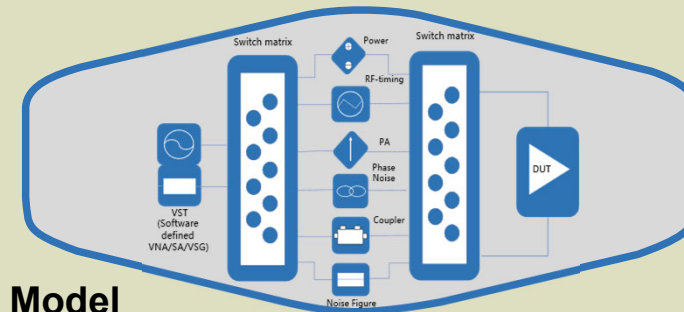
advantages

4

Achieve **high-end** test by innovative test model without expensive instrument.

- High isolation and long-life switch matrix
- Cold-Source NF measurement
- Model based S-parameter test
- Low phase noise measurement
- RF Timing Analysis and Correction
- Load correction for unmanned operation

Test Features



Test Model

Typical Products and Applications

Knox-FPM2000

Up to 20GHz Filter/DiFEM/PAMiD Tester



advantages

1

Predicts the packaged performance of the die under test.



advantages

2

Reduces the test **costs** by customized hardware.



advantages

3

Accelerates the test **speed** by AI based DUT model.



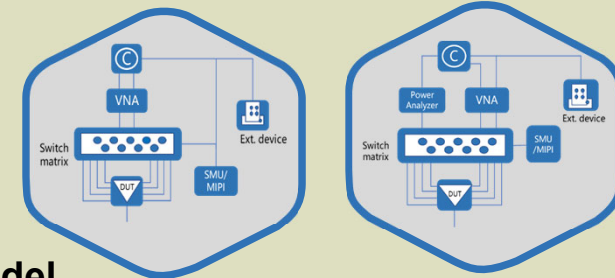
advantages

4

Dedicated to the test requirements of filter/DiFEM/PAMiD with low costs.

- Load reflection correction
- De-embedding or embedding
- High-speed test of S-parameter
- Economical scalar power test up to 50dBm
- All-in-one calibration

Test Features



Test Model

Typical Products and Applications

Knox-PA2000 PA/LNA Tester



advantages

1

High performance source with **pre-distortion**.



advantages

2

High output power VNA up to 50dBm.



advantages

3

High performance **cold source** noise figure test box.



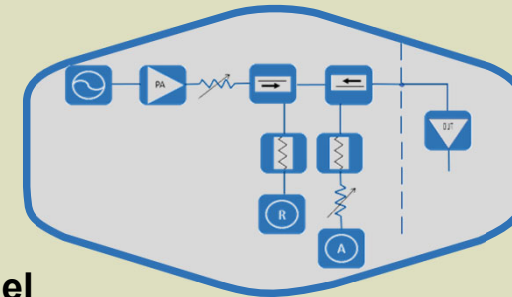
advantages

4

Dedicated to the test requirements of LNA/PA with low costs.

- RF source with digital pre-distortion
- Gamma power correction
- Configurable RF ports & multi-site parallel
- Economical scalar power test up to 50dBm
- High harmonic rejection test capability

Test Features



Test Model

Typical Products and Applications

Avatar-HS1000 High-speed Serial Link Tester



advantages

1

SerDes at-speed test up to **12.5GBaud**, PCIe 3.0, USB 3, JESD204B, MIPI, etc.



advantages

2

Full test function: Tx/Rx return loss, Tx eye/jitter, Rx eye/JTOL, Tx EQ, Rx EQ.



advantages

3

Very low inherent jitter, minimize bias in jitter measurement.



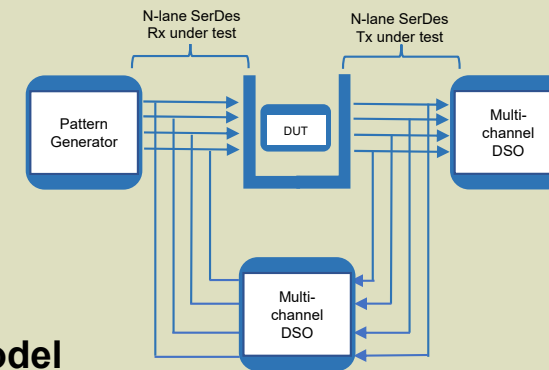
advantages

4

Small form factor, allow multiple Serdes lanes(≥ 16) being tested **simultaneously**.

- High-speed analog front-end with CDR
- NRZ/PAM4 format support
- Cable & fixture removal capability
- Built-in DSP for CTLE/FFE/DFE emulation

Test Features








Test Model

Typical Products and Applications

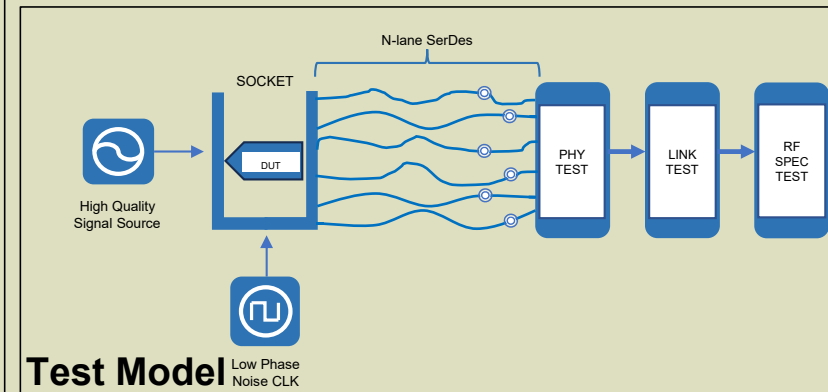
Avatar-MS1000

High-speed ADC/DAC Tester

-  **advantages**
1 Advanced digital **pre-distortion** (DPD) technique deliver high quality RF source
-  **advantages**
2 **Instrument-grade** clocking capability minimizes systematic errors
-  **advantages**
3 Patented source **de-embedding** method to reach true DUT performance
-  **advantages**
4 **Serdes PHY and LINK** test capabilities enable JESD204B compliance test
-  **advantages**
5 **All-in-one**, dedicated solution eliminates need for expensive desktop instruments

- RF source with digital pre-distortion
- Low jitter clock with jitter injection
- De-embedded analog front end
- Independent SerDes test capability

Test Features



Special Part for Today



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