Test Hardware Signal Integrity Design for SOC with IP-Specific Impedance

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NXP Semiconductor

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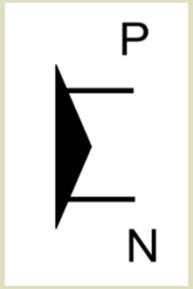
SI-Design for SOC with IP Specific Impedance

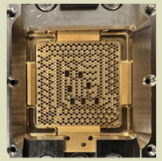
Agenda

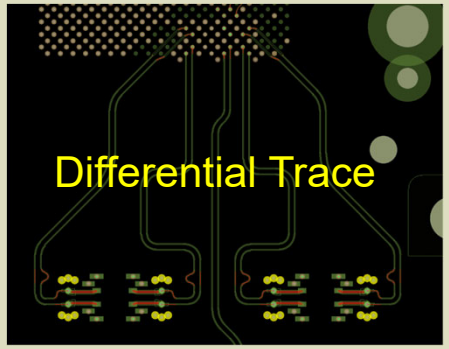
- SOC I/Os with unique impedance requirements
- SERDES signal path segments
- Modeling, Simulation Results Table
- Signal path SI Integration Process
  - Transmission line performance of each segments
  - Complication and variability of test socket
- DDR SI modeling
- Dominant entities of the transmission line integration
- Summary and Conclusion

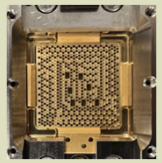
SOC IP's with Specific Differential Impedance

TX IBIS Model
- Mod-T
- Mod-I
- Mod-L









RX IBIS Model
- Mod-T
- Mod-I
- Mod-L

TX, RX Impedance IP Specific (Package Electrical Rules for IMX95 and Tunis)
- Standard I/Os 100 Ohms, Diff 50 Ohms SE,
- USB 90 Ohms, (5G+, 10G+ Data Rate)
- PCIE/Ethernet 85 Ohms, (16G,28G, 32G Data Rate+)
- DDR 80 Ohms Diff, 40 Ohms SE, (4G, 8G+ Data Rate+); Not on Bias-Tee Loop back

TX Impedance Thevenin Equivalent circuit Math=VNA TDR Profile **RX Impedance**

S-Parameters

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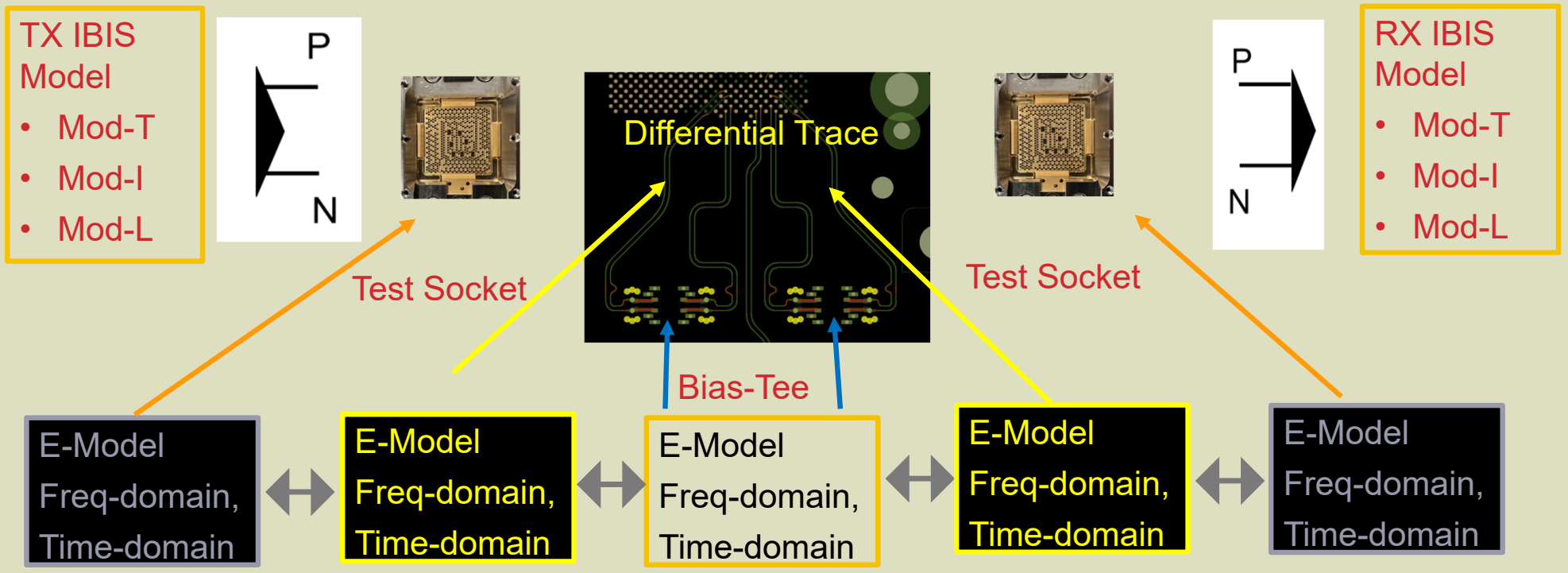


SI-Design for SOC with IP Specific Impedance

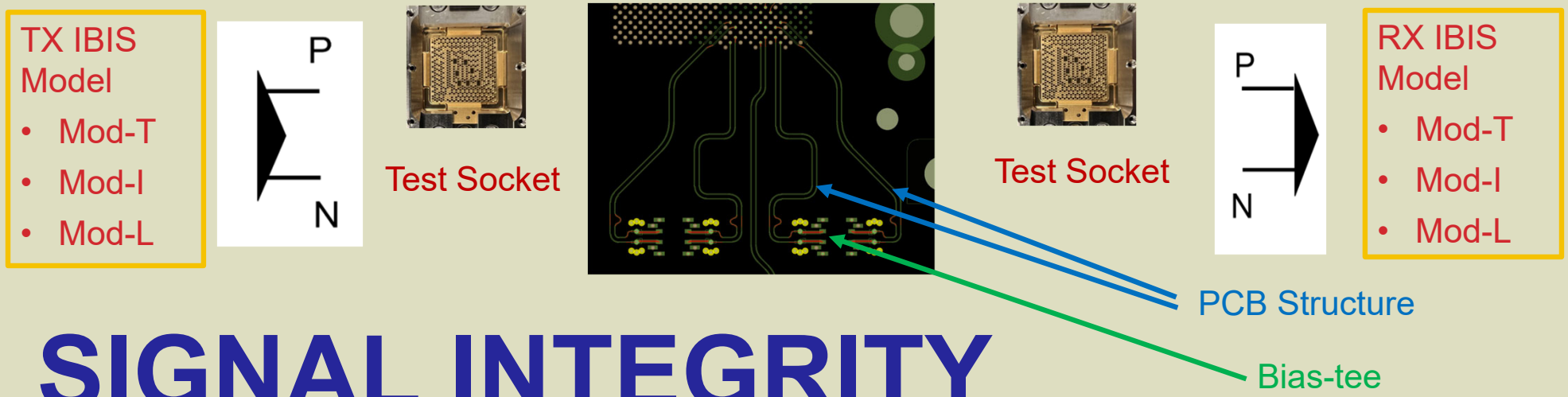
IP Specific Impedance

- The requirement includes Package Design Rules.
- Requires PCB Structures(pads, vias, traces) to comply with IP specific Impedance.
- Requires Test Socket to comply with IP specific Impedance
- Requires board component to match with IP specific impedance

IP modeling, simulation results with PRBS-31 for the complete signal path (Ip-package-socket-pcb)

IP Type	Model	Impedance (Diff) (Specifications)	Data Rate	Modeled, Simulated best results Impedance range (Ohms)	Point of Measurements
PCIE	T	85 Ohms	16G	(85Ohms)- 90 Ohms	External
DDR	T	80 Ohms(40 Ohms SE)	8G	90 Ohms to 100 Ohms	Internal
Ethernet	I	85 Ohms	16G	85 Ohms to (90 Ohms)	External
PCIE	I	85 Ohms	10G	85 Ohms to (90 Ohms)	External
USB3	I	90 Ohms	10G	90 Ohms	External
DDR	I	80 Ohms (40 Ohms SE)	4G	90 Ohms to 100 Ohms	Internal
PCIE	L	100 Ohms	28/32G	90 Ohms to 100 Ohms	External

Over 160 circuit permutations modeled



SIGNAL INTEGRITY INTEGRATION BY SEGMENT

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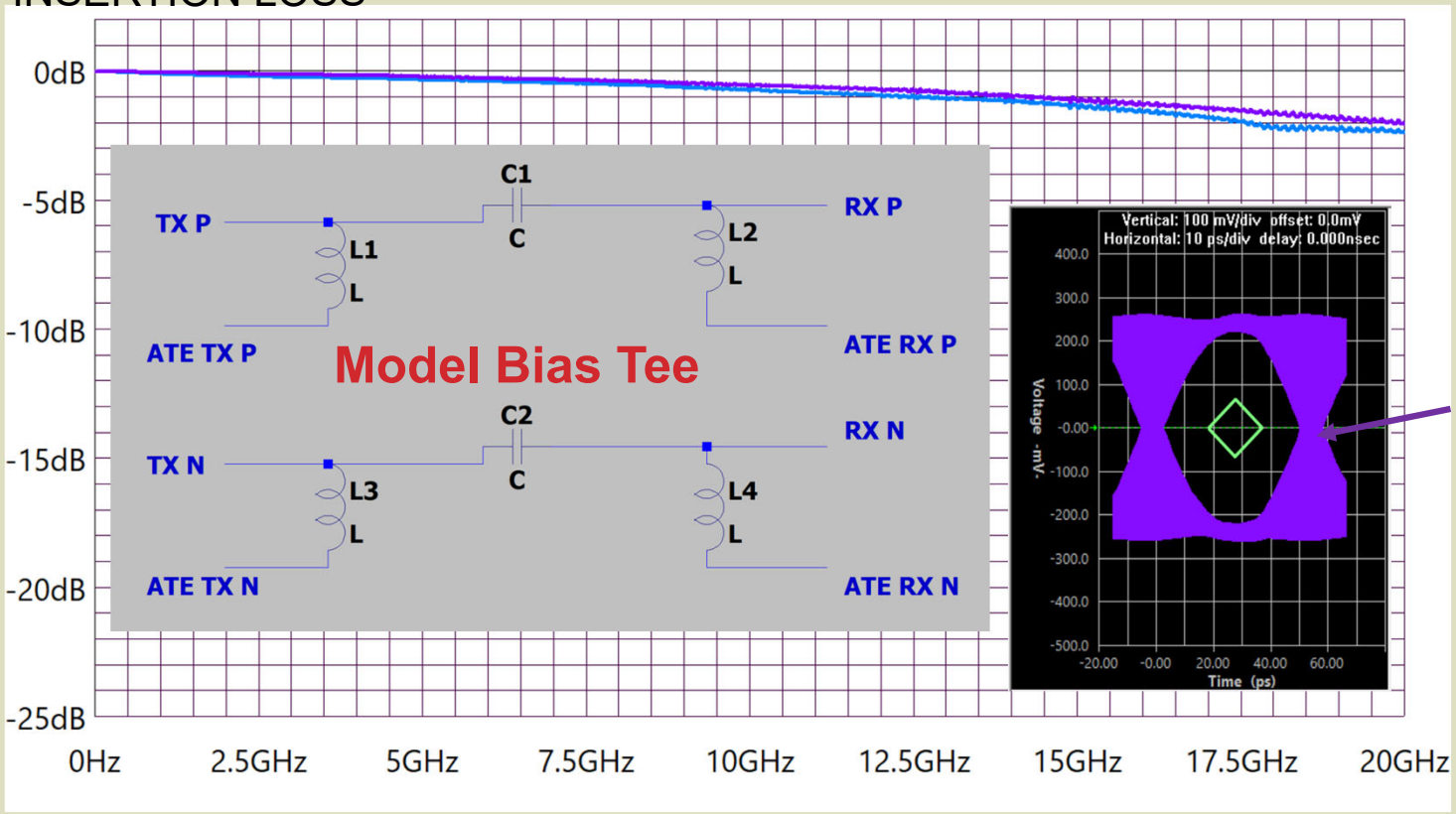
Model:Bias-Tee V3

S2D1 INSERTION LOSS

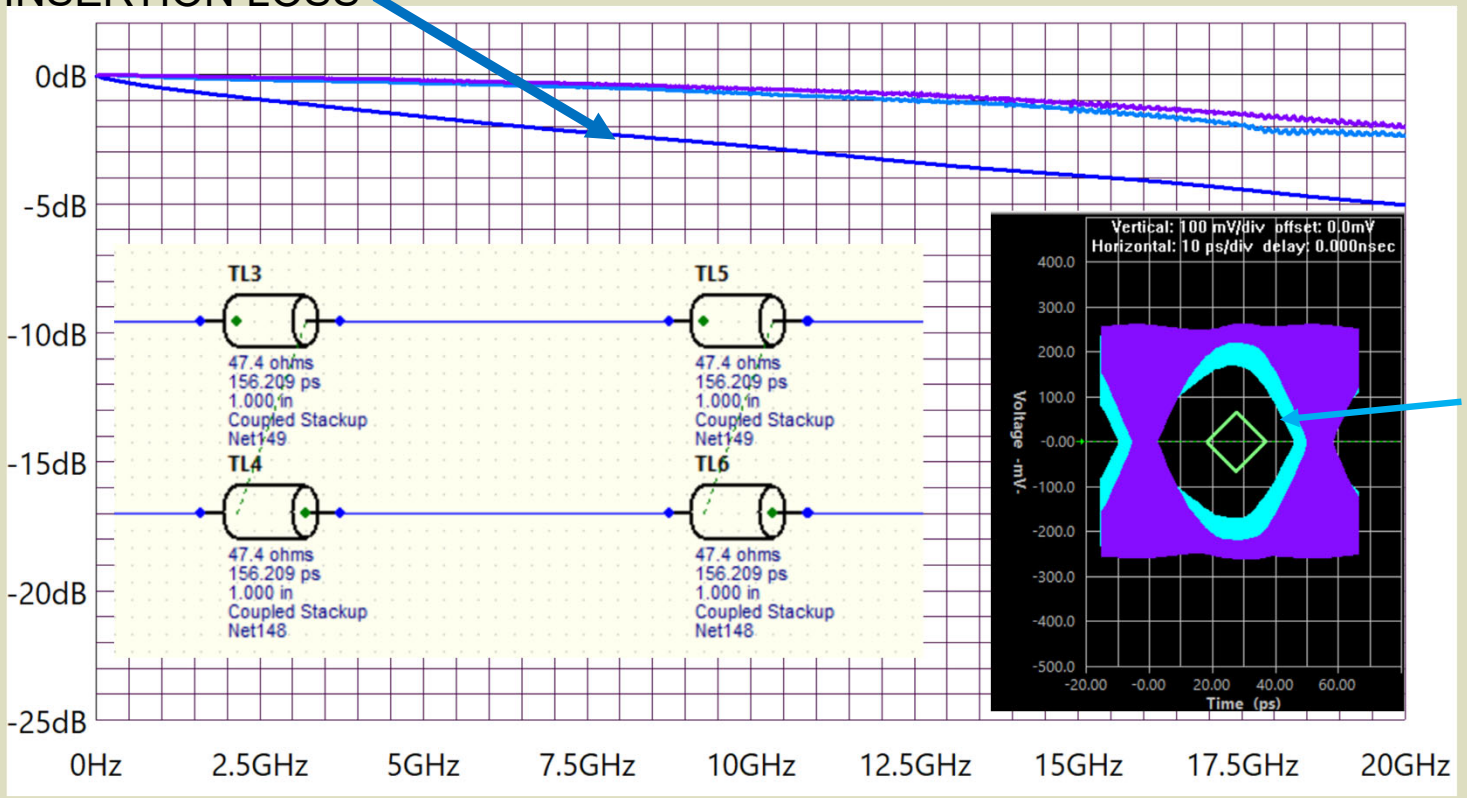


Model: Differential Trace 2x 1 inch 3 mils wide

S2D1 INSERTION LOSS

IBIS Model

- Model-I



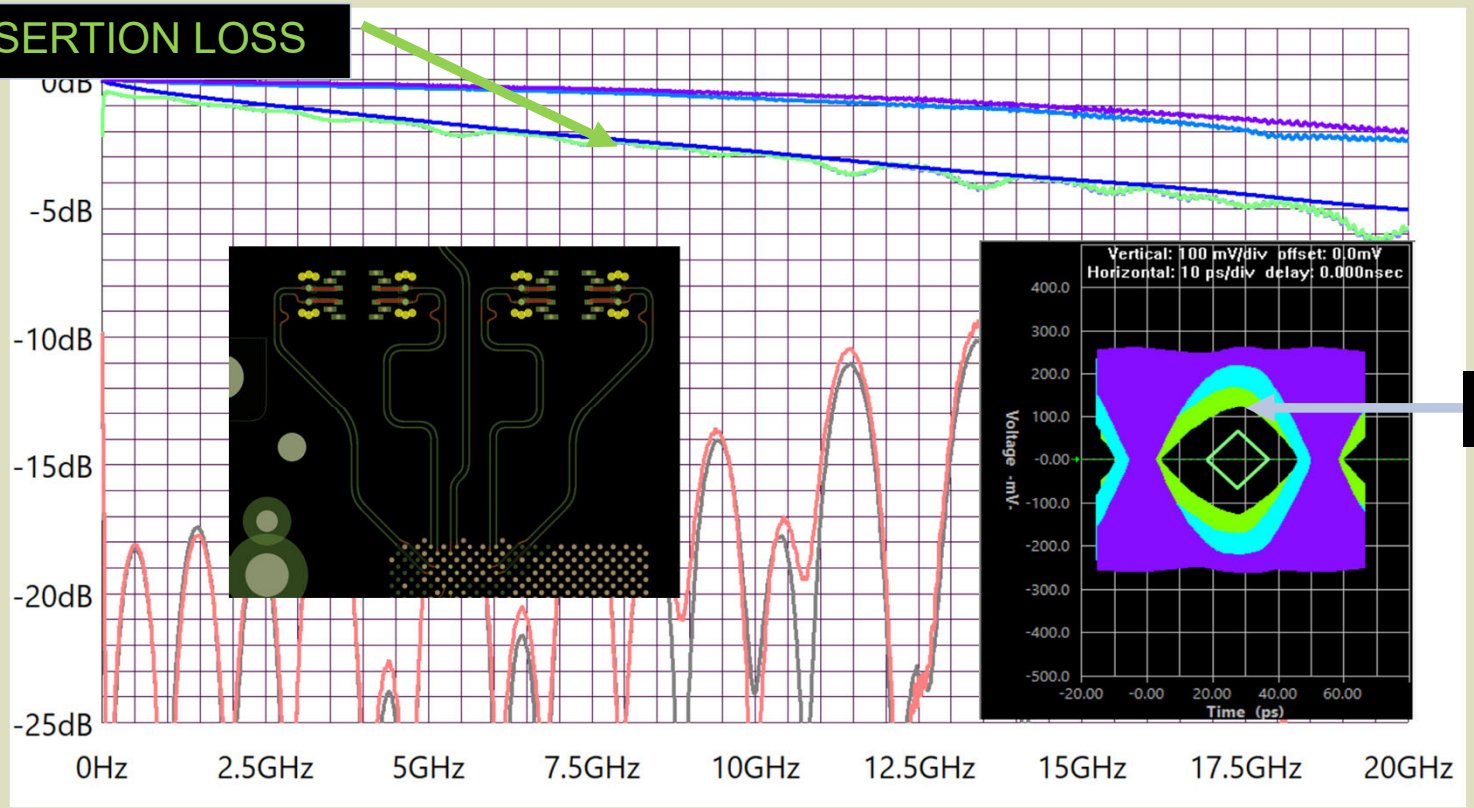
Date Eye

Model: Bias-Tee V3 & Differential Trace 2x 1 inch

S2D1 INSERTION LOSS

IBIS Model

- Model-I



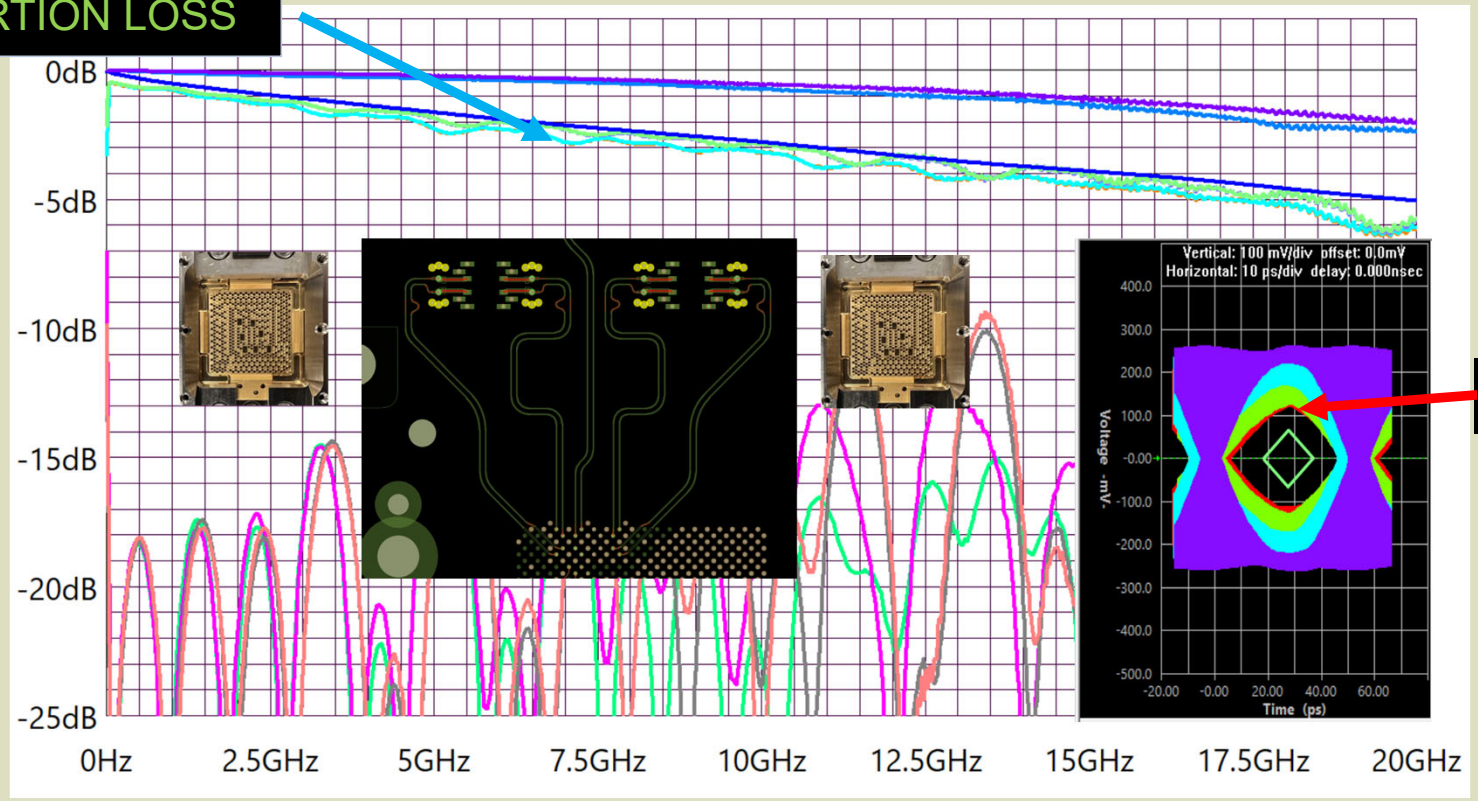
Date Eye

Model:Bias-Tee V3, Differential Trace(2x), Test Socket (2x)

S2D1 INSERTION LOSS

IBIS Model

- Model-I



Date Eye

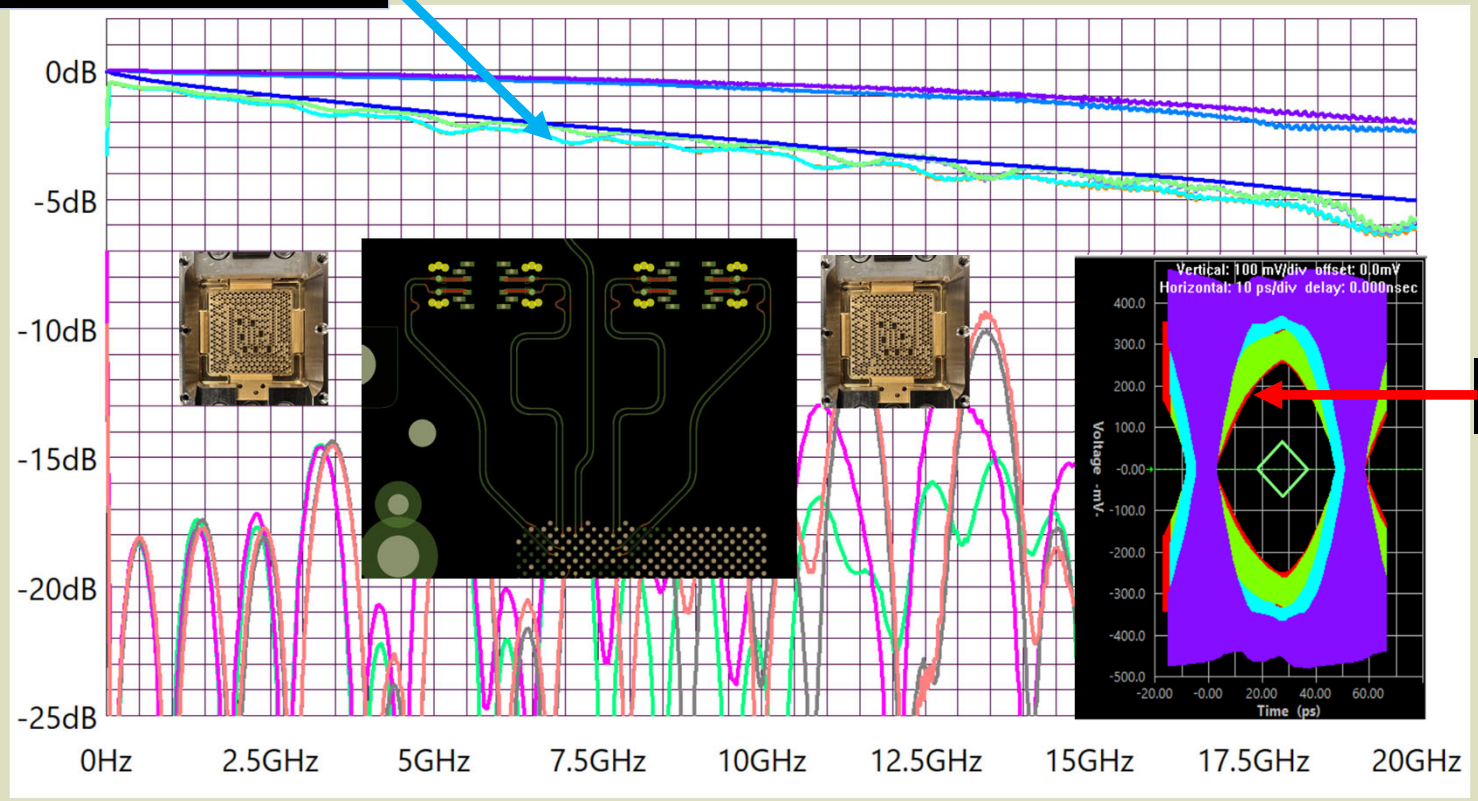
SIGNAL INTEGRITY SAME HARDWARE DIFFERENT I/O IBIS MODELS

Model:Bias-Tee V4, Differential Trace(2x), Test Socket (2x)

S2D1 INSERTION LOSS

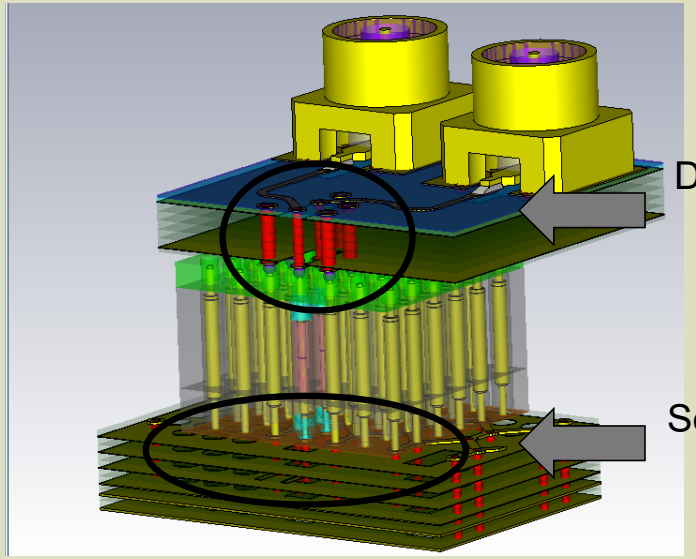
IBIS Model

- Model-T



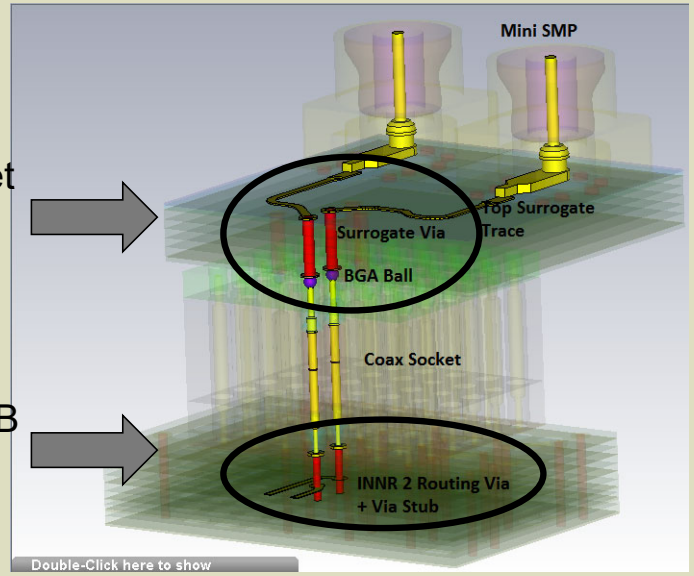
COMPLICATIONS, INTRICACIES OF TEST SOCKET DESIGN AND INTEGRATION

Bits 2018 Slide on Test Socket & Transisions



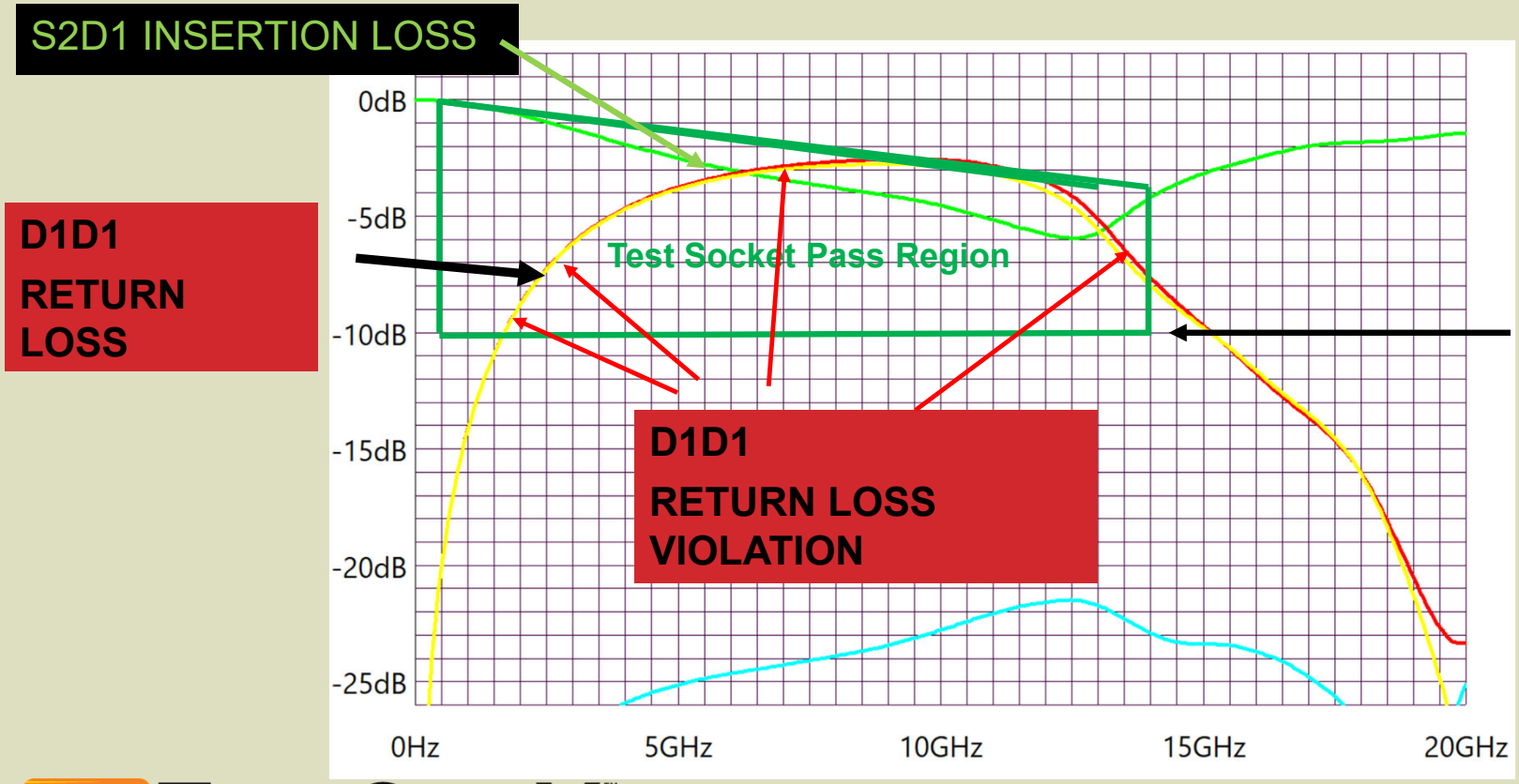
DUT to Socket transition

Socket to PCB transition

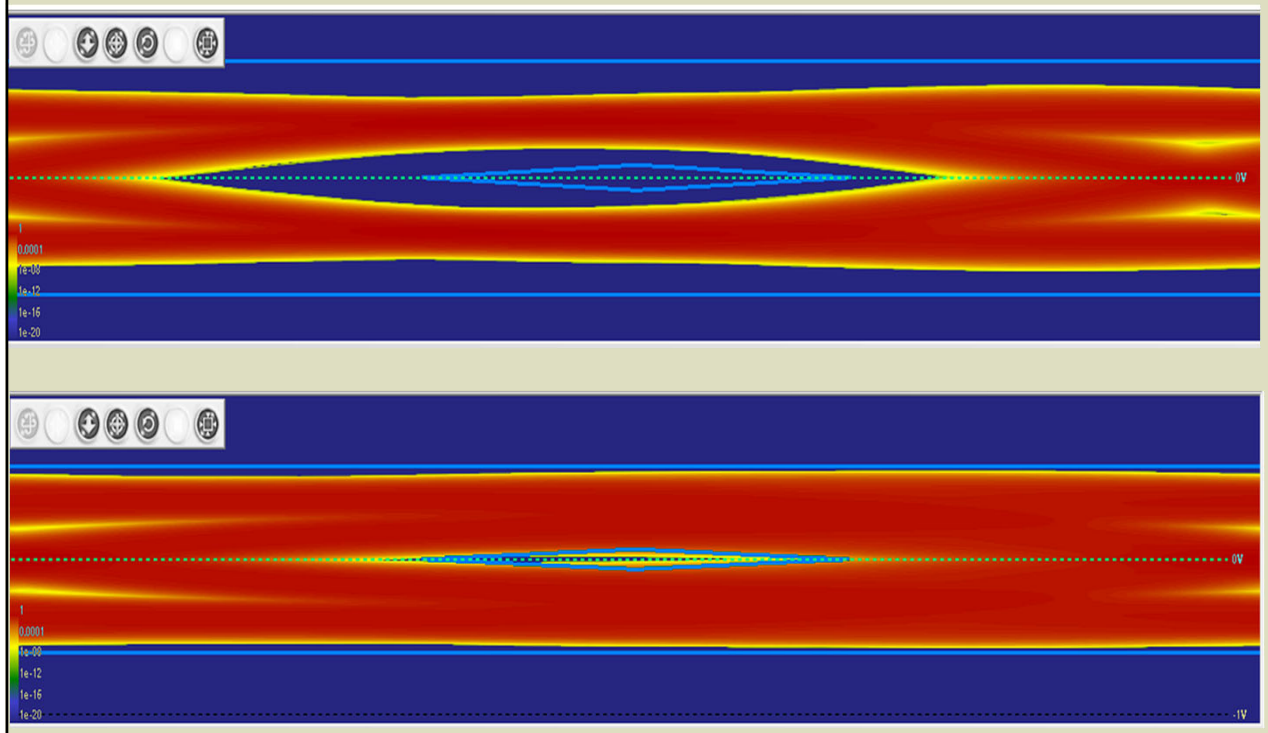


At 28+ Gbps, transition to/from socket as important as socket!!!

Low performance test socket (High return loss) Poorly conceived design (Assumed!)



Low performance test socket (High return loss) PRBS-31 @18G Data Eye



W/ Equalization

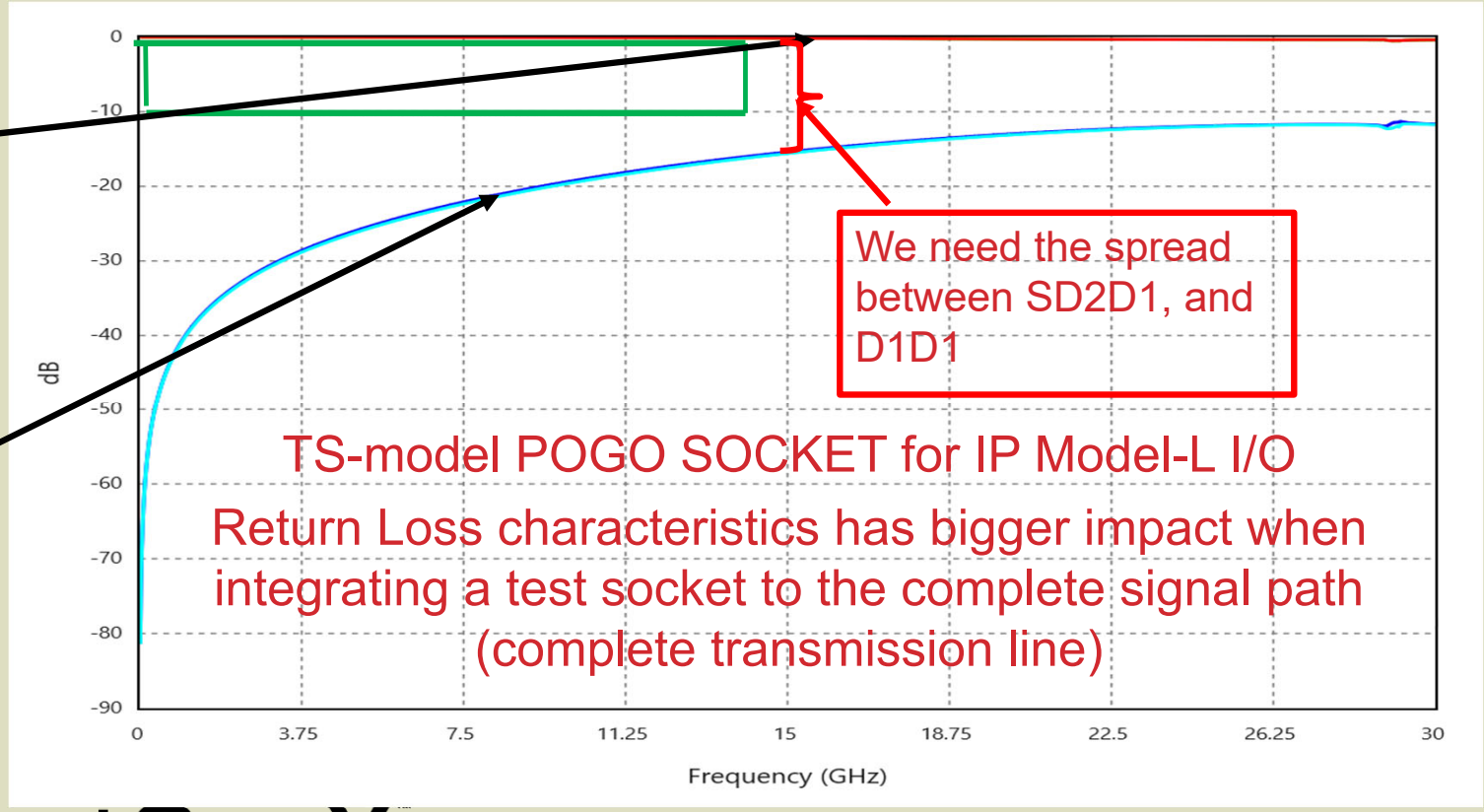
Barely Pass

Eyes Wide Shut

W/O Equalization

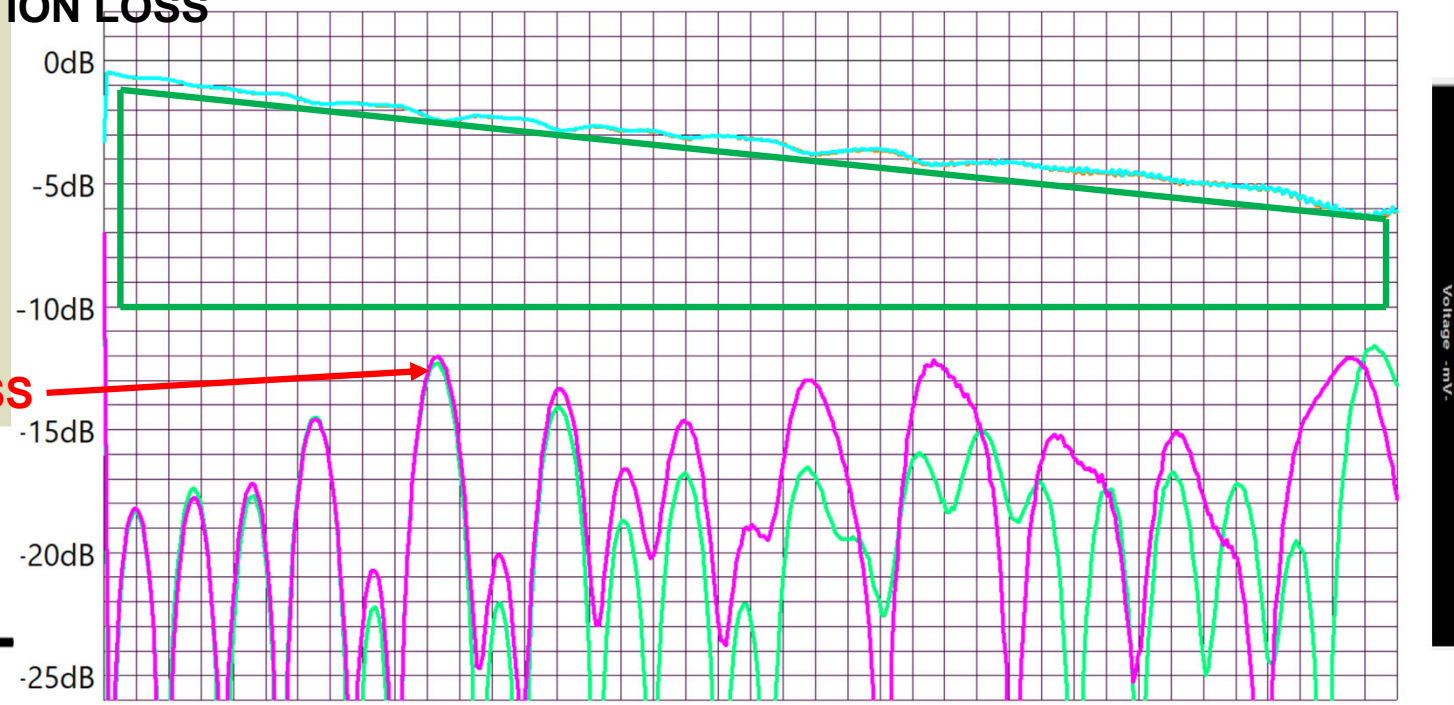
Performance requirements for test socket & specific IP IBIS Model

HW PASS Region



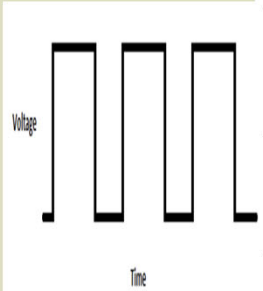
PRBS-31, 28G , High Performance Test Socket

S2D1 INSERTION LOSS

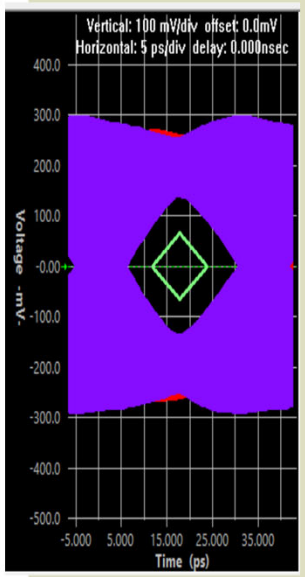


D1D1

RETURN LOSS



Input Signal



Date Eye

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Test Socket Summary, Comments:

- There is a general lack of knowledge on the impact of test socket on the transmission line segment.
- The impact of contact-zones and its integration to the transmission line hardware is another less understood process in SI design.
- Test socket degrades as a function of insertion count. Design budget to account from Cycle=0 to Cycle=Replacement

WHAT WE LEARNED FROM MODELING AND SIMULATION RESULTS

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Data-Eye Assessment @ 90 Ohms acceptable not to compromise yield budget. Not ideal but manufacturable solutions.

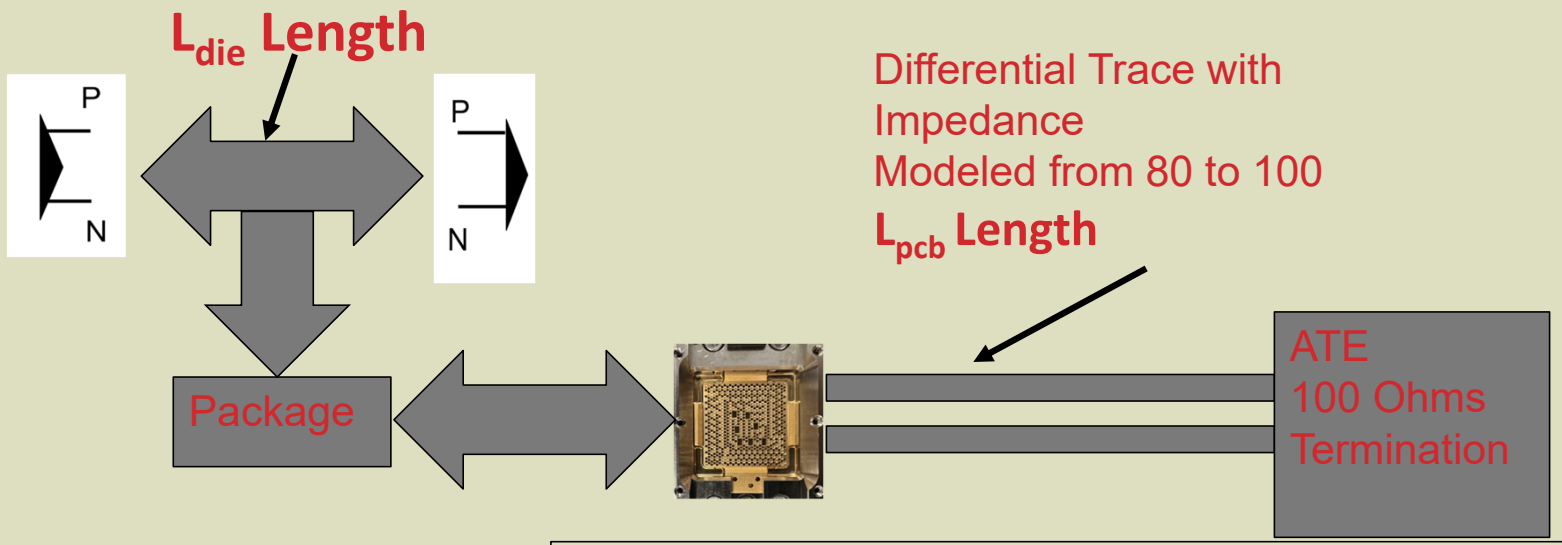
SI-Design for SOC with IP Specific Impedance

Modeling and simulation results:

- Compliance to IP specific impedance provided the best results. Specifically for short-wavelength IPS.
- Model-T PCIE simulations indicated best performance at 90 Ohms vs the 85 Ohms recommended.
- Slower data rate or longer wavelength IPs can be made to operate at acceptable deviation with tolerable consequences (e.g. Model-I Ethernet from 85 Ohms to 90 Ohms)

SIMPLIFIED DDR MODELING AND SIMULATION

DDR Simplified Model Representation In-die measurement (Model-Simulation)



L_{pcb} >>>> L_{die}

At signal wavelength of interest, The DDR data eye is dominated by the Impedance of the PCB trace, at 90 Ohms to 100 Ohms.

Critical Entities of Test Hardware Transmission Line Performance(Aside from geometries & dielectric)

- IP Specific IBIS Models as a function of
  - I/O Standards, Technology
  - IP Provider
  - Geometry
- As function of wavelength discontinuity needs to be contained and managed for the entire signal path segment.
- Transition Zones between signal segments are common source of discontinuity.

Conclusion, Recommendation

- IP Specific Impedance on a single SOC is here and future of NXP Products.
- One size fits all impedance is less applicable with increasing data-rate (shorter wavelength)
- IP I/O Models as function of technology, IP providers have profound impact on the data-eye after transmission line.
- Test Socket design and SI-Integration is an area for improvement.
- This new requirement in SI design is best application for AI-Design (Next TestConx). Specifically for circuit optimization.

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