Differential Probe Design to Support PCB Characterization to 40 GHz for 112G PAM4 Applications

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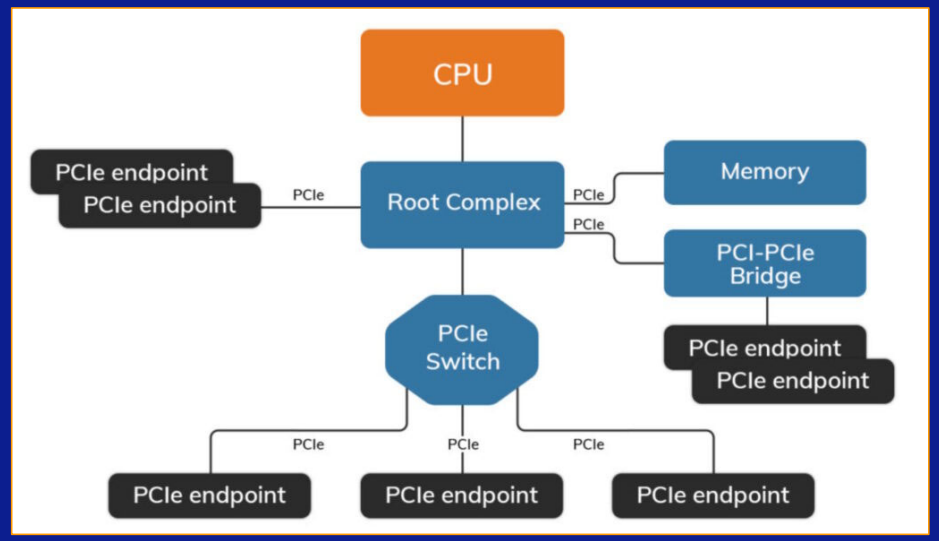
PTSL

Introduction

- Summary
  - GbE market forecast
  - PCIe market forecast
- GSSG 0.5 mm pitch probe
- Simulation
- Measurement methods
- Analysis
- Conclusion

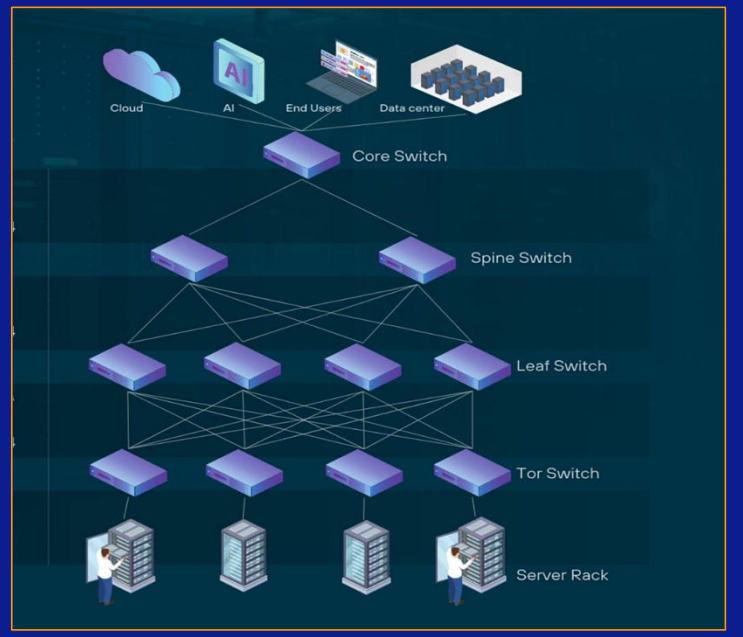
Background

- Data center expansion and artificial intelligence are driving data bus developments
  - GbE for server to server communication
  - PCIe for NPU/CPU to peripheral communication



PCIe Connection Drawing

Source: https://www.microcontrollertips.com/whats-a-pcie-root-complex/

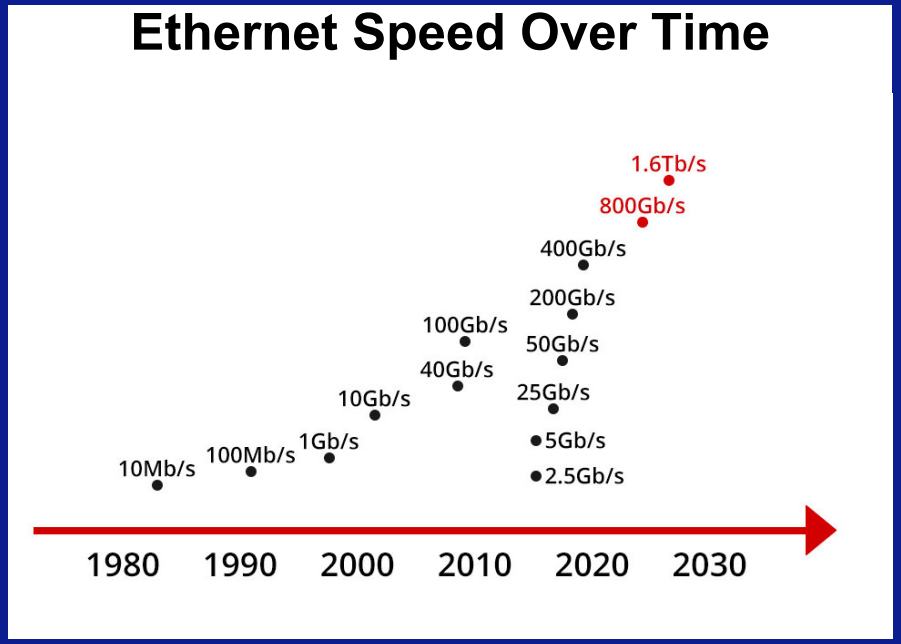


Full Data Center Communication

Source: https://www.atoptechnology.com/greening-the-future-atop-ultra-efficient-and-eco-friendly-400g-800g-data-center-solutions/

GbE Market Data Rate Requirements

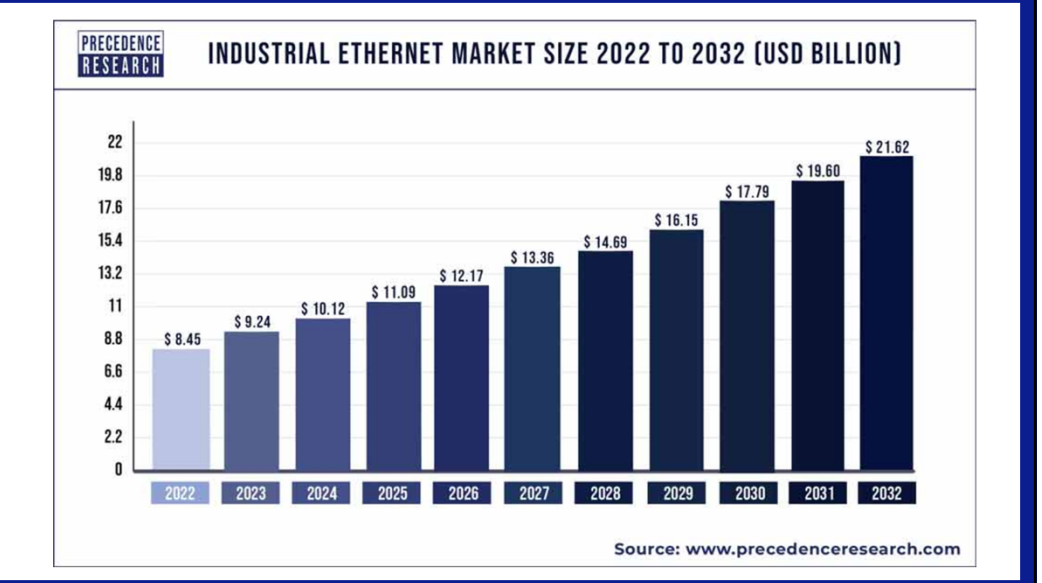
- Digital data rates increase at least 2x with each new generation.
- Data centers, AI, and 5G, are major drivers.



Source: https://community.fs.com/article/800g-16t-ethernet-innovations-and-challenges.html

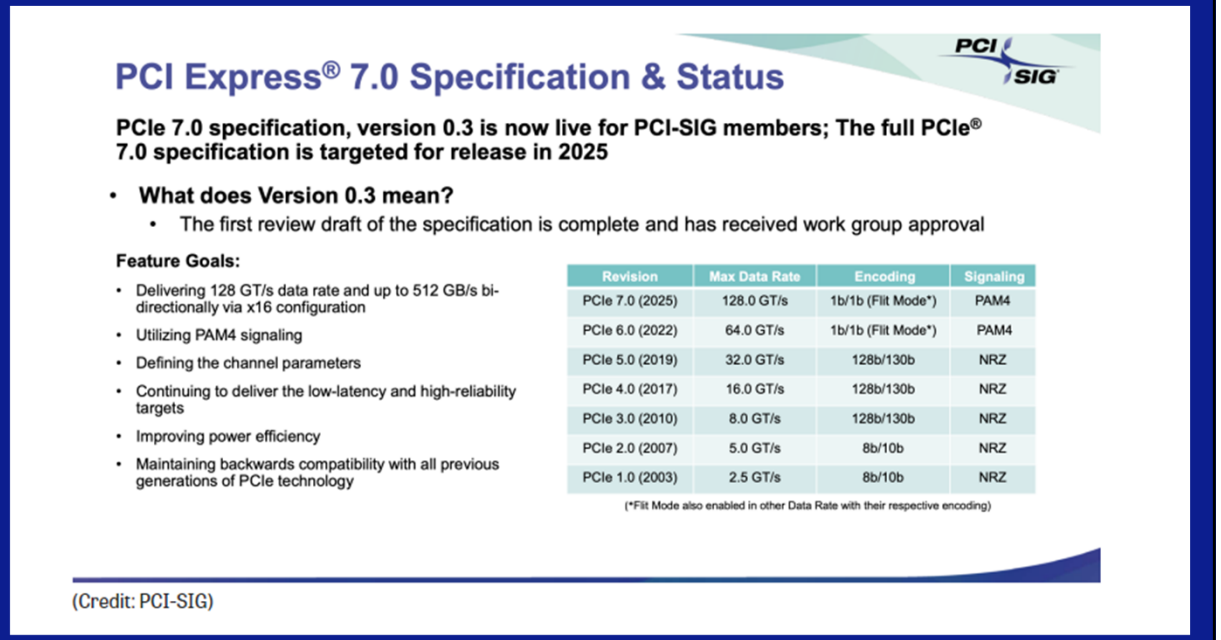
Ethernet Market Growth

- The growth of Ethernet will go from about $8.5B in 2022, to more than double by 2032 to $21B annually
- This will be driven by expansion as well as movement to faster standards



PCIe Market Speed Requirements

- Increased speed of data per lane will require continued improvement in test
- The ability to measure the performance will be stressed to reach higher bandwidths to confirm device performance
  - PCIe 6.0: 64Gbps @ 16GHz
  - PCIe 7.0: 128Gbps @ 32GHz



PCI Express® 7.0 Specification & Status

PCIe 7.0 specification, version 0.3 is now live for PCI-SIG members; The full PCIe® 7.0 specification is targeted for release in 2025

- **What does Version 0.3 mean?**
  - The first review draft of the specification is complete and has received work group approval

Feature Goals:

- Delivering 128 GT/s data rate and up to 512 GB/s bi-directionally via x16 configuration
- Utilizing PAM4 signaling
- Defining the channel parameters
- Continuing to deliver the low-latency and high-reliability targets
- Improving power efficiency
- Maintaining backwards compatibility with all previous generations of PCIe technology

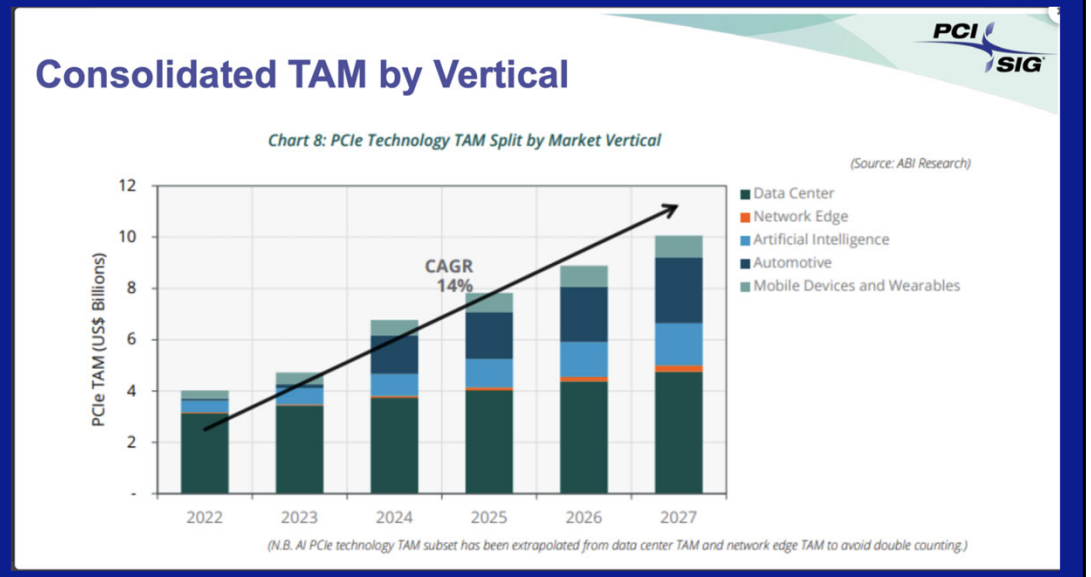
Revision	Max Data Rate	Encoding	Signaling
PCIe 7.0 (2025)	128.0 GT/s	1b/1b (Flit Mode*)	PAM4
PCIe 6.0 (2022)	64.0 GT/s	1b/1b (Flit Mode*)	PAM4
PCIe 5.0 (2019)	32.0 GT/s	128b/130b	NRZ
PCIe 4.0 (2017)	16.0 GT/s	128b/130b	NRZ
PCIe 3.0 (2010)	8.0 GT/s	128b/130b	NRZ
PCIe 2.0 (2007)	5.0 GT/s	8b/10b	NRZ
PCIe 1.0 (2003)	2.5 GT/s	8b/10b	NRZ

(*Flit Mode also enabled in other Data Rate with their respective encoding)

(Credit: PCI-SIG)

PCIe Market Growth

- PCIe is expecting a CAGR of 14% between 2022 and 2027
- This growth will require characterization of 85 Ω differential channels at 32 GHz



- Source: https://www.hpcwire.com/2023/06/13/pcie-market-to-hit-50b-pcie-7-0-v-0-3-now-available/

GbE and PCIe

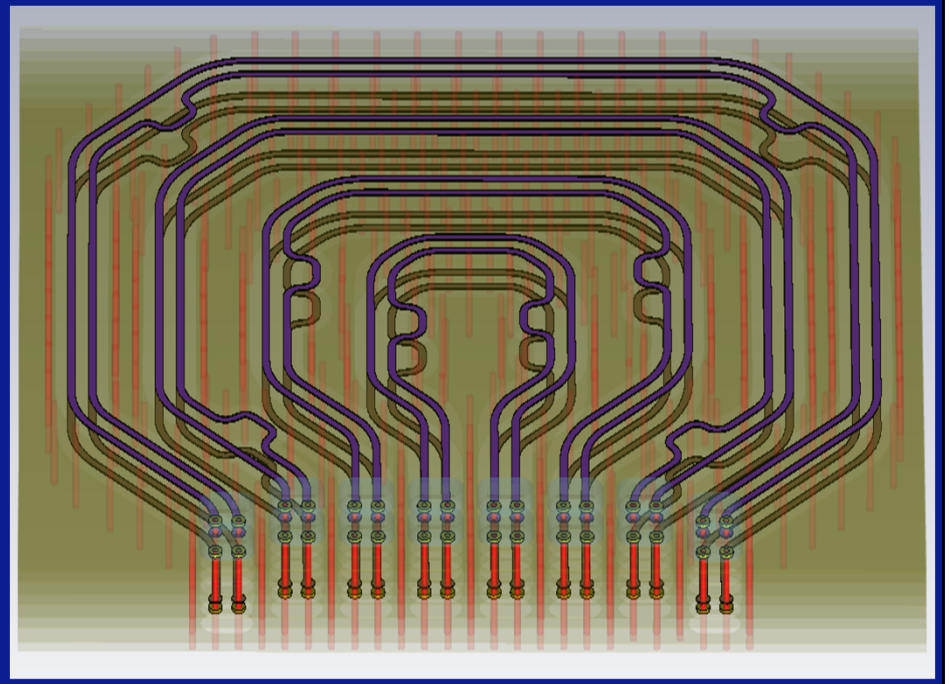
- *Due to Gigabit Ethernet and PCIe being the primary data bus for data centers & AI networks, the ability to measure and confirm the data channels at these high speeds at PCB-scale pitches is requiring investigation into how to characterize the PCB*

Gigabit Ethernet and PCI Express

Generation	GbE	PCIe 7.0
Standards and consortiums	IEEE 802.3 Ethernet Alliance	PCI-SIG
Data rate	112 Gbps PAM4	128 Gbps PAM4
Baud	56 GBd	64 GBd
Nyquist frequency	28 GHz	32 GHz
Common uses	Chip to chip, chip to fiber optic connections	Chip to chip, chip to peripherals

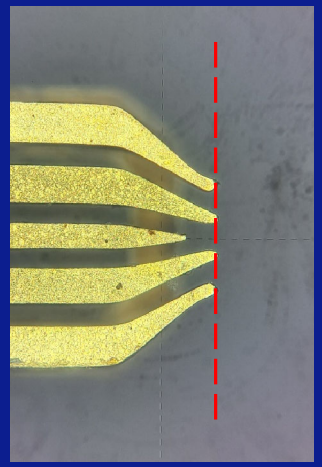
112 Gbps PAM4 External Loopback Routing

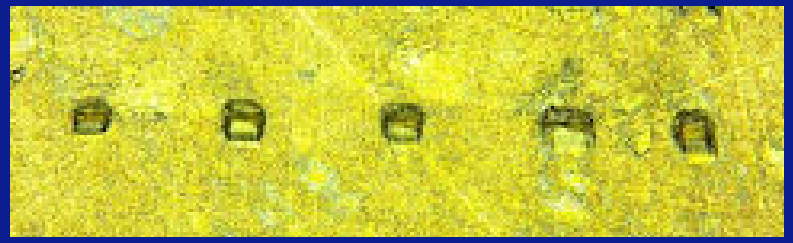
- Differential DUT vias are 0.5mm pitch in this example
- Differential probes are available in GSSG up to 1.0 mm pitch for PCB and space transformer applications, but many of the probes on the market struggle with these pitches at the frequencies required



Probe Tip Alignment and Scrub Marks

- Probes must show excellent scrub marks, as well as good tip alignment for use on PCBs
- In manual setups, probe mark size and uniformity are used to qualitatively determine overdrive and planarity





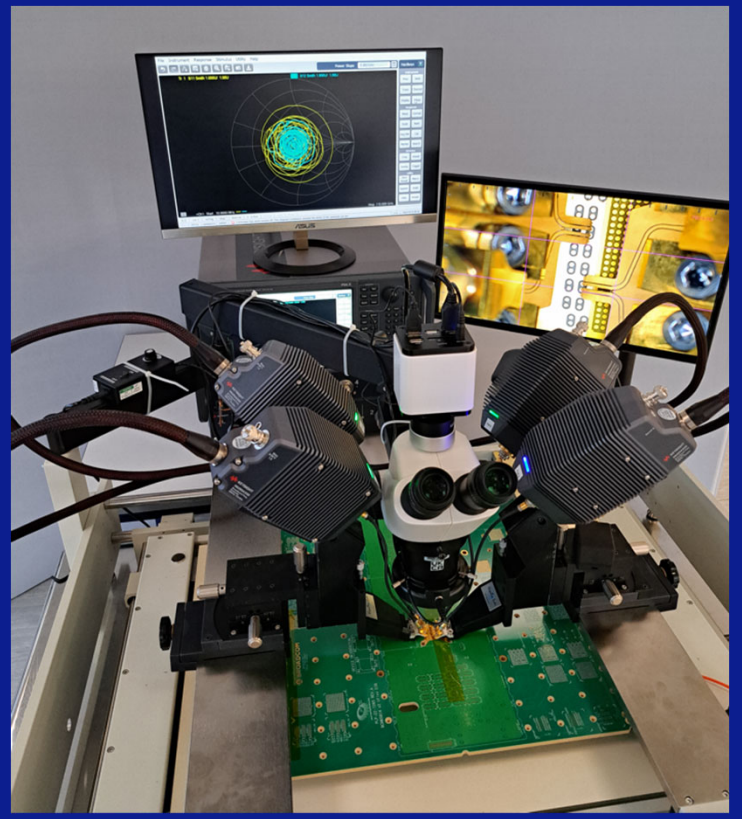
GSGSG 125 µm pitch scrub marks at 40 µm overdrive

Wide Pitch S-Parameters

- S-parameter performance
  - Since the device is operating in differential mode, we are presenting the S-parameters as SDD (differential), not single ended S-parameters
  - Customer specification for this board is to function at 28 GHz with BW to 40 GHz

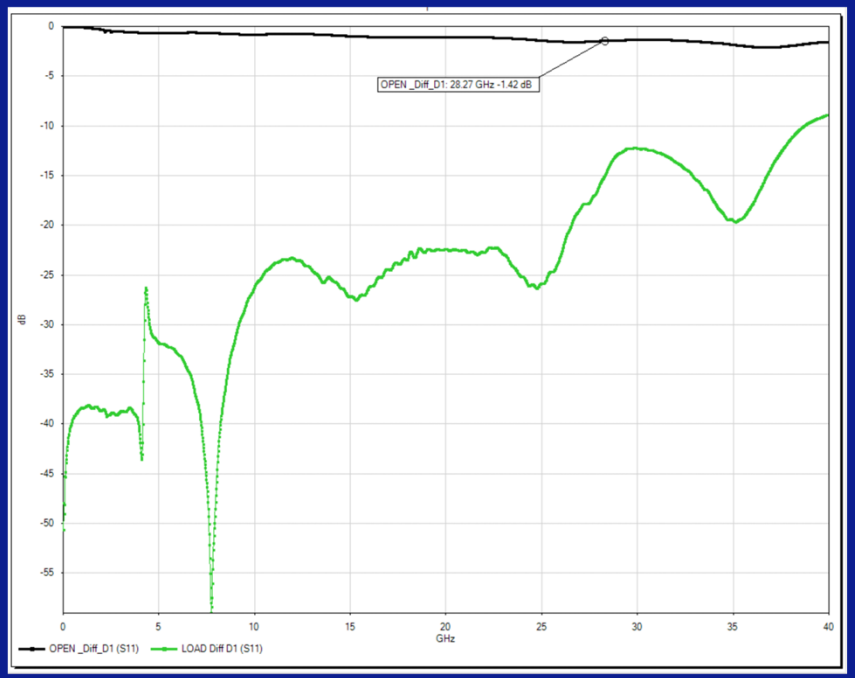
VNA Characterization Setup

- The test setup consists of:
  - Keysight 110 GHz, 4-port PNA-X
  - 110 GHz mechanical calibration kit from Keysight
  - Manual probe station
  - Two GSSG 0.5 mm pitch probes

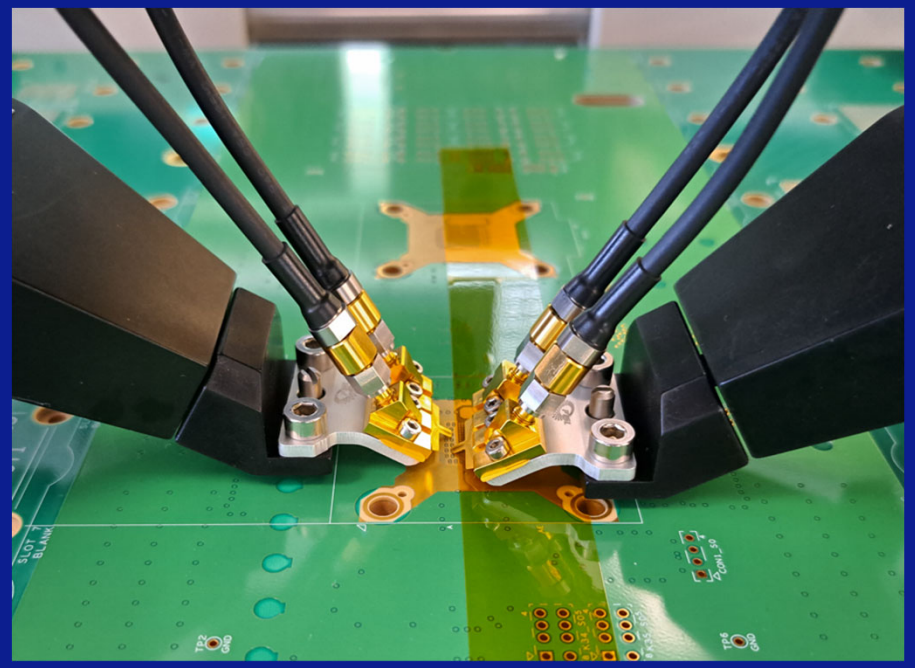


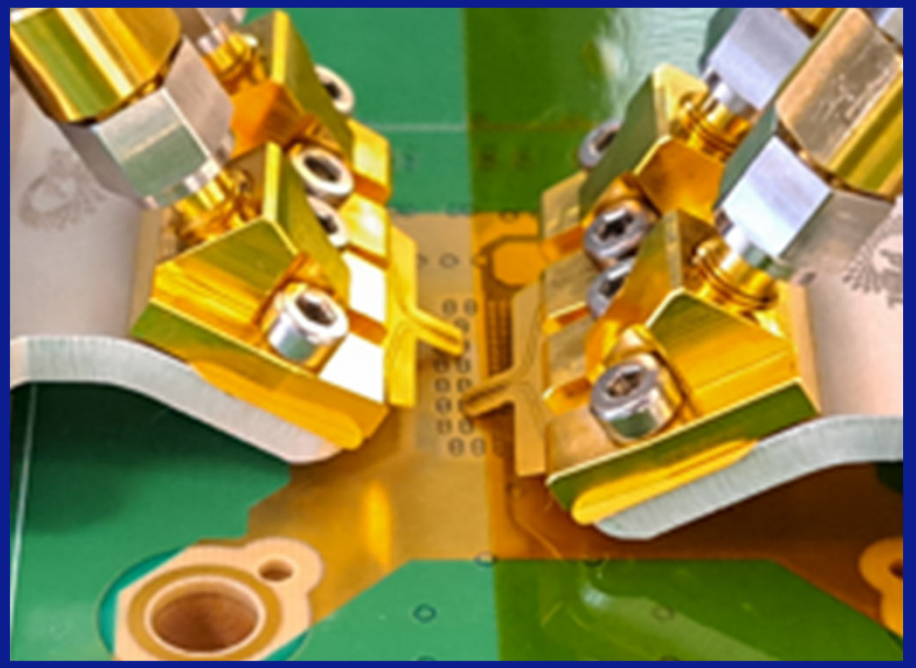
500 µm GSSG Probe VNA Measurements

- 500 µm GSSG probe measured performance on an open and load
- S11 into open = -1.42 dB @ 28 GHz
  - This is roughly double the insertion loss (S21) of the probe
- S11 into load = -12 to -15 dB @ 28-32 GHz
  - This shows the RL of the probe



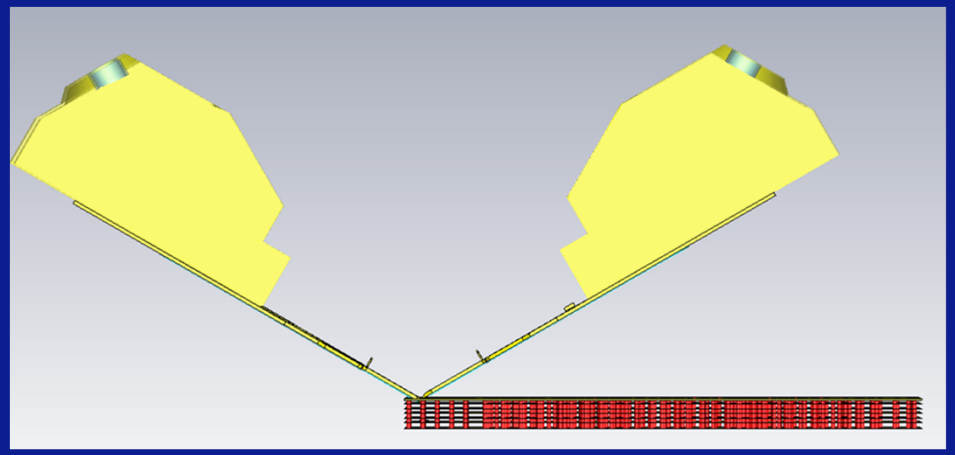
Two 500 µm GSSG Probes for True 4-port Differential Measurements

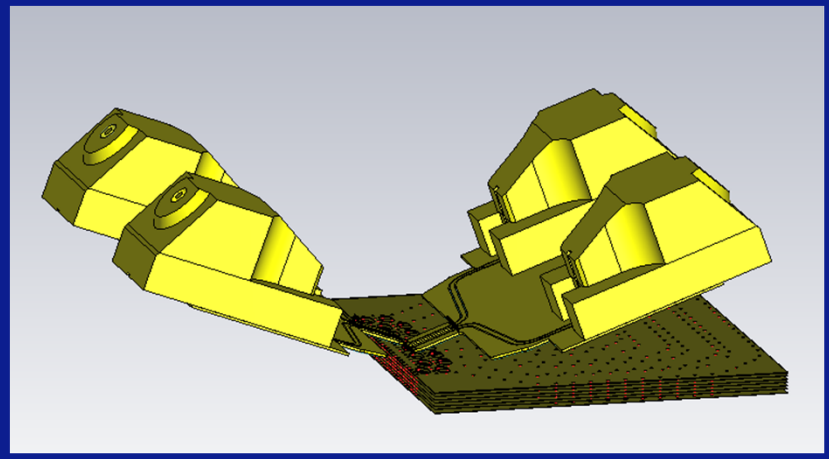




Simulation of the Loopback

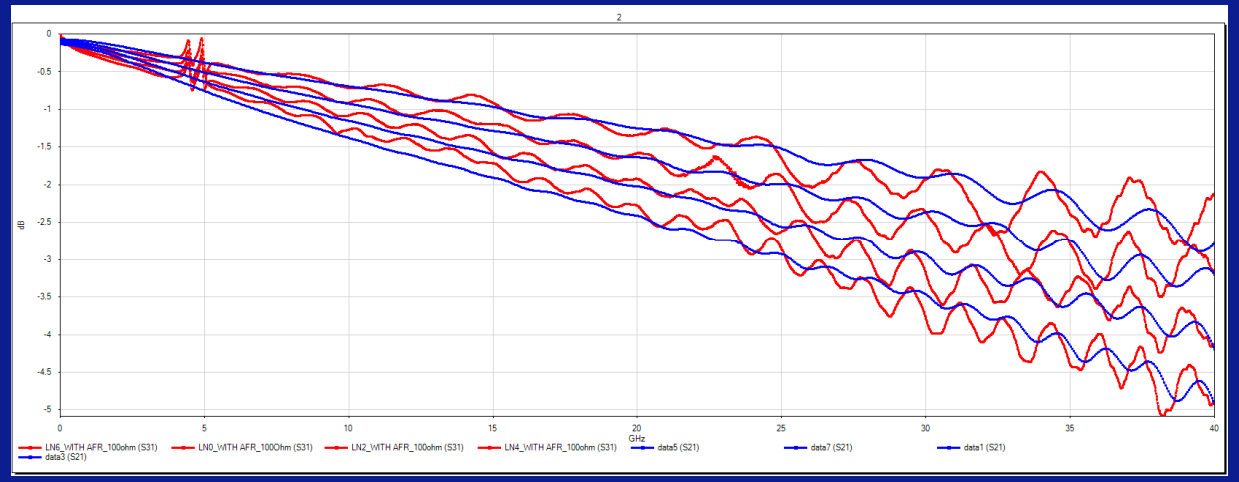
EM 3D simulation is done in CST Studio to simulate the performance of the DUT with the probe in the simulation model to compare with measurements





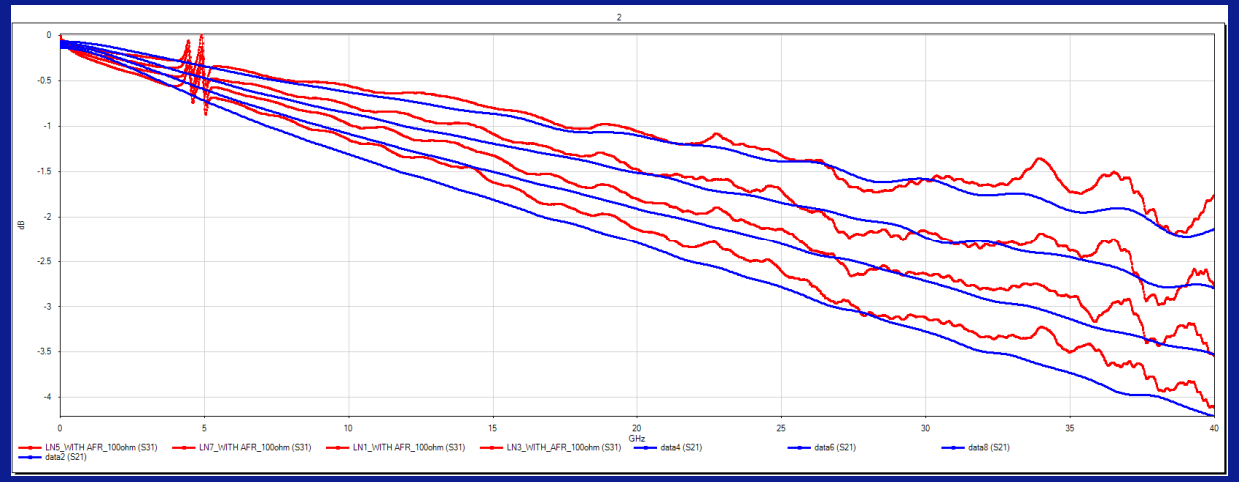
PCB Loopback Insertion Loss – Layer 2 Traces

- Measurements with simulation results of Sdd21
  - The simulations correlate really well up to 40 GHz with measurements
  - Measurements made with 500 µm pitch GSSG probes



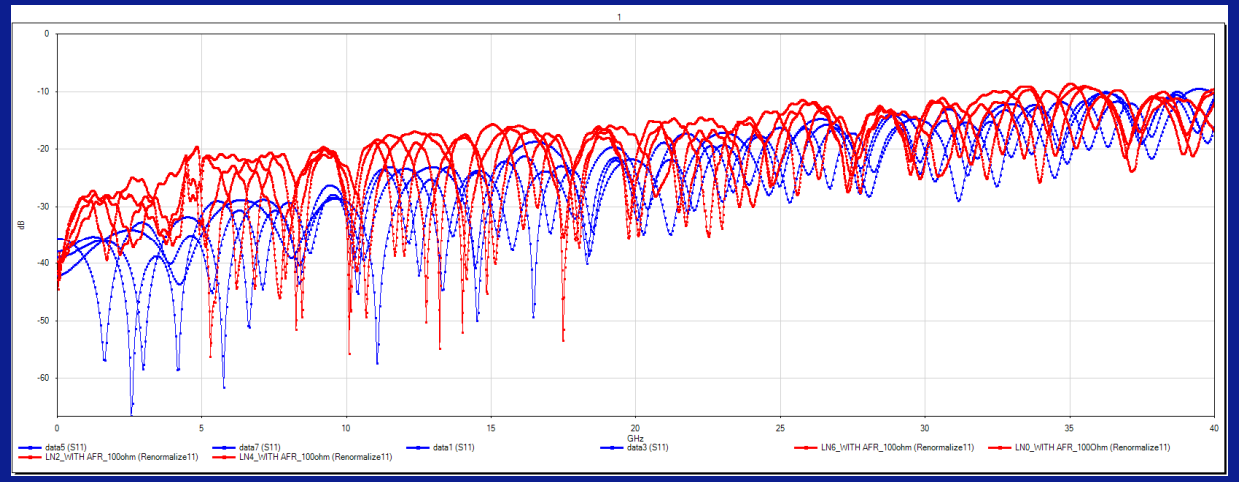
PCB Loopback Insertion Loss – Layer 5 Traces

- Measurements with simulation results of Sdd21
- The simulations correlate really well up to 40 GHz with measurements
  - Measurements made with 500 µm pitch GSSG probes



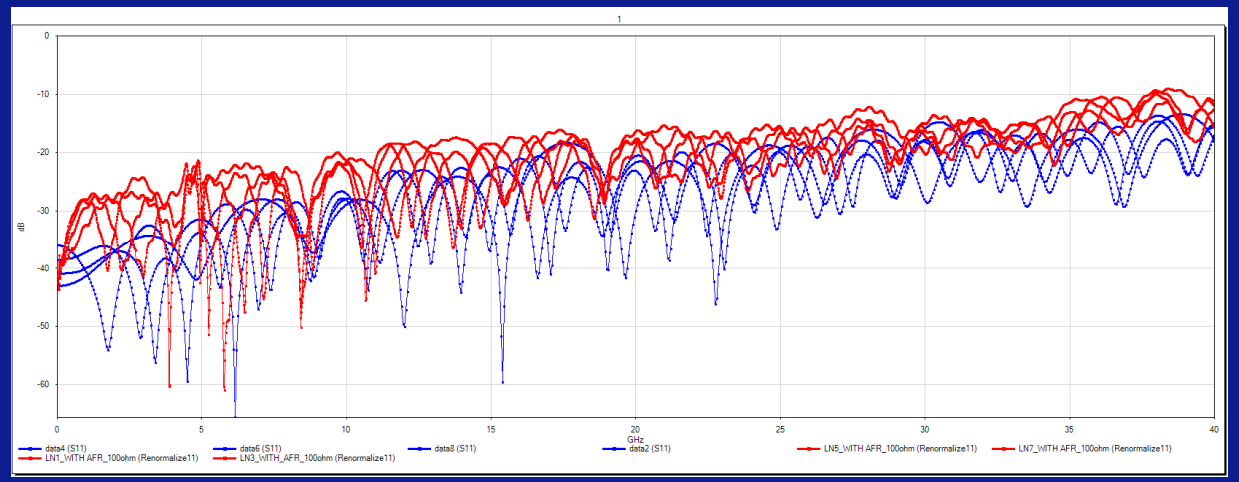
PCB Loopback Return Loss – Layer 2 Traces

- Measurements with simulation results of Sdd11
  - The simulations correlate really well up to 40 GHz with measurements here as well
  - Measurements made with 500 µm pitch GSSG probes



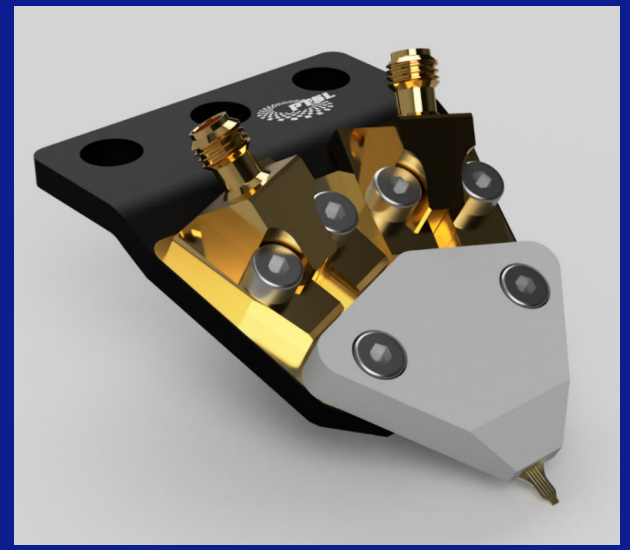
PCB Loopback Return Loss – Layer 5 Traces

- Measurements with simulation results of Sdd11
  - The simulations correlate really well up to 40 GHz with measurements here as well
  - Measurements made with 500 µm pitch GSSG probes



Conclusion

- Successfully measured the results of a 0.5mm pitch DUT with differential loopback for testing a Gigabit Ethernet interface
  - Simulations and measurements match really well
  - Measured data indicates bandwidth for PCIe 7.0 at 32 GHz
- Measurements enabled by PTSL's NuvoRF probe
  - Excellent performance up to 40 GHz in GSSG configuration



PTSL NuvoRF GSSG probe

Acknowledgements

- Tim Penlington for measurements
- Dave Barnes
- Robin Cedeno for simulations

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