Test cost saving and test time reduction solution design and application for automotive on ATE

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TestConX中国 China

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  - Optimized powerup
  - TTR Tips
- Test time analysis tool
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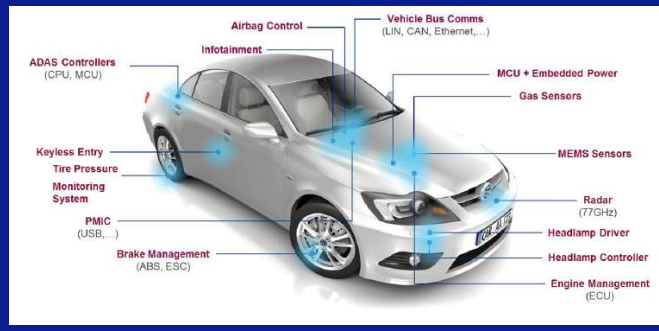
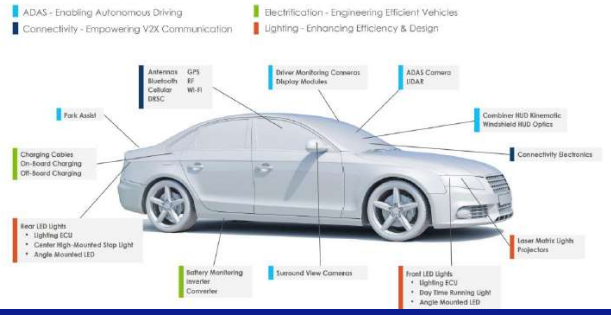
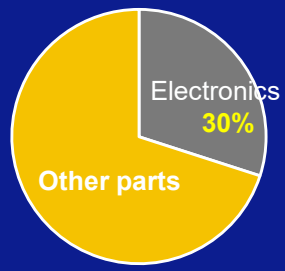
Automotive Electronic Classification





Traditional Automotive

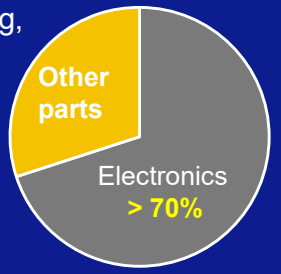


Traditional Automotive:

- Safety and Chassis
  - ABS, ESC, Airbag…
- Power Train
  - Engine Management, injection, transmission…
- Body comfort electronic
  - Door/window/seat controls, LED lighting, wiper…
- Infotainment
  - Audio, GPS…
- Sensors Control
- Acceleration, gyro, pressure…
- Car Radar

New Generation Automotive:

- Hybrid & Electric Vehicles (EV)
  - Battery monitor, Battery Charger, balancing,
  - Motor Driver/controller
  - Switches (HS/LS, H-Bridges…)
- ADAS system extends
  - Lidar
  - Digital Lighting
  - Camera and Sensors
- V2X (vehicle to everything)
  - 5G, Cellular, Wi-Fi, BT, IoT,…



Electronic Automotive

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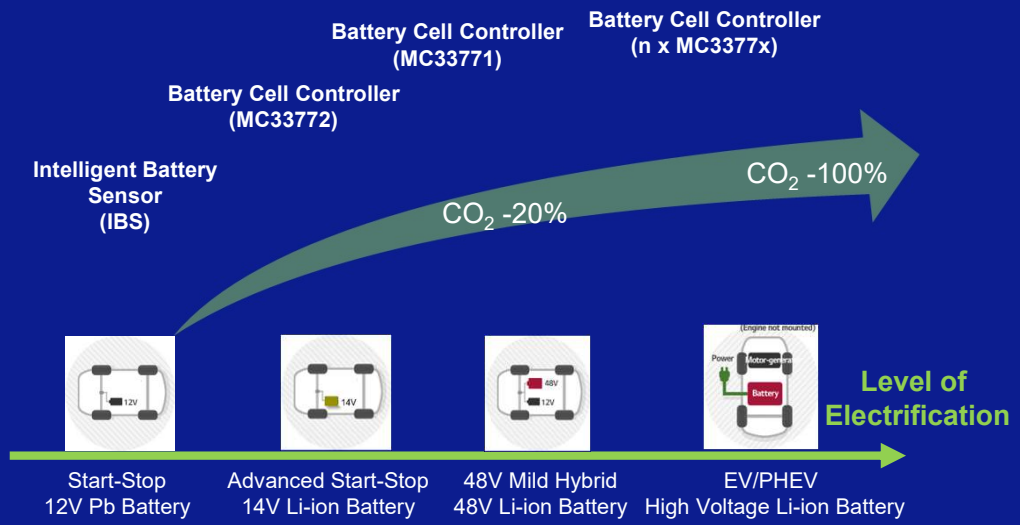
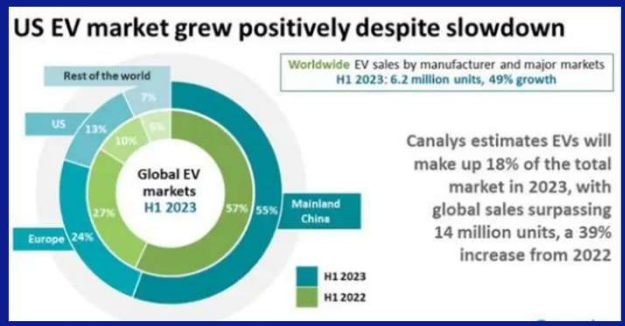
Automotive Electronic Classification-NEV





- 2030: ~50% of all vehicles sold contain electrified powertrains
- Dynamic market environment with emerging (xEV) OEMs
- China major market driver
- Europe leading in 48V hybrid

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Automotive Electronic Testing Challenges

- Different Level VI cards combination
- Increasing components because of high parallelism
- Lots of resource sharing
- Test time and test cost
- High voltage and current requirements and high accuracy measurement
- High test program quality and yield
- Vector memory limitation

Test Cost Control

One good test solution can use lesser license and resource to achieve Lesser test time, Higher yield, and Higher parallelism.

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Memory Pooling and Sharing--Pooling

Reason: Some devices require large patterns for functional tests of SCAN (or ATPG) pins. One can deter the issue of not enough pattern memory space during load board design.

Solution: PS1600 CHs that belong to 8-Channel group use the same physical memory. This is exploited by the so-called memory pooling. Memory pooling allows you to distribute the vector memory within a channel group flexibly among the channels of the group.

Real case:

Digital Pins(SCAN pins)	10
Digital Pins(Non-SCAN pins)	19
PMUX control pins	24
Utility control pins	4
Total:	57

- Distribute the SCAN pins evenly across the PS1600 cards.
- If you have unassigned PS1600 CHs, distribute it to 8-Channel group with Scan Pin.

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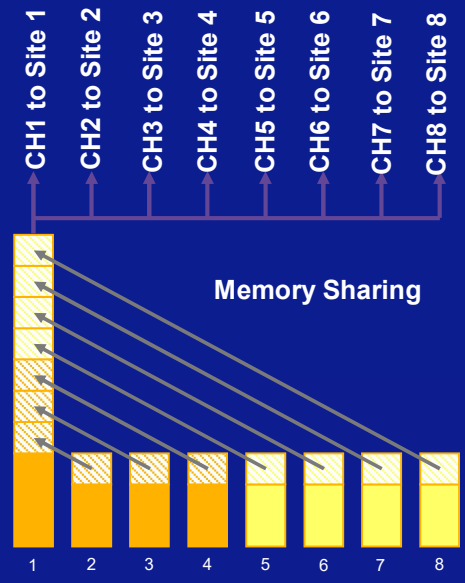
Memory Pooling and Sharing--Sharing

The channels that are assigned to different sites of the same pin **physically share their vector areas**, provided that these channels belong to the same 8-channel group.

- Multiple pins get data from one memory configuration.
- Pattern content of one pin can be broadcasted to 8 pins.



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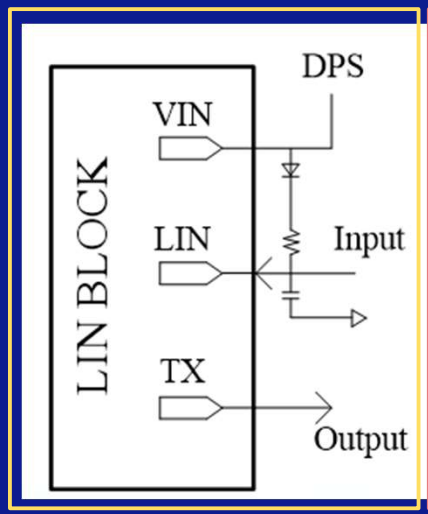
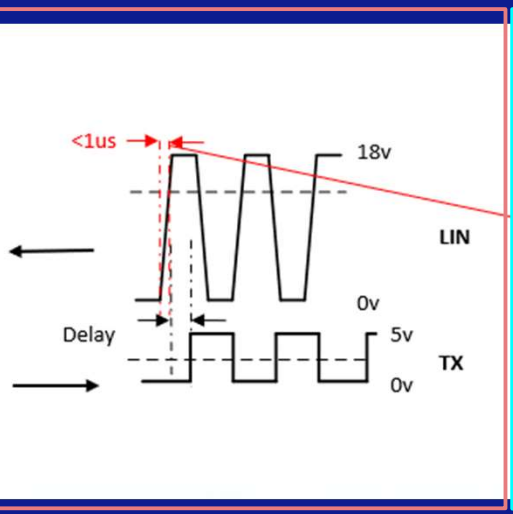
LIN Bus-Propagation Delay

Local Interconnect Network

LIN hardware setup:



The Propagation delay test :



The specification requirement :

- Stimulus
- Voltage: 18 V
- Stimulus Slew rate > 18v/1us

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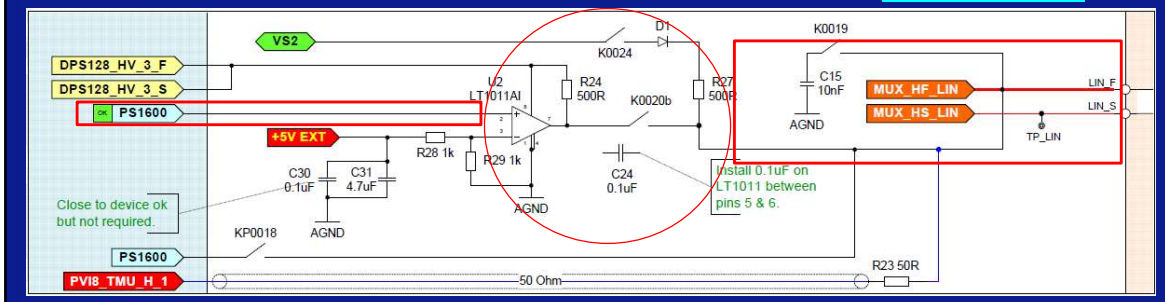
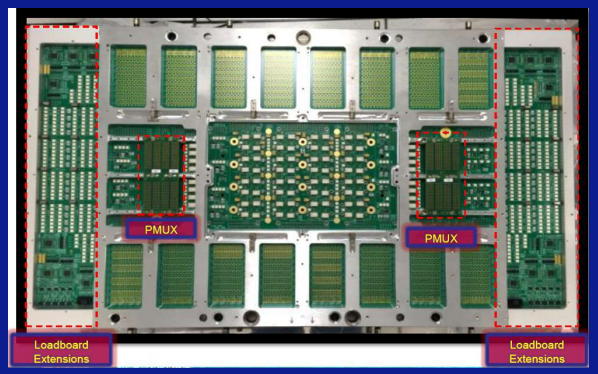
LIN Bus-Propagation Delay

- Use PS1600 with amplifier to send high voltage in high slew rate

Real Case: X16





DUT Board with wings

1. High Cost

2. More Hardware Risks

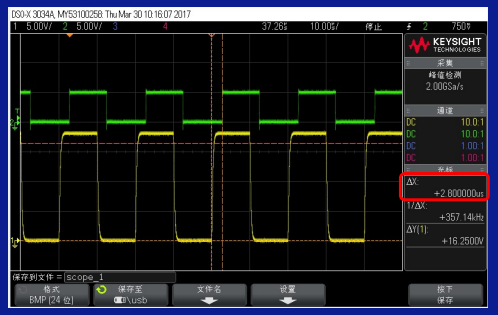
- Consumes lots of components -- consumes DUT Board spaces
- Lower accuracy -- amplifier error involved

LIN Bus-Propagation Delay

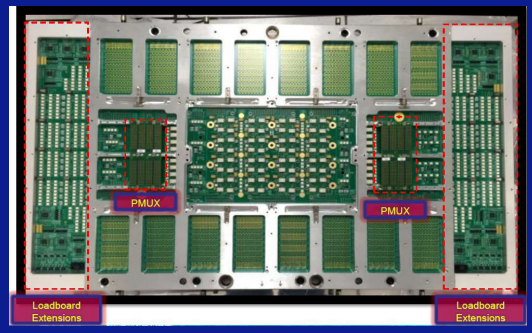
❖ Specification

Digital driver [3]		
	-8 V ≤ V_{IL}, V_{IH}, V_T ≤ +8 V	-40 V ≤ V_{IL}, V_{IH}, V_T ≤ + 80 V
Driver states	V_{IL}, V_{IH}, V_T [4], High-Z	V_{IL}, V_{IH}, V_T [4], High-Z
	± (30 mV + 0.1 % of setting)	± (50 mV + 0.1 % of setting)
Level accuracy		
Overshoot / undershoot	10 % of programmed level	10 % of programmed level
Maximum drive current	± 50 mA	± 50 mA
Driver slew rate (typical)	50 V / µs @ 3 V swing	80 V / µs @ 12 V swing

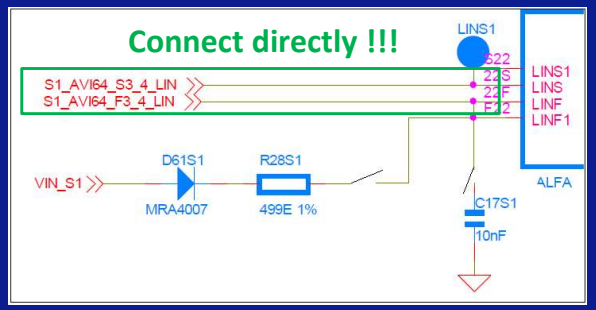
❖ Results

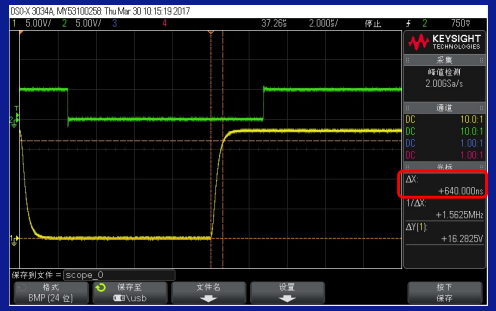


First version: with wings

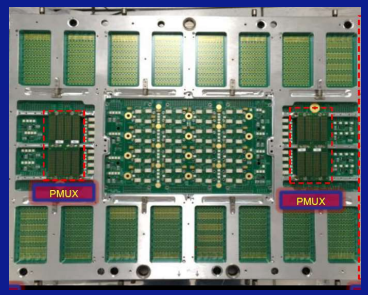


❖ DUT Board Design





Final version: without wings



REDUCE COST !!!

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Tester License/Hardware Limitation

Cards	Limitations	Solutions
	Speed and vector memory limitation	Xmode,93K memory sharing and pooling
	TMU license	Spec search, digital capture
	BADC shared among one pogo block(16 pins)	SA(PPMU),assign to different block
	HV pin is only 01 channel of pogo block	Use level to active high voltage channel
	8 HCUs/differential voltmeters for one card, one per group of 8 chanels	Assign to different group
	Digital I/O mode	Create new mode context
	TMU license	PMU mode, digital I/O mode, several measurement modes, resource sharing
	Hi-res AWG is available per group of 8 channels.	Assign to different group.±4Vand±8V
	TMU license	PMU mode, digital I/O mode, several measurement modes,resource sharing
	±60 vrange,-60V…+120V range	Default for ±30V range

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TTR Strategy

Hardware	Software	Tool-TP360
• Solution • Assignment	• TTR tips	• Measure/analysis • Breakdown

- Kelvin test
- DC resources sharing using PMUX
- Optimized powerup

- Software points for TTR
  - Merge RDI BLK
  - Merge test suites

- Collect and analyze test time
- Check the test program quality

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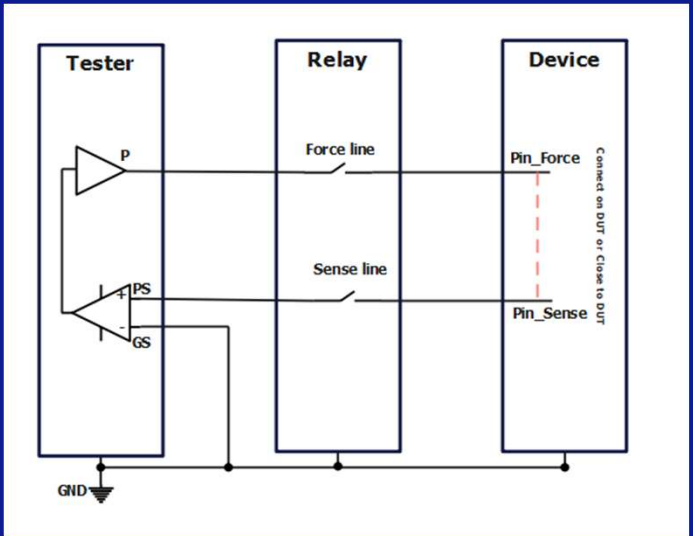
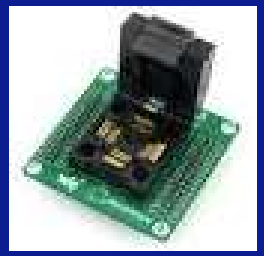
Kelvin Test

Kelvin Connection



Kelvin connection on LB



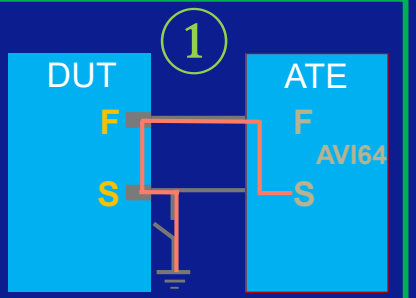
Kelvin socket

Kelvin prober card

Regulation loop control can compensate the voltage drop on the P# line, make sure the voltage presented to DUT.

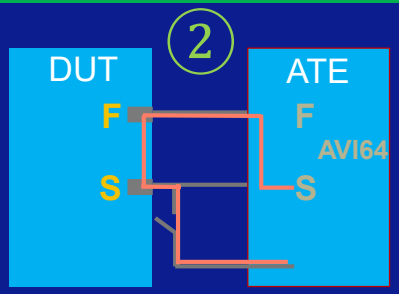
Kelvin Test

4 Ways of Kelvin Test

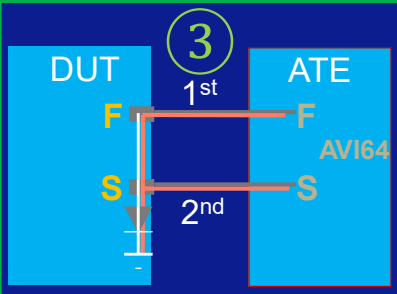


Relay to GND:
IFVM with sense over force

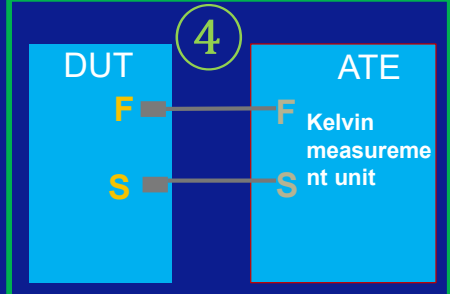
Recommended method



Relay to PS1600, PS1600 force 0V:
IFVM with sense over force
Disadv: additional PS1600 needed



By ESD:
1st : IFVM with sense over force
2nd: IFVM with force over sense
Disadv: two measurements is needed, will take more test time.



By Kelvin measurement unit:
Return the pass/fail result.
Disadv: No test value

```
rdi.dc().pin("ALL_AVI_group").disconnect().execute();//Before change connect state, need to disconnect firstly
//Set up sense only
rdi.dc().pin("ALL_AVI_group").vForce(0 V).vForceRange(3 V).iForceRange(200 mA).iClamp(-200 mA, 200 mA).connectState(TA::SENSE_OVER_FORCE).execute();
RDI_BEGIN(m_tUserRunMode);
rdi.route().applyState("KELVIN_G1_PMX").execute();//close PMUX
rdi.wait(1 ms);
rdi.dc(m_sTsName + "G1").pin(m_sKelvinPins1).iForce(4 mA).vClamp(-3 V, 3 V).measWait(2 ms).vMeas().execute();//--- measure
```

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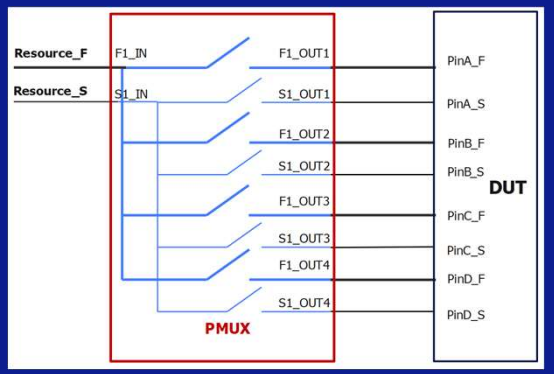
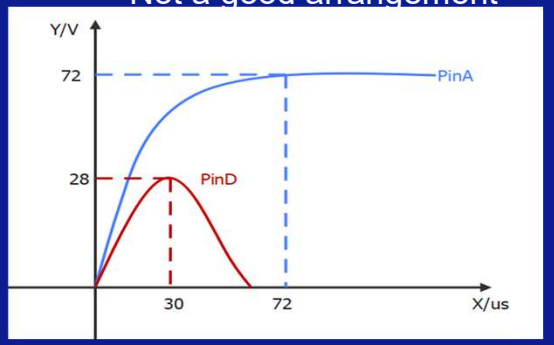
TTR-Resource Assignment for PMUX

Pin	Min voltage	Max voltage
PinA	-10V	72V
PinB	-10V	72V
PinC	-10V	72V
PinD	-2V	15V
PinE	-10V	70V

Min/Max voltage requirement sheet



Not a good arrangement



PMUX switches can help achieve the tester resource shared.
When resource card forces 72V to PinA, Spike voltage will appear on the PinD no matter the OUT4 switch is on or off.
Possible results:

- Increase the test time
- Damage the device
- Low yield
- Impacted the lifecycle of product

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TTR-Resource Assignment for PMUX

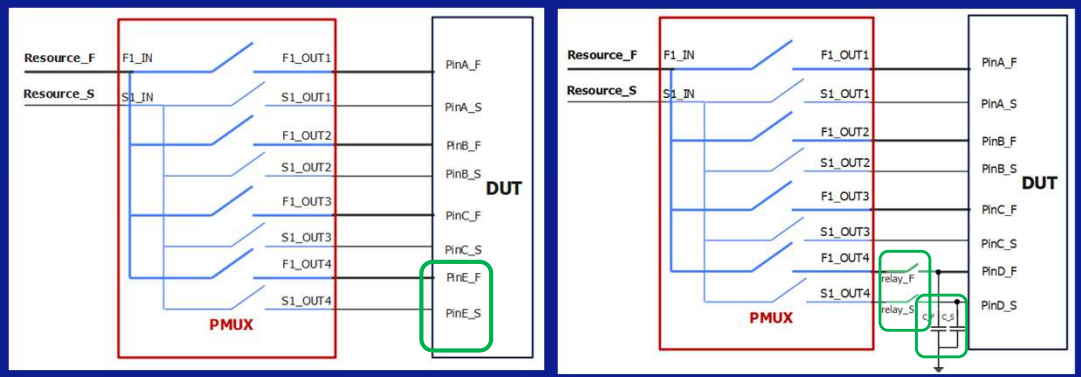
- To remove spike:
  - Use the vSlewRate() to control the rise time
  - Use stepped force volt to get the target volt
  - Use the waveform() and samplePeriod() to slow down the voltage slope

```
rdi.dc().pin(PinD).vForce(72 V).vForceRange(80 V).iForceRange(50 mA).iClamp(-50 mA,50 mA).vSlewRate(100 mV).execute();

anaWaveform  wavup_72V("rampup_72");
wavup_72V.definition(TM::RAMP).periods(1).direction(TM::POS).samples(72).min(0 V).max(72 V);

rdi.dc().pin(PinD).vForce().vMeas().waveform(wavup_72V).samplePeriod(10 us).execute();
```

Long test time



Same level voltage pins to one PMUX
Use relay or capacitor to do isolation

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TTR-Optimized Powerup

Original:

Resources	Relay	Pin
AVI64_15(TMU)	PMUX	VBAT/VBOOST
AVI64_16	PMUX	VBOOST/VBAT
FVI16_2	AQY222	VBAT
FVI16_4	AQY222	VCCP
DPSHV_1	AQY222	VBAT
DPSHV_2	AQY222	VBOOST
DPSHV_3	AQY222	VCC5
DPSHV_4	AQY222	VCCIO

New:

Resources	Relay	Pin
AVI64_15(TMU)	PMUX	VBAT/VBOOST
~~AVI64_16~~	~~PMUX~~	~~VBOOST/VBAT~~
FVI16_1	AQY222	VCCIO
FVI16_2	AQY222	VBAT
FVI16_3	AQY222	VBOOST
FVI16_4	AQY222	VCCP
DPSHV_1	AQY222	VCC5
~~DPSHV_4~~	~~AQY222~~	~~VCCIO~~

- Frequently switch the resources combination of powerup to meet requirement of high voltage, accurate measurement and TMU using in the test flow.
- Often can use the FVI16 to satisfy the needs of test condition. The lesser resources combination and switching, the lesser test time.

TTR-Tips

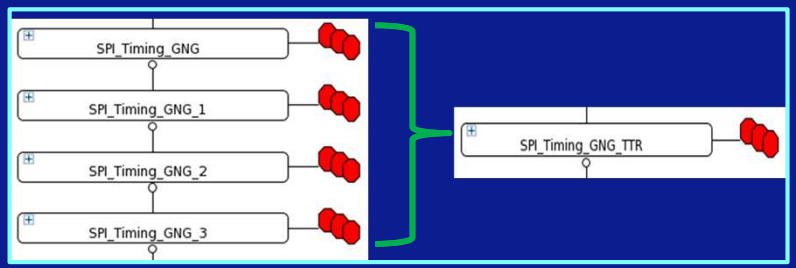
```
RDI_BEGIN(TA::BURST);
    rdi.dc().pin("VDDP").vForce(5.1 V).execute();
RDI_END();

RDI_BEGIN(TA::BURST);
    rdi.dc().pin("VDDC").vForce(1.53 V).execute();
RDI_END();
```

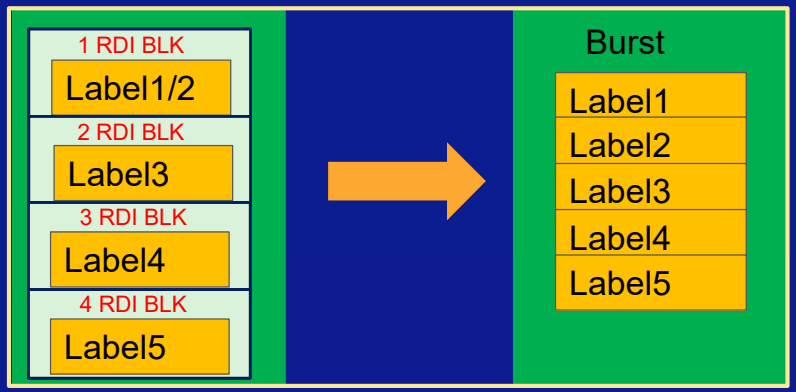
RDI block

```
RDI_BEGIN(TA::BURST);
    rdi.dc().pin("VDDP").vForce(5.1 V).execute();
    rdi.dc().pin("VDDC").vForce(1.53 V).execute();
RDI_END();
```

RDI execute

```
RDI_BEGIN(TA::BURST);
    rdi.dc().pin("VDDP").vForce(5.1 V)
            .pin("VDDC").vForce(1.53 V)
            .execute();
RDI_END();
```





- Merge RDI block
- Merge RDI execute to allow parallel execution
- Merge test suite

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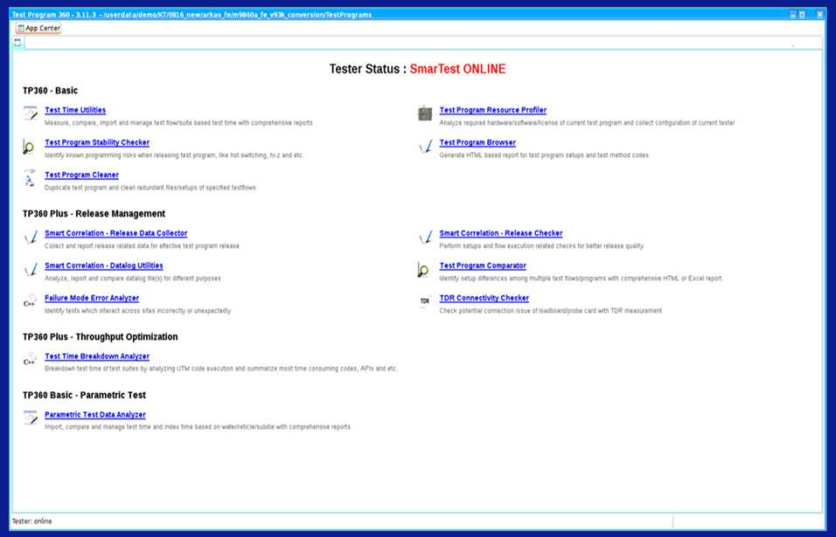
Test Time Analysis Tool

- Test time is key point for test program, so it is important if one tool can help us to collect and analyze test time automatically.
- Test Program 360(TP360) is a GUI tool independent of SmarTest, designed to check the quality and performance of your test program.



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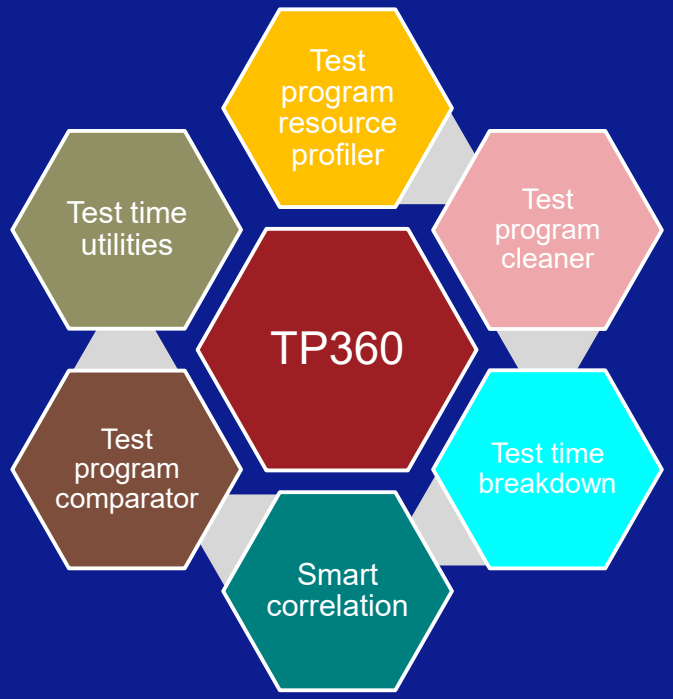
Test Time Analysis Tool

It provides various function modules for you to easily examine test programs in different scenarios and different purposes.



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Summary

1: Vector memory optimization: Memory pooling and sharing.

2: One real case: One reduced cost solution with digital I/O mode

3: Hardware license/limitation: Resource assignment and points.

4: Kelvin test: The advantages and disadvantages of 4 test solutions.

5: Resource assignment for PMUX: the pins of same level voltage to one PMUX or isolation.

6: Resource optimization for PowerUp: Lesser resources combination and lesser test time.

7:TP360 introduction and some TTR tips.

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