Substrate on PCB solution for 0.35mm pitch 26~47GHz mmWave device testing

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Virtual ▪ November 21-23, 2023

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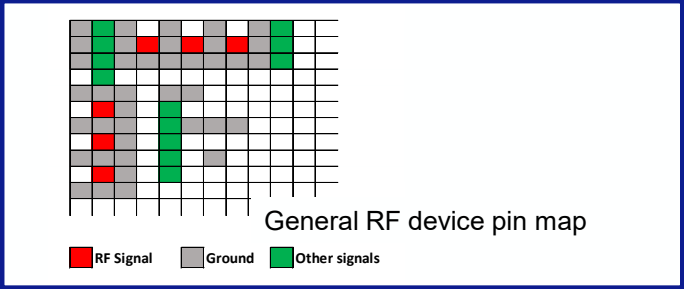
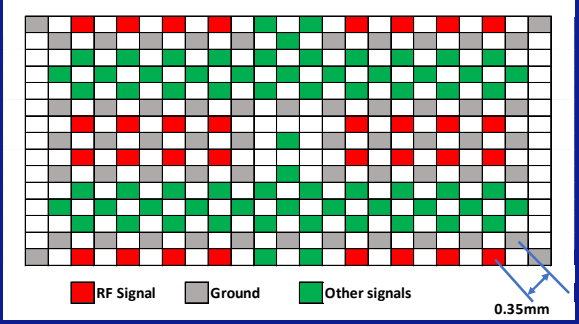
Introduction

- Application towards to use higher frequency (5G FR2, 77GHz radar, etc.)
- Generally, higher frequency RF device with small pin pitch, mmWave device's pin pitch as small as 0.35mm or even smaller.
- Compared to general RF device, mmWave device's RF signal pins: more quantity, concentrated, do not locate in device edge, example as right figure[1]:





- These features make mmWave device's hardware design more challenging: need consider return loss, insert loss, fabrication and assembly, etc.

RF Signal Routing Structure

- Route signal trace on surface layer:
  - Avoid via on signal path
  - Lower design Dk, lower propagation delay
  - Wider trace width and lower loss
- Prefer to route RF trace on surface layer. But for mmWave device with special feature shown in previous page, need route signal trace on inner layer with via:
  - Structure1: single board, need multi-type laser via /blind via, fabrication complexity increase
  - Structure2: with substrate on signal path, transit pitch to 1mm or more, transit pattern to make RF signals on pattern edge, simplify mother board design. Fabrication and assembly complexity increase

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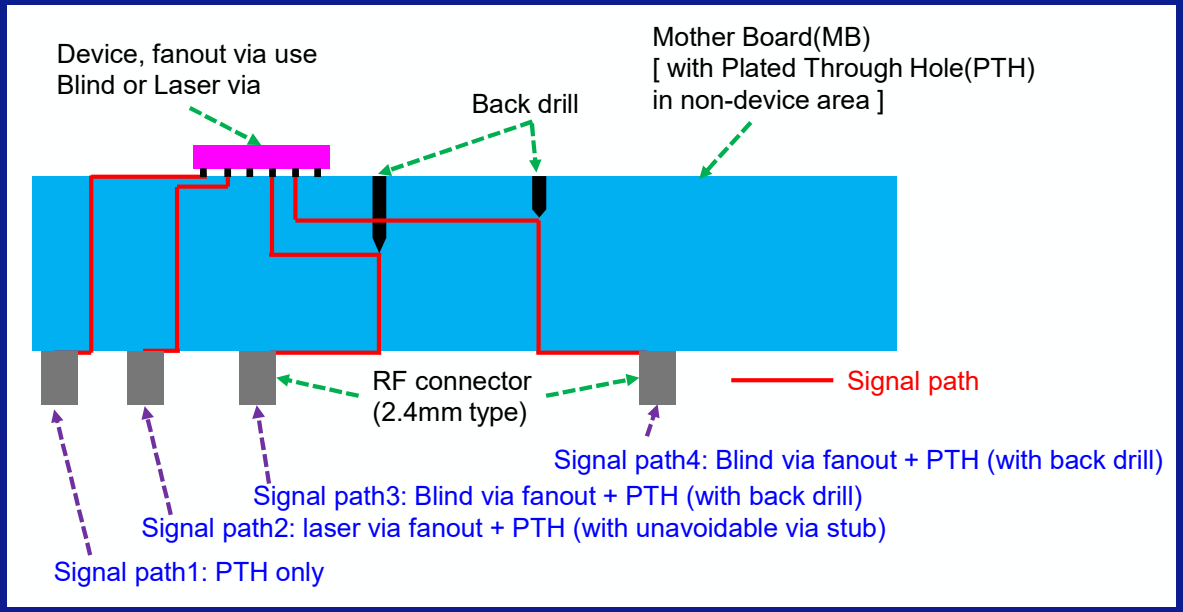
Signal Path Structure1

- Signal structure: single board



1.Many via type significantly increase fab complexity and lead to low yield, sometimes is impossible to fab.

2. Optimize via in signal path is difficult for mmWave frequency. And many type vias will exacerbate this difficulty.

3. Performance may not meet requirement at interested frequency band. (sample study on next page)

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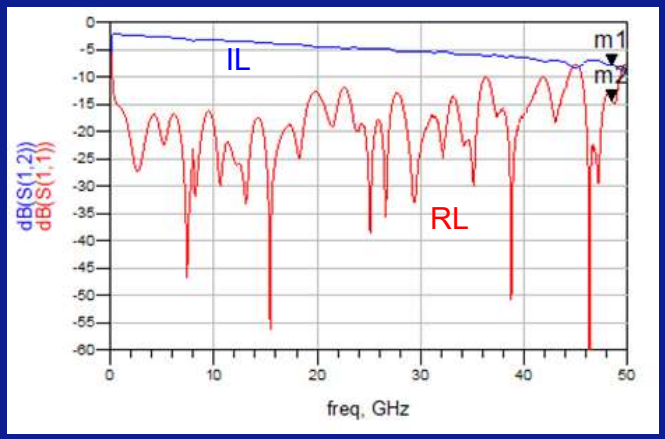
Full Path Result Sample (Structure1)

- Analysis condition: 0.35mm device, frequency range: 26 ~ 47GHz, require RL<-15dB.
- Full path result:



IL: -7.85dB @ 48.5GHz
RL: -7.72dB @ 45.5GHz

- In conclusion: Single board structure may not be suitable for all generic RF device, especially for certain mmWave device introduced in Page3.

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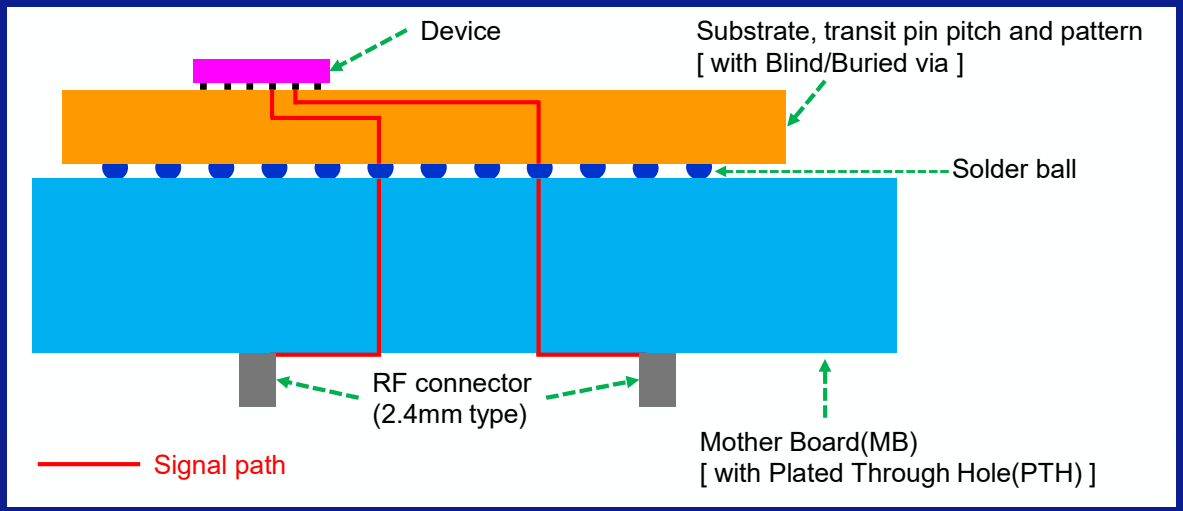
Signal Path Structure2

- Signal structure: with substrate



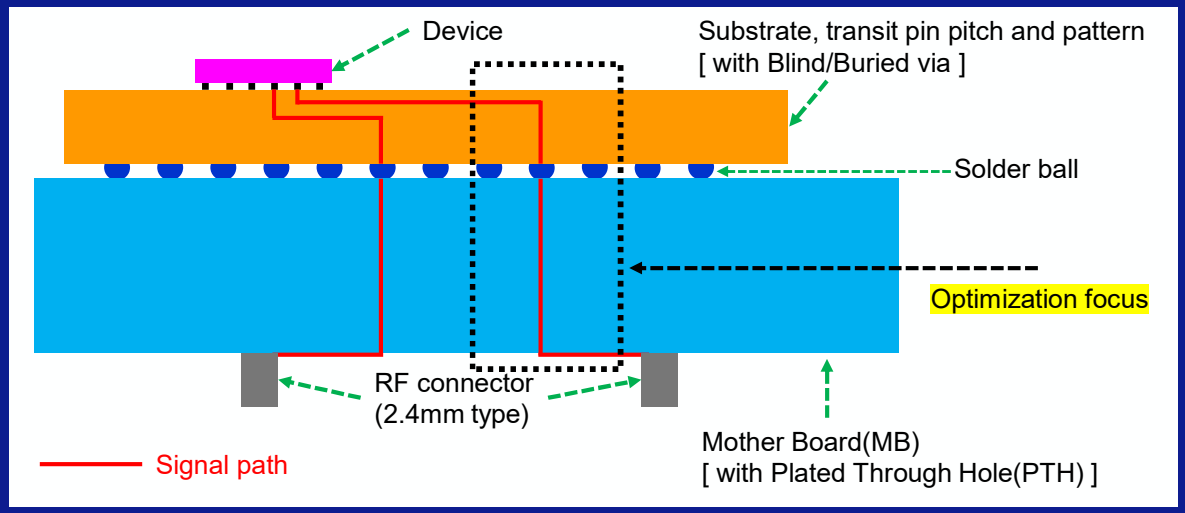
1.Blind/Buried via on substrate only and substrate size is small, will decrease MB fab complexity.

2. Without via stub, and one type PTH via in mother board, optimization is easier.

3. More general hardware structure for mmWave device testing

Signal Path Structure2

- Signal structure: with substrate



Design optimization will focus on “Substrate + Solder ball + MB PTH”

- Analysis condition: 0.35mm device, frequency range: 26 ~ 47GHz, transit pitch and pattern by substrate, require RL<-15dB.

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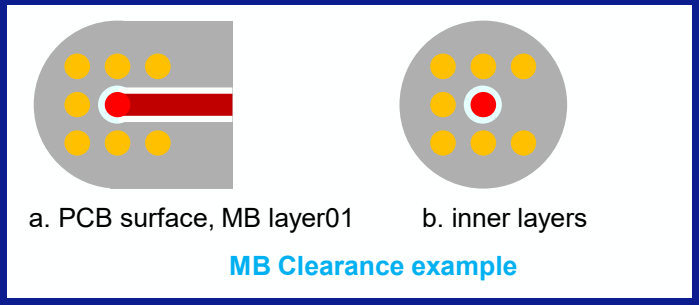
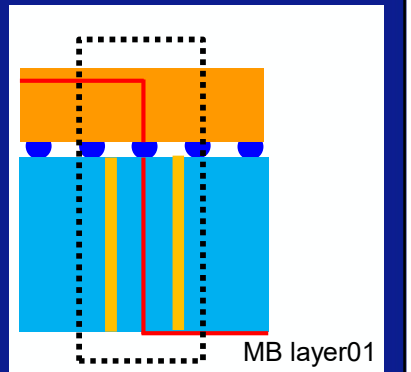
Optimize Consideration

- Consider fab capacity, based on dielectric material and stack-up, simulation will help determine:
  - BGA pin pitch and drill size
  - MB: GND clearance need to be adjusted through all Layer
    - Signal via to around ground via clearance
    - Signal via to around ground copper clearance

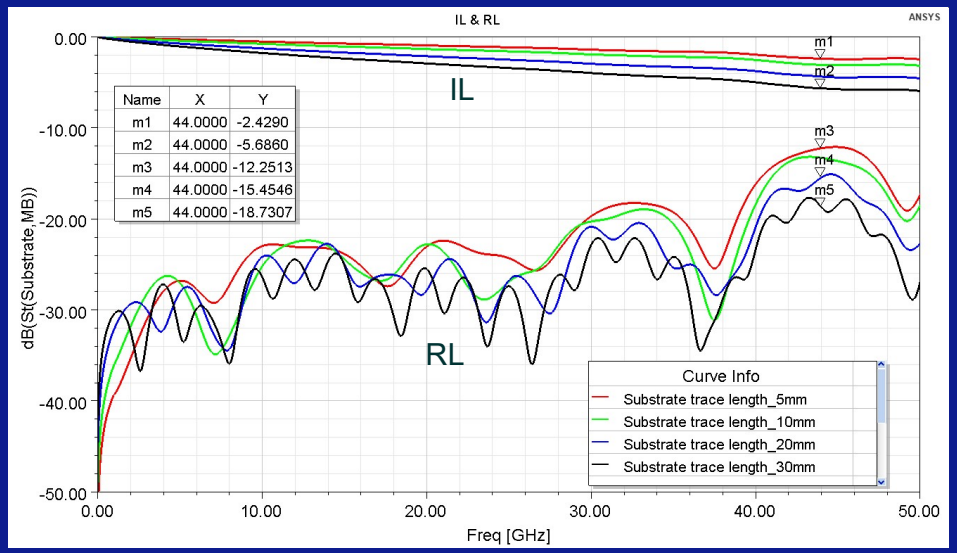


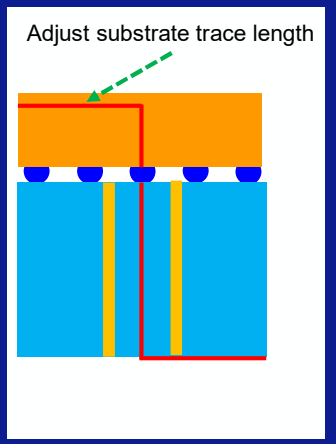
MB Clearance example



Optimize Consideration

- Adjust trace length appropriately in substrate to mitigate via's reflection:



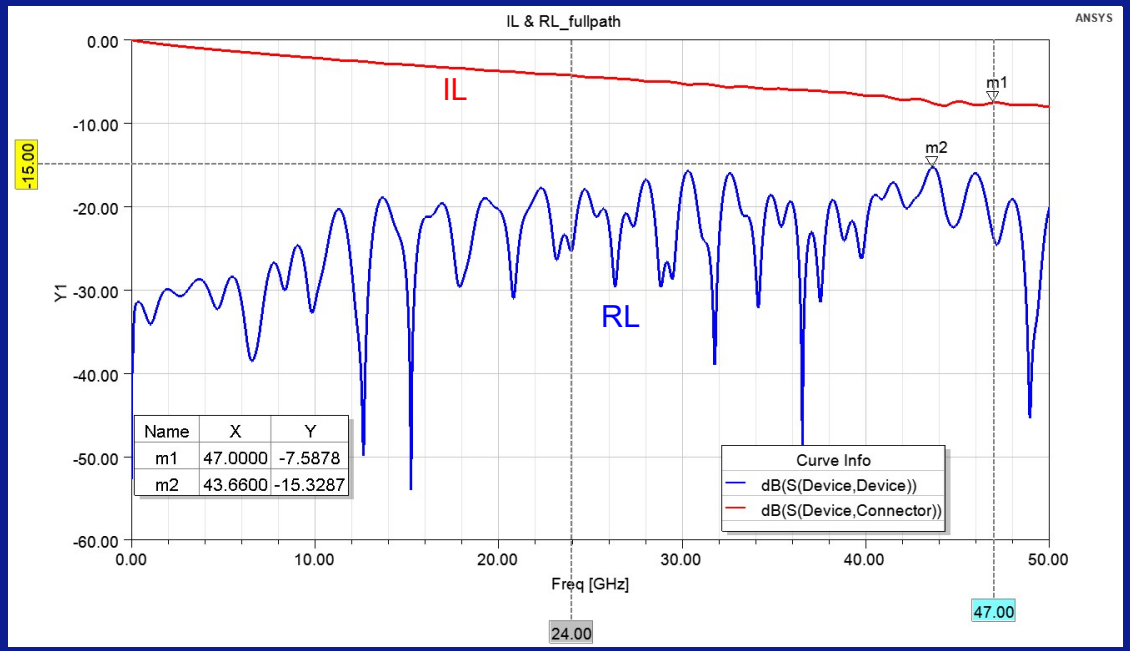


@44GHz		
Length	**IL (dB)**	**RL (dB)**
5mm	-2.43	-12.25
10mm	-3.11	-13.30
20mm	-4.39	-15.45
30mm	-5.69	-18.73

Longer trace with worse IL but better RL, try to balance between IL and RL.

Full Path Result Sample (Structure2)

- Full path result:



IL: -7.58dB @ 47GHz
RL: -15.3dB @ 43.66GHz

IL difference between simulation and measurement <15%

Conclusion

- Simulation help determine drill, signal via to ground via/copper clearance, trace length, etc. Optimization need obtain a balance between RL and IL for full path.
- For mmWave device with ≤0.35mm pitch: substrate on PCB solution can effectively achieve performance requirement at 26~47Ghz frequency with lower optimization cost. In same certain cases, substrate on PCB solution will be a better choice than single board solution.

References

- [1] K. M. Lee, J. H. Oh, M. S. Kim, et al. RF Pogo-Pin Probe Card Design Aimed at Automated Millimeter-Wave Multi-Port Integrated-Circuit Testing[J], Electronics, 2021,10(19),2446. https://www.mdpi.com/2079-9292/10/19/2446

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