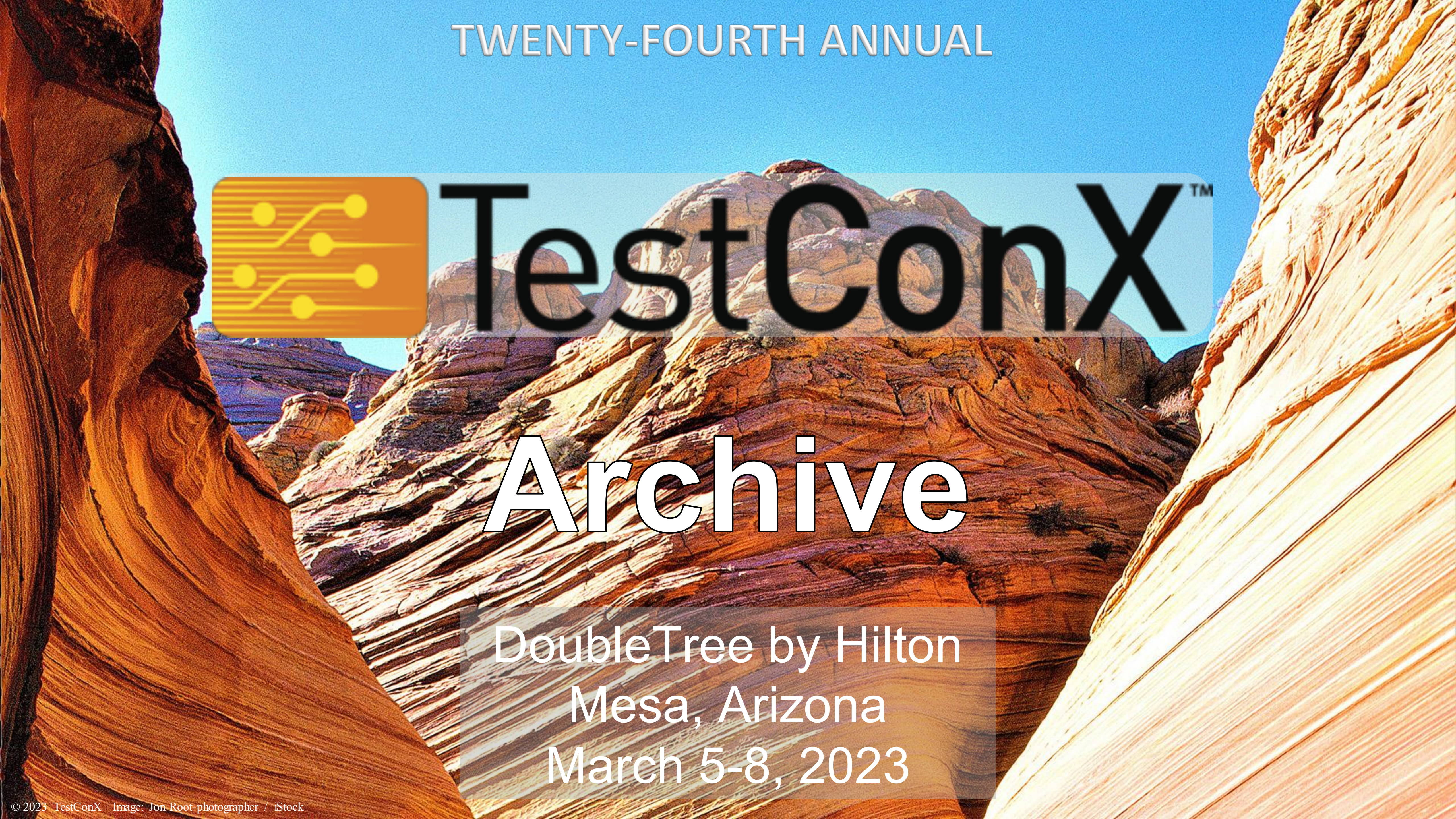

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Mesa, Arizona
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# Full RF Characterization of Contactor Design on Load Board

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Noel Del Rio - NXP

TestConX
Mesa, Arizona • March 5-8, 2023

# Agenda

- New markets
- Contactors and Load Board design
- Simulation / Measurements
- Challenges and solutions
- Conclusion

# New Market

Growth in the global market is due to increasing sale of consumer electronics, unabated expansion of the automotive industry and technological advances driving high bandwidth integrated RF devices applications

Device Requirements:
Low noise, high gain, advanced power delivery, high frequency

Contactor Requirements

Low loss (1dB >40GHz)

High isolation (>60dB)

Low inductance (<0.1nH)

Matched impedance (50Ω+/- 5%)

# Contactor design

## Features & Benefits

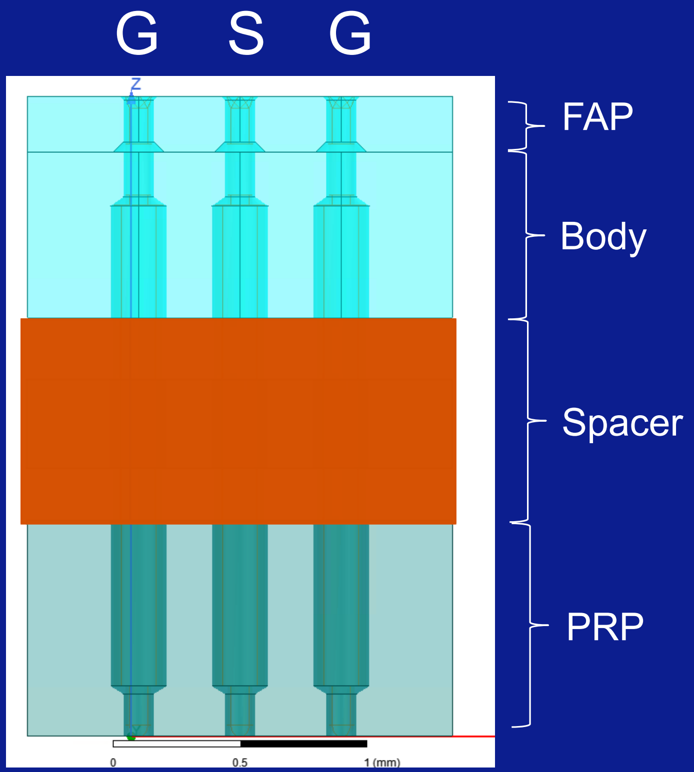
- Uses standard spring probe technology for affordable 5G mm Wave device testing
- Dielectric optimization Field replaceable individual probes available
- Significantly improves insertion loss and return loss at all pitches
- Low inductance 5G application solutions ranging from 6GHz to >=54GHz signals
- Fine pitch package, wafer, and WLP compatibility

## Applications

- mm Wave 5G applications
- Transceivers, FEMs, PAs, LNAs, Switches, Filters
- Everything 5G

# Contactor cRacer Optimization Process

- Select pin based on required pitch and tip profile
- Select contactor materials for PRP, Spacer, Body and FAP to provide required mechanical strength and dielectric performance
- Dielectric is adjusted, then RF performance is re-simulated in GSG or GSSG configuration
- Tune performance by matching to required impedance (typically 50 Ohms) across bandwidth of interest

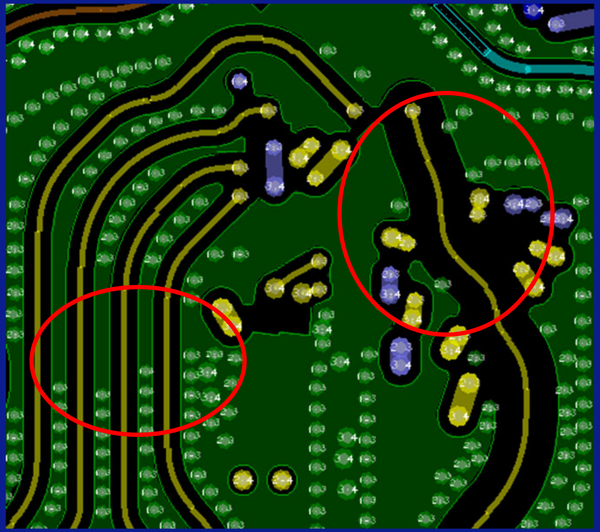



PRP = Probe Retainer Plate
FAP = Floating Alignment Plate

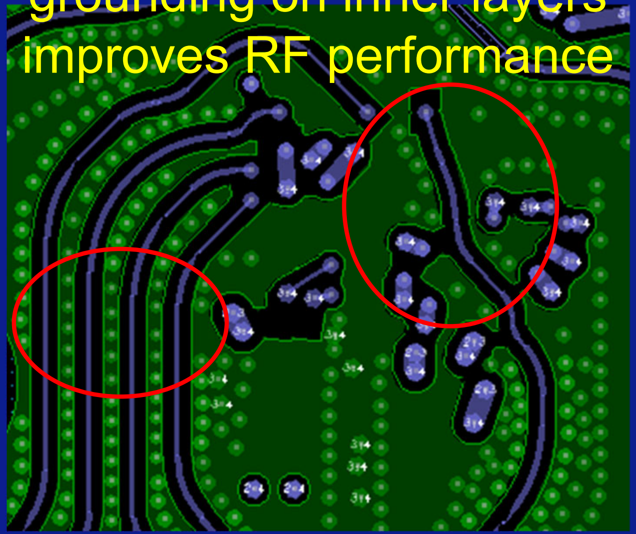
# Load Board Signal Path Optimization

- Simulation and optimization process can include entire signal path, including PCB, with review of changes required to get best RF performance in conjunction with cRacer cross-section

**Before Optimization**

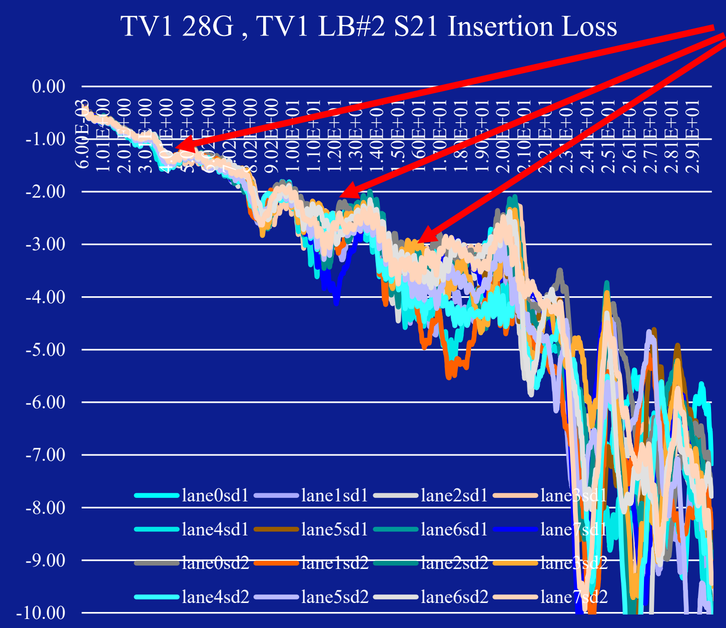


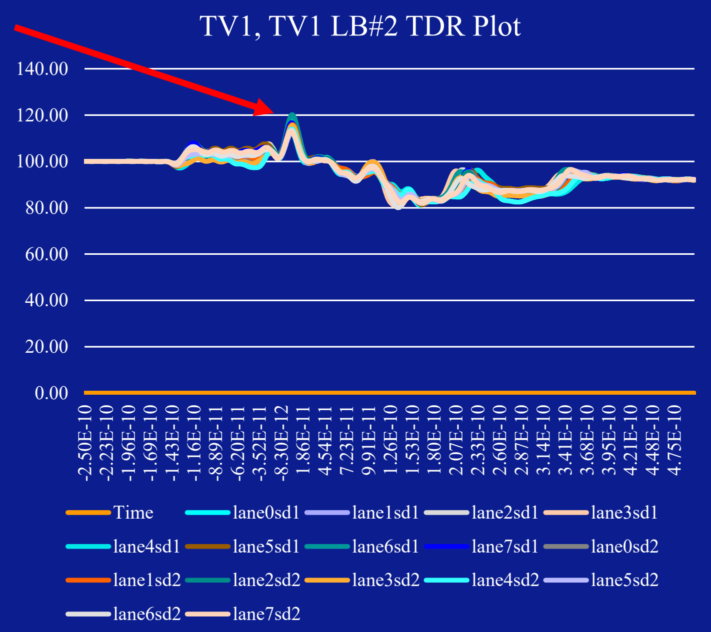
**After Optimization :** more grounding on inner layers improves RF performance



# Example Design and Performance validation of 28 GHz test socket

The inductive pins correlate with rippling on S21 plots for TV1 REV1



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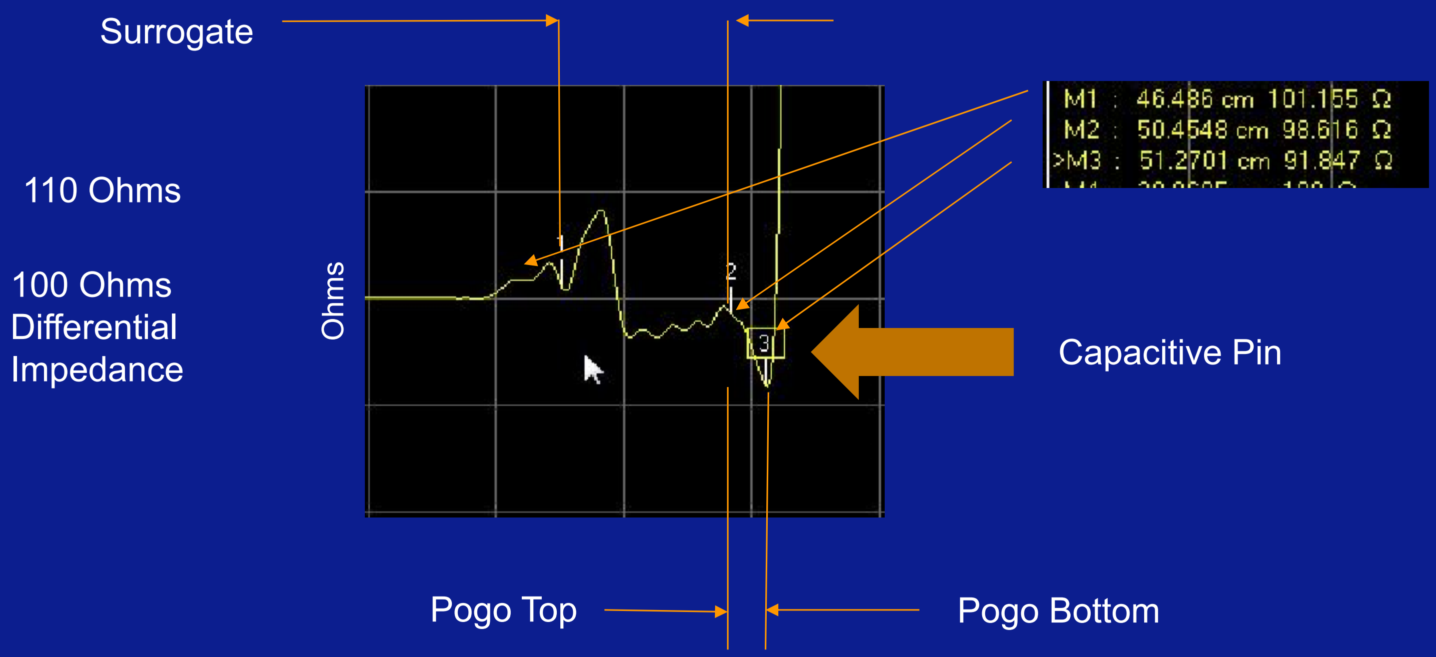
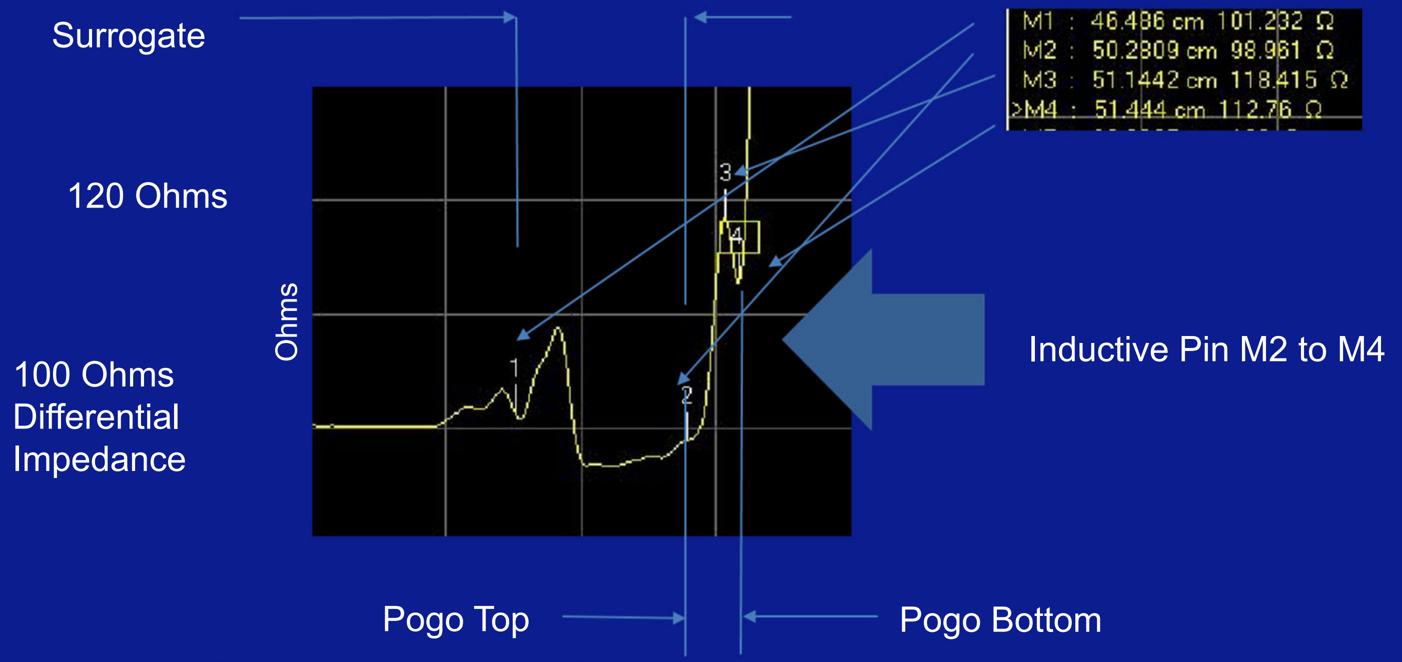
## Example Design and Performance validation of 28 GHz test socket

Socket T4-B to T4-BTV1 conversion resulted capacitive pin



# Examples Design and Performance validation of 28 Ghz test socket




The TV1 Team decided against SKT4-A

1. High discontinuity (>120 Ohms Impedance
2. S21 Failed to clear the -10db limit at 15GHZ at cycle = 0

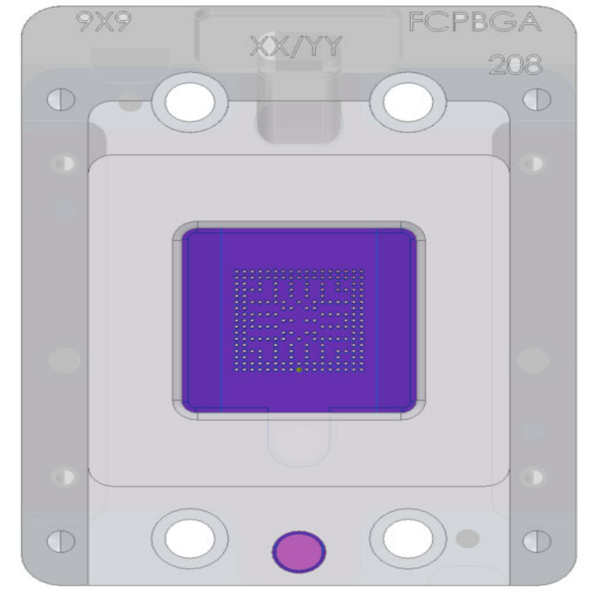
# TestConX 2023

## Simulation – Examples - Device Pinout

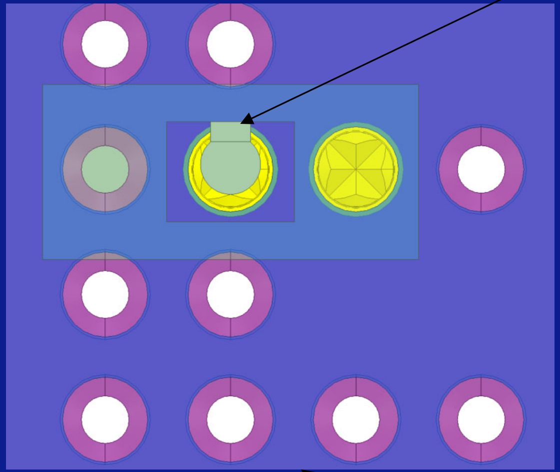
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | DRAM_CA5_A | USB1_TXRTUNE | USB1_D_N | RTC_XTALI | CLKIN1 | PMIC_ON_REQ | ADC_IN1 | XTALI_24M | PDM_BIT_STREAM0 | I2C2_SCL | I2C1_SCL | UART1_TXD | SAI1_TXFS | SAI1_TXD0 | PDM_CLK | VSS |
| B | DRAM_CK_C_A | DRAM_CA4_A | USB1_VBUS | USB1_D_P | RTC_XTALO | CLKIN2 | POR_B | ADC_IN0 | XTALO_24M | PDM_BIT_STREAM1 | I2C2_SDA | I2C1_SDA | UART1_RXD | SAI1_RXD0 | SAI1_TXC | GPIO_IO00 | GPIO_IO01 |
| C | DRAM_CA3_A | DRAM_CK_T_A | | VDD_USB_0P8 | | VSS | | VSS | PMIC_STBY_REQ | VDD_BBSM_0P8_CAP | | VSS | | VSS | | GPIO_IO02 | GPIO_IO03 |
| D | DRAM_CS[illegible]_A | DRAM_CA2_A | VSS | USB1_ID | | TAMPER0 | | TAMPER1 | | ONOFF | | UART[illegible]_TXD | | UART2_RXD | VSS | GPIO_IO04 | GPIO_IO05 |
| E | DRAM_CS1_A | DRAM_CA1_A | | | | VDD_USB_1P8 | | VDD_USB_3P3 | | NVCC_BBSM | | VSS | | | | GPIO_IO06 | GPIO_IO07 |
| F | DRAM_CA0_A | DRAM_CKE1_A | VSS | DRAM_RESET_N | VDDQ_DDR | VSS | | VSS | | VSS | | VDD_ANA0_1P8 | VDD_ANA0_0P8 | GPIO_IO12 | VSS | GPIO_IO09 | GPIO_IO10 |
| G | DRAM_CKE0_A | DRAM_DQ07_A | | | | VSS | VDD_SOC | | VDD_SOC | | VDD_SOC | VSS | | | | GPIO_IO11 | GPIO_IO13 |
| H | DRAM_DQ06_A | DRAM_DQ05_A | VSS | DRAM_ZQ | VDDQ_DDR | | VDD_SOC | | VSS | | VDD_SOC | | NVCC_AON | VDDQ_ANY | VSS | GPIO_IO14 | GPIO_IO15 |
| J | DRAM_DQ04_A | DRAM_DMI0_A | | | | VSS | | | | | | VSS | | | | GPIO_IO16 | GPIO_IO19 |
| K | DRAM_DQ03_A | DRAM_DQ02_A | VSS | DRAM_DQS0_C_A | VDD2_DDR | | VDD_SOC | | VSS | | VDD_SOC | | NVCC_GPIO | GPIO_IO08 | GPIO_IO17 | GPIO_IO20 | GPIO_IO21 |
| L | DRAM_DQ01_A | DRAM_DQ00_A | | | | NVCC_WAKEUP | VSS | | NVCC_WAKEUP | | NVCC_WAKEUP | VDD_ANAVDET_1P8 | | | | SD2_DATA3 | SD2_DATA2 |
| M | DRAM_DQ15_A | DRAM_DQ14_A | VSS | DRAM_DQS0_T_A | VDD2_DDR | VSS | | VSS | | VSS | | VSS | VDD_ANA1_0P8 | GPIO_IO18 | VSS | SD2_CLK | SD2_CMD |
| N | DRAM_DQ12_A | DRAM_DQ13_A | | | | VDD2_DDR | | VDD_ANA1_1P8 | | VSS | | NVCC_SD2 | | | | SD2_DATA1 | SD2_DATA0 |
| P | DRAM_DQS1_T_A | DRAM_DQS1_C_A | VSS | VDD2_DDR | | DAP_TMS_SWDIO | | DAP_TDI | | SD2_RESET_B | | SD2_CD_B | | SD2_VSELECT | VSS | SD3_DATA2 | SD3_DATA3 |
| R | DRAM_DMI1_A | DRAM_DQ11_A | | VSS | | VSS | | VSS | ENET1_TD1 | VSS | | VSS | | VSS | | SD3_DATA0 | SD3_DATA1 |
| T | DRAM_DQ10_A | DRAM_DQ08_A | DAP_TDO_TRACESWO | CCM_CLKO1 | ENET1_RX_CTL | ENET1_RD1 | ENET1_RD3 | ENET1_MDC | ENET1_TX_CTL | ENET1_TD3 | SD1_CMD | SD1_DATA4 | SD1_DATA0 | SD1_DATA1 | SD1_DATA2 | SD3_CLK | SD3_CMD |
| U | VSS | DRAM_DQ09_A | DAP_TCLK_SWCLK | ENET1_RXC | ENET1_RD0 | ENET1_RD2 | ENET1_MDIO | ENET1_TXC | ENET1_TD0 | ENET1_TD2 | SD1_CLK | SD1_STROBE | SD1_DATA3 | SD1_DATA5 | SD1_DATA6 | SD1_DATA7 | VSS |

Red circles are the GS (ground signal configuration

# Simulation Optimized– Examples cRacer050 contactor design only GS configuration



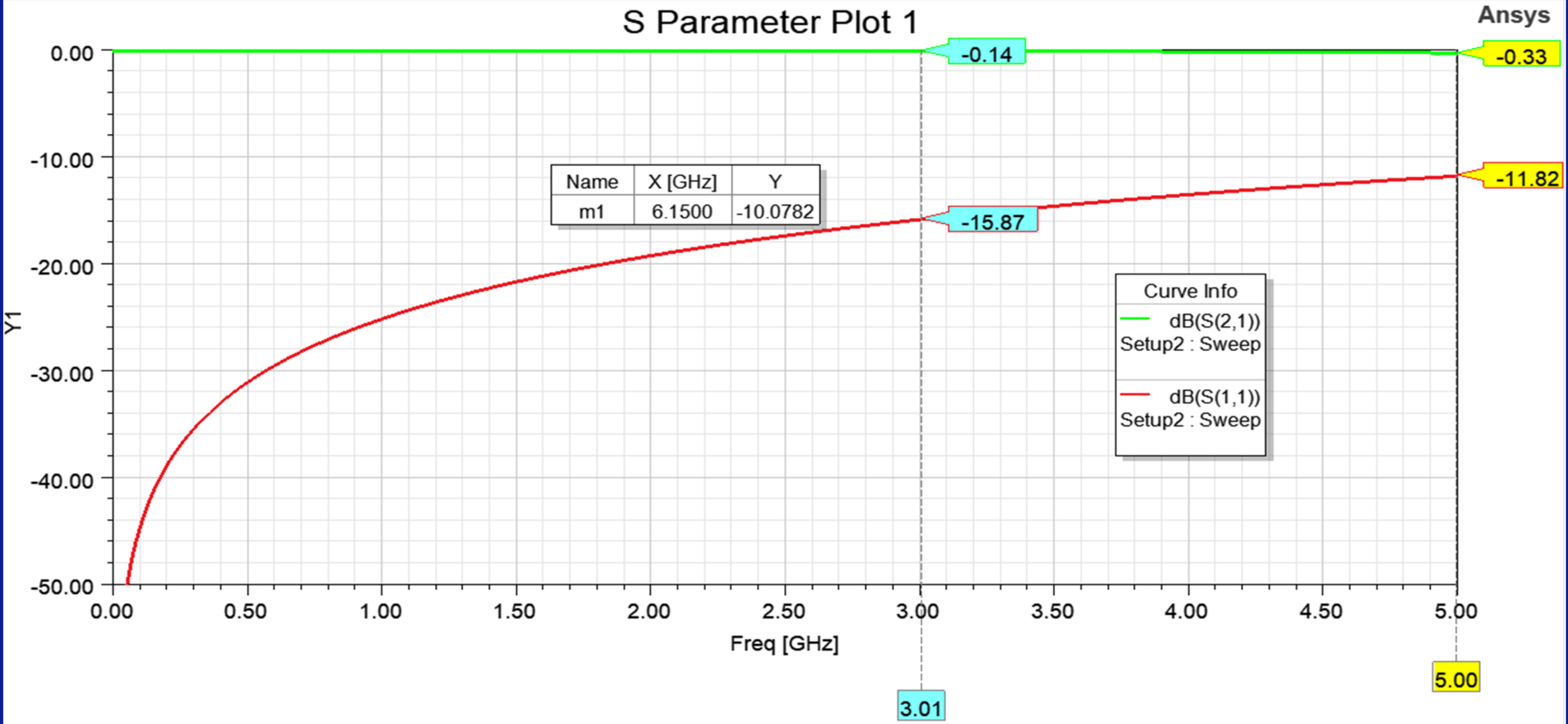

cRacer050 contactor design only GS configuration



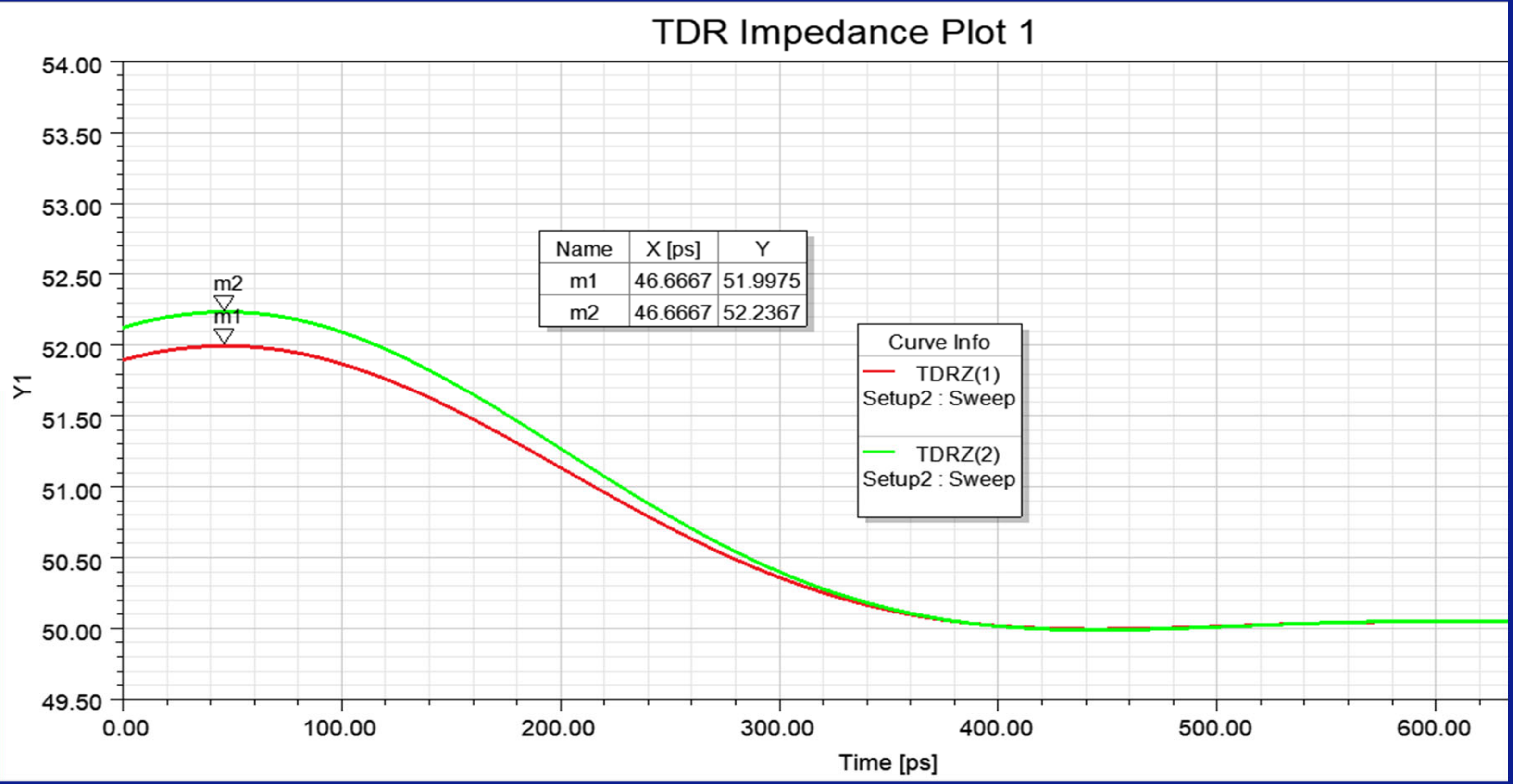
Port1 DUT side

Port2 BOARD Side

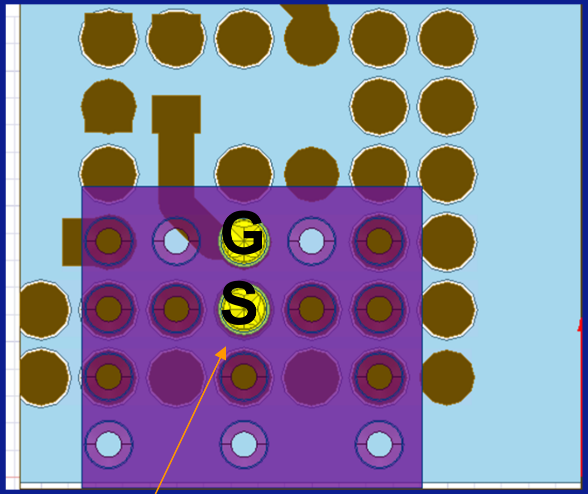
# S-Parameters; Port 1 is DUT side; Port 2 is Board side contactor only



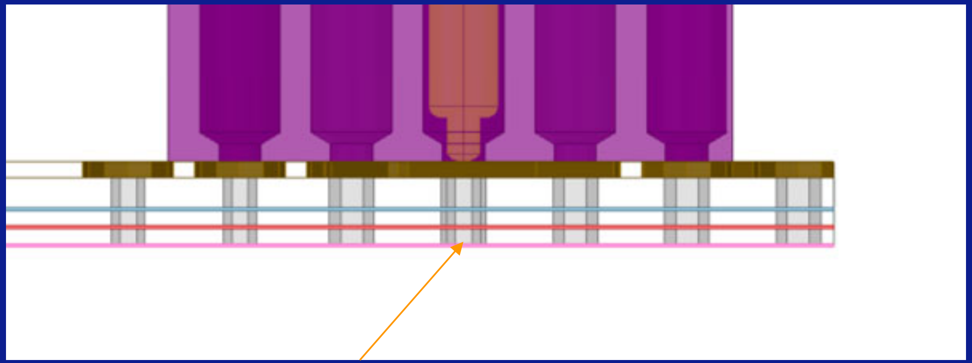
# TDR Port 1 is DUT side; Port 2 is Board side
# 3GHz contactor only



# Simulation – Example System simulation contactor plus PCB in GS configuration NO FAP




Port 1 DUT side



Port 2 BOARD side

Contactor plus PCB

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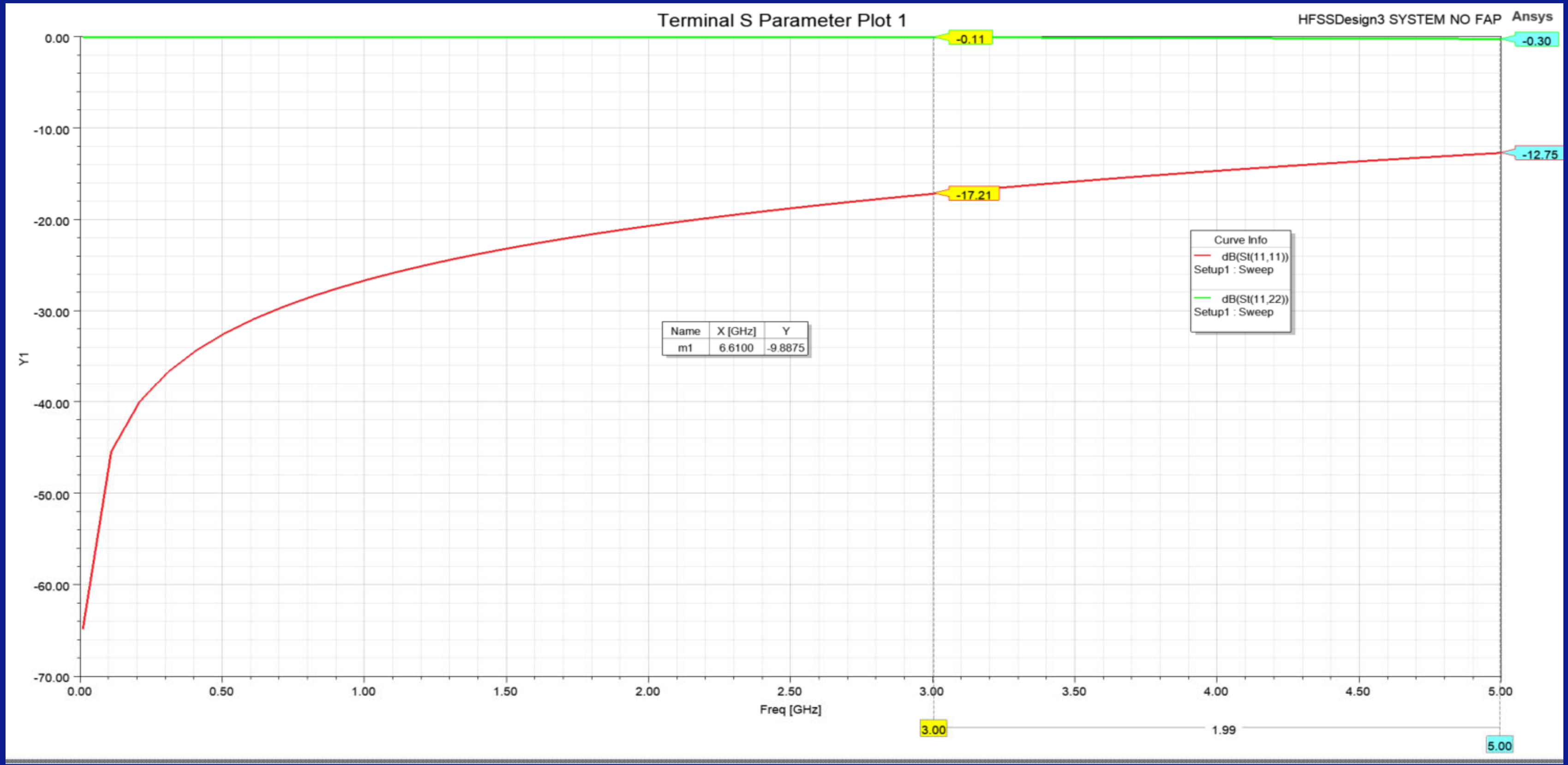
# S-Parameters; Port 1 is DUT side; Port 2 is Board side NO FAP



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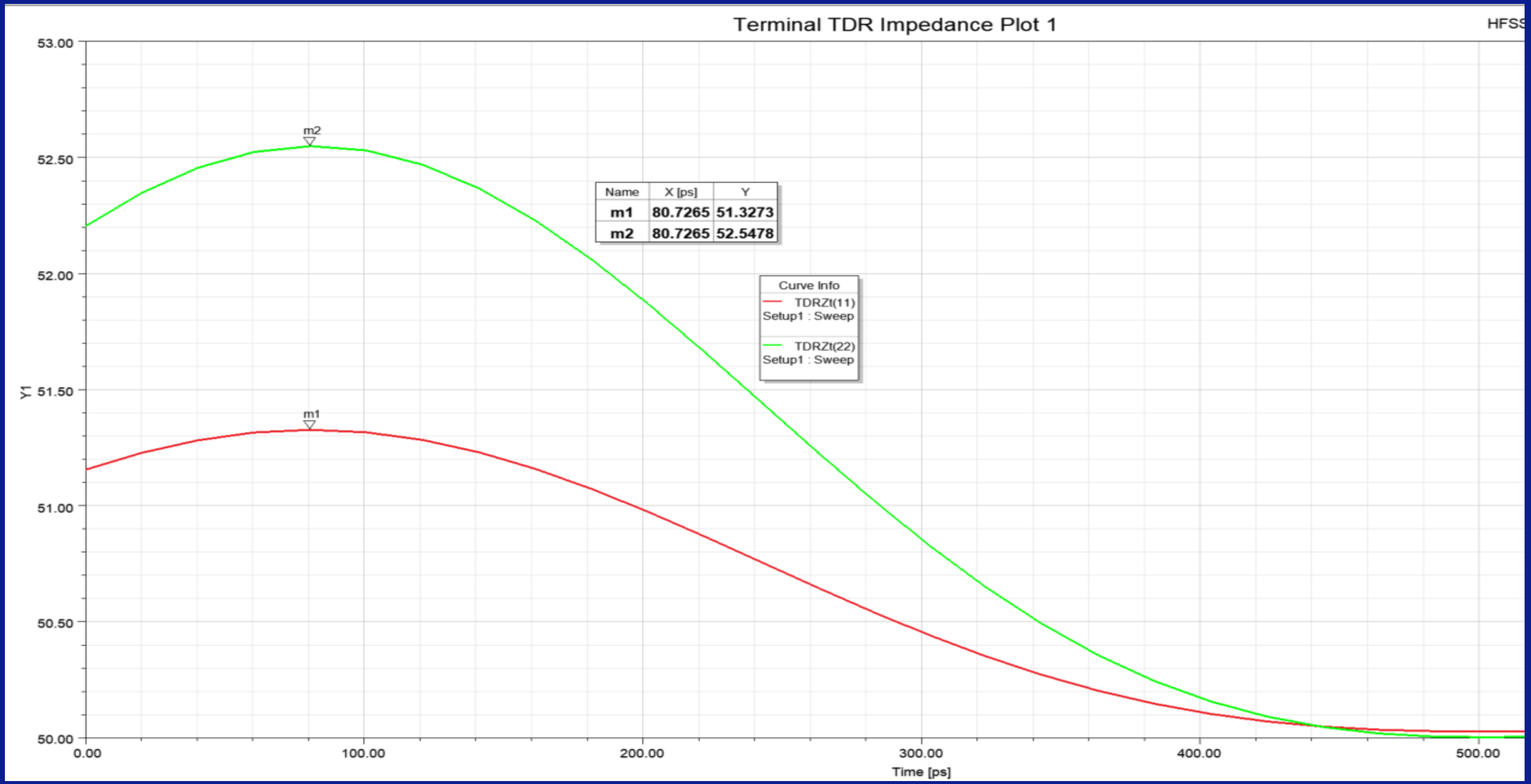
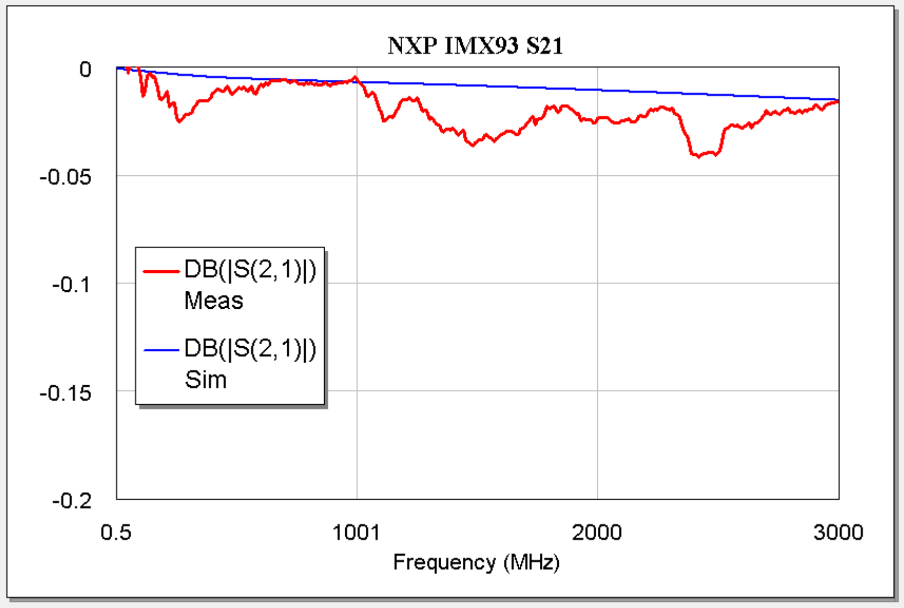
# TDR Port 1 is DUT side; Port 2 is Board side 3GHz NO FAP

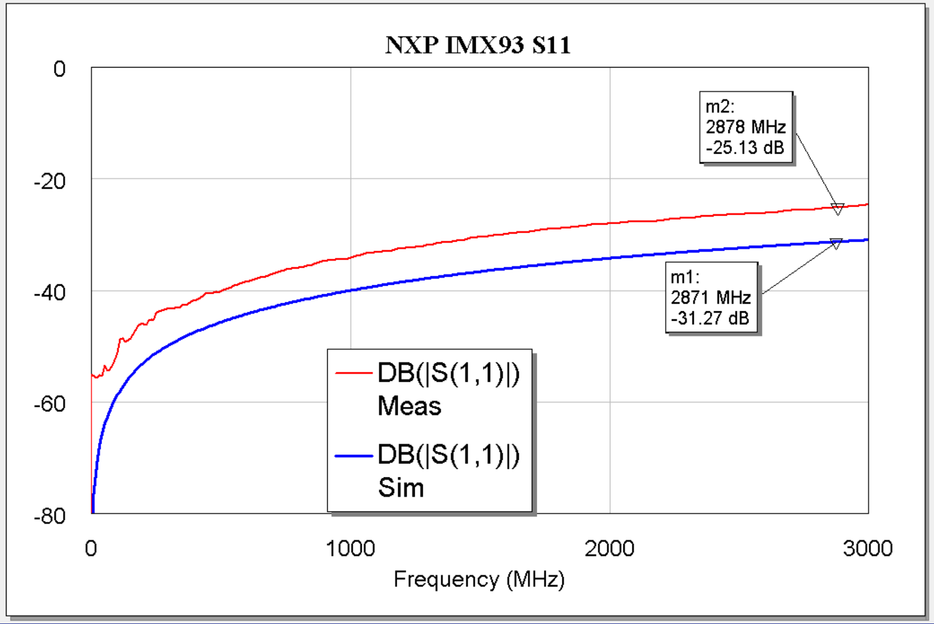



| Name | X [ps] | Y |
|---|---|---|
| m1 | 80.7265 | 51.3273 |
| m2 | 80.7265 | 52.5478 |

# Correlation results S-Parameters

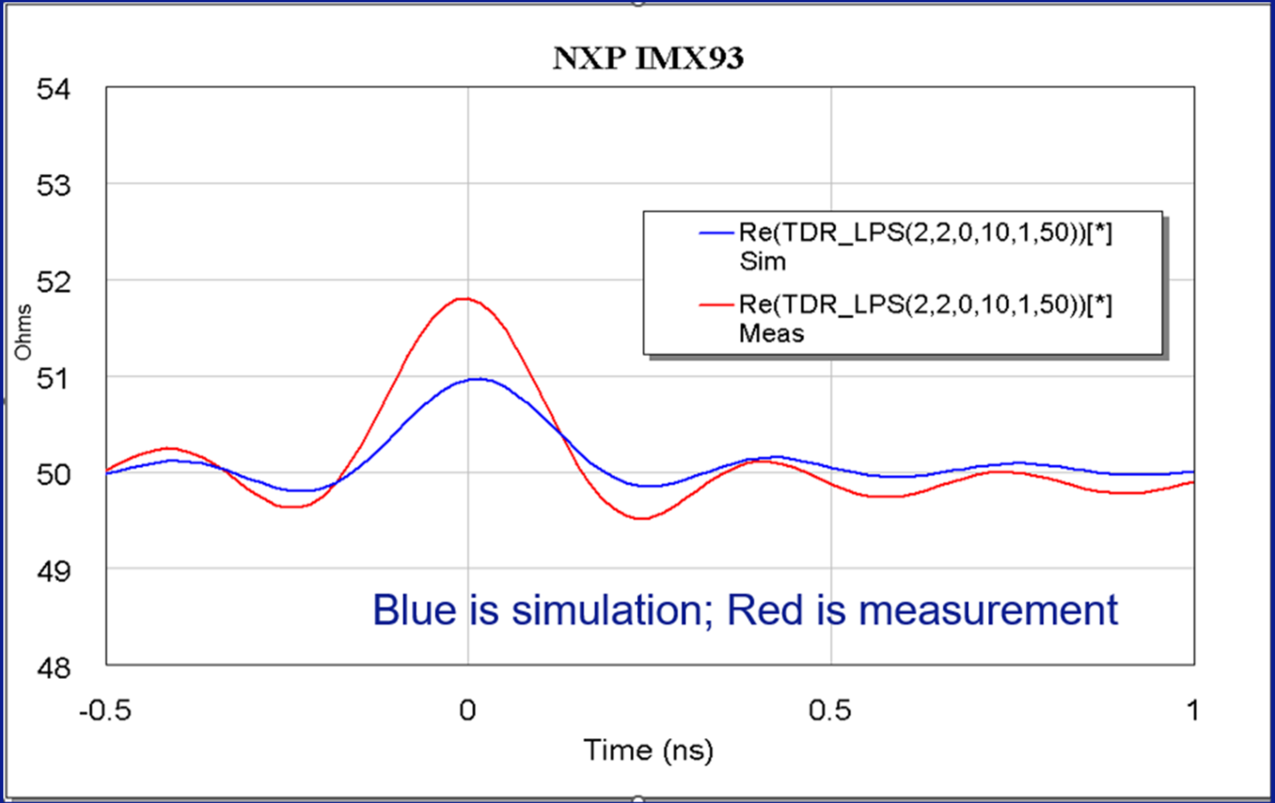
## Blue is simulation; Red is measurement




Contactor plus PCB

# Correlation results TDR Port 1 is DUT side; Port 2 is Board side 3GHz contactor only



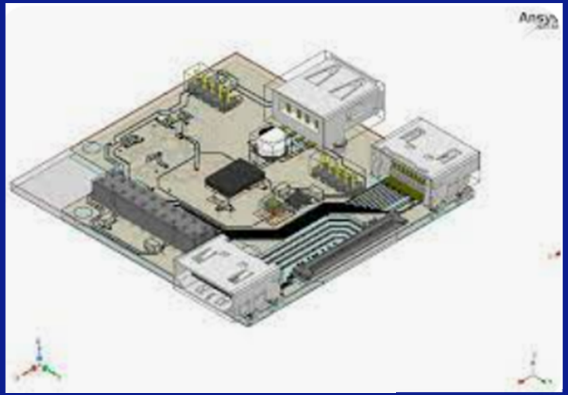

Contactor plus PCB

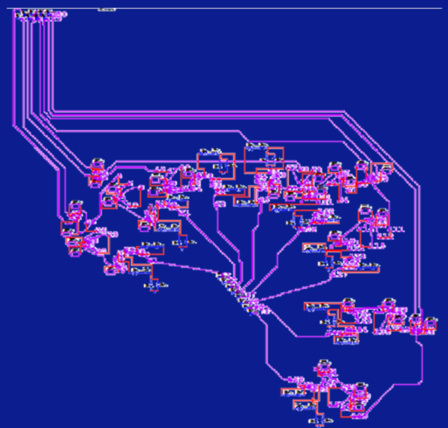
# Simulation

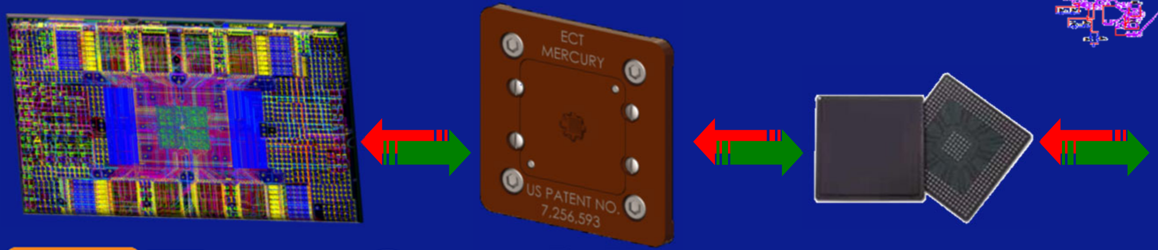
Simulation must be accurate to be useful

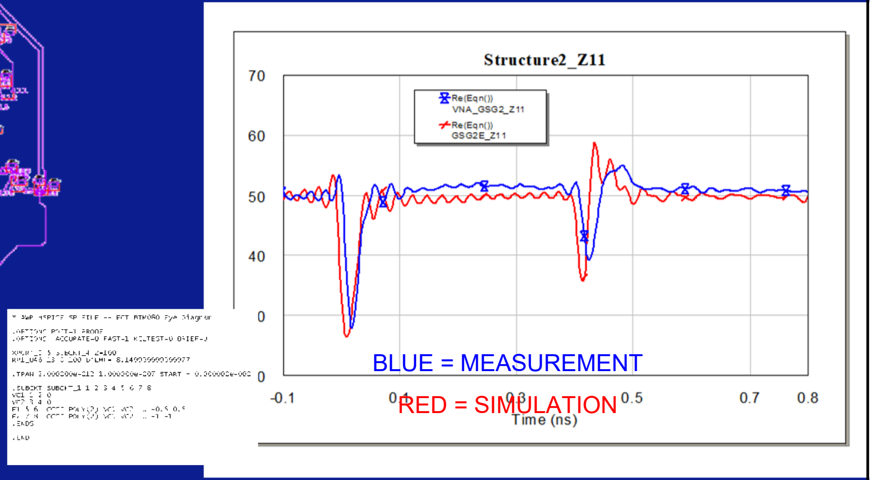
Fully integrated Test Solutions are optimized with Simulation

NI AWR Design Environment™



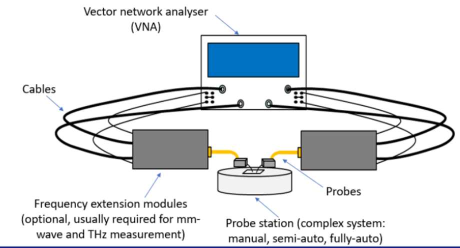




# VNA Characterization

- Vector Network Analyzer
  - Measures S parameters: Insertion Loss, Return Loss, Crosstalk
  - 4 ports required for differential measurements
  - Time Domain option for impedance analysis, eye diagrams




- Why VNA Measurement?
  - VNAs are exceptionally accurate and repeatable instruments when you implement proper measurement techniques and user calibration
  - Accurate measurement helps you correlate to the simulation
  - measurements provide the confidence to make performance/cost decisions
  - Test vehicles can be created quickly and easily by confirming model accuracy

# VNA Characterization

- Prepare
  - Place VNA in a stable environment and warm up VNA for proper amount of time at least 30 minutes
  - Use high-quality adaptors, cables, and torque wrenches
  - Check that all connections are clean and undamaged, use connectors lint-free swab to moisten with isopropyl alcohol
- Check
  - Set the VNA frequencies, IF bandwidth, power, and other parameters
  - Ensure that the calibration standards and device under test connect properly to the VNA
  - Plan for any special accommodations such as non-insertable devices and the loading of calibration kit definitions

# VNA Characterization

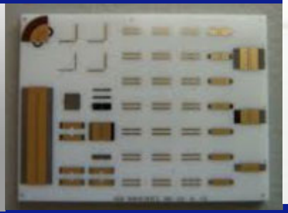
- Calibrate
  - Remove the device under test and calibrate the VNA by stepping through the calibration procedure
  - Verify that the calibration is good and store the instrument state and calibration
- Perform
  - Connect the DUT (device under test)
  - Make the measurements and extract the S-parameters

# VNA Characterization and calibration

- ❑ Stability of the system and good planarity setup to ensure repeatability of measurement

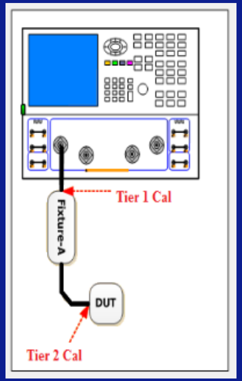
- ❑ Good calibration and verification
  - Electronic Calibration (ECAL)
  - SOLT Short Open Load Thru
  - SOLR Short Open Load Reciprocal
  - LRM Line Reflect Match
  - LRRM Line Reflect Reflect Match
  - TRL Thru Reflect Line

Ecal



Calibration Substrate

Calibration Kit



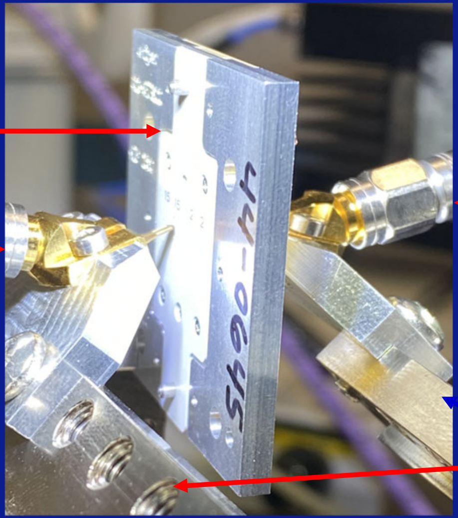

❑ Correction methods
- •CPM (Cal Plane Manager)
- •Mixed Cal
- •AFR (Automatic Fixture Removal)

# Testing setup Direct probing of the RF fixture

- Simulate probe + cross-section performance
- Optimize cross-section for best results
- Build test fixture using preferred cross-section to hold pins at test height
- Measure RF Insertion Loss (S21) and Return Loss (S11, S22) and correlate to simulation

Test fixture combining probes under test with optimized cross section

RF GSG test probes at required pitch



RF GSG test probes at required pitch

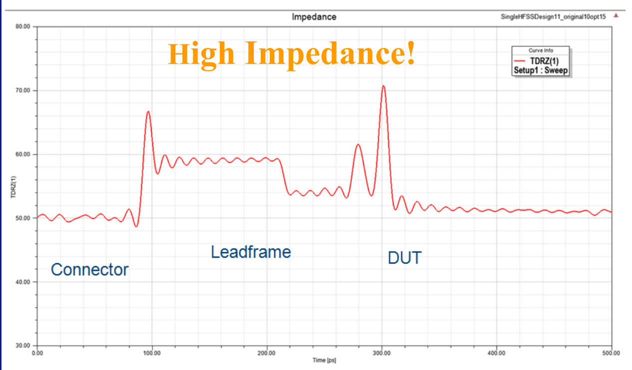
Mounting and alignment hardware

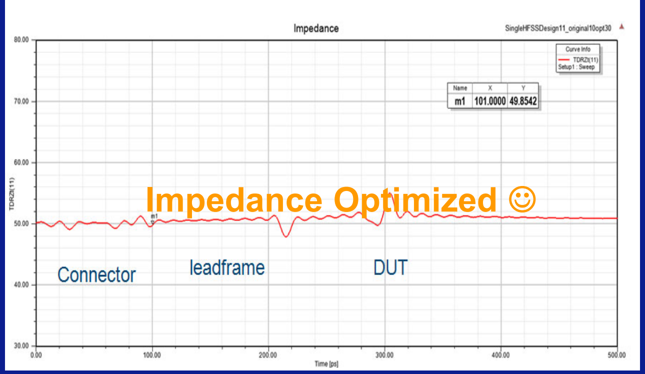
- **Port1: 0.5 mm probe =DUT Side**
- **Port2: PCB Side = Board Side**

# Simulation Challenges and Solutions

❑ **Problems**

--High impedance
-Voids in Substrate
-Discontinuities
-Tolerance
-Ground configuration
-Coupling




❑ **Solutions**

-Gap size optimized in coplanar waveguide
-Launch and transition optimized
-Port selection
-Ground slug
-Probe selection

# Conclusion

- High-speed design of semiconductor test interfaces is extremely challenging
- System simulation capabilities and measurement correlation are essential to provide test interfaces optimized for any customer application