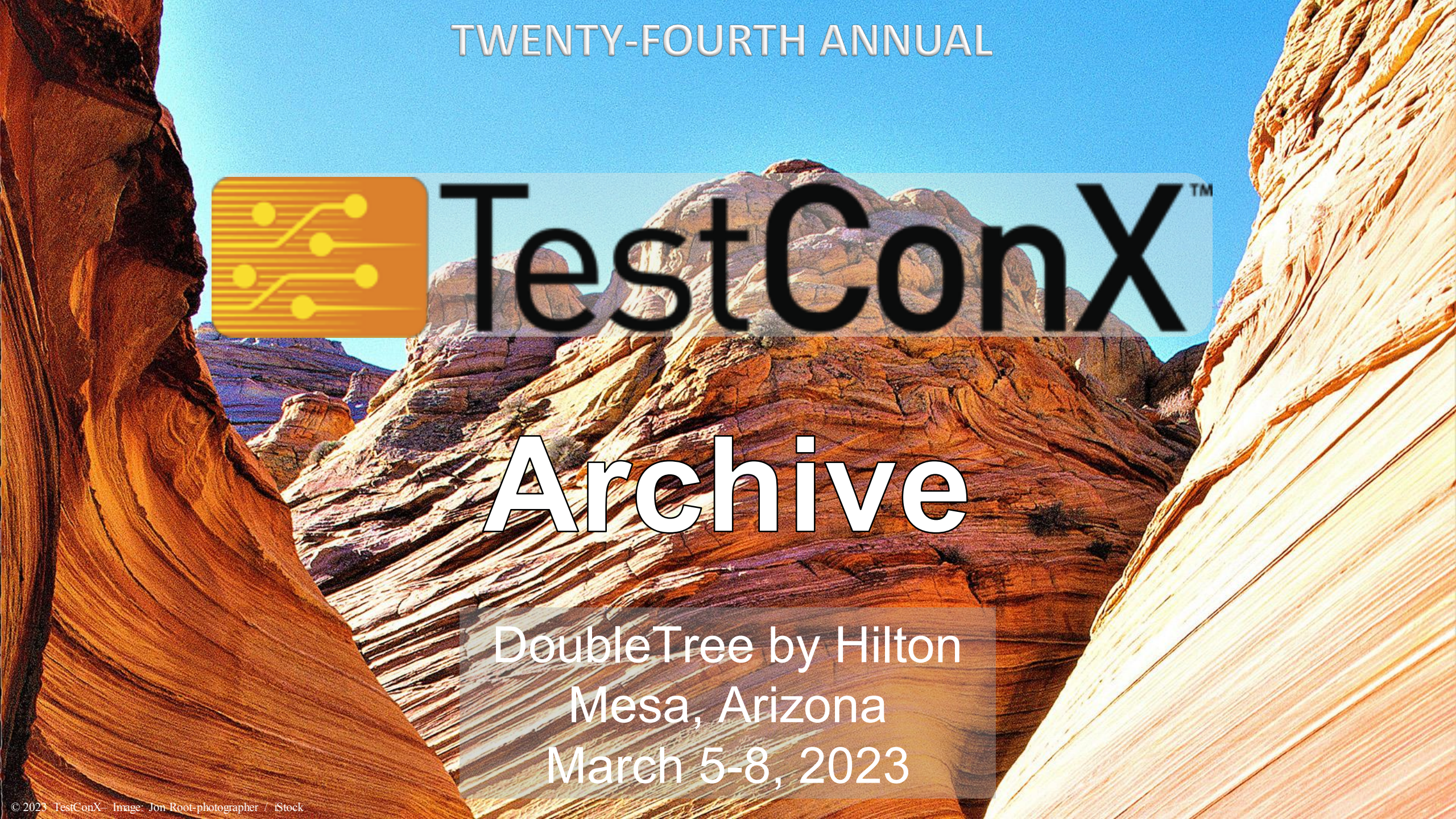

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Portable Stimulus Test Development and Execution on ATE Systems

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Mesa, Arizona • March 5–8, 2023

Agenda

- Motivation - Why do we need a new type of methodology on ATE Systems?
- Next generation ATE system
- PSS test case generation
- PSS Test Case Execution on ATE
- Analysis and Debugging
- PSS Test Development in Action on DUT via ATE
- Conclusion

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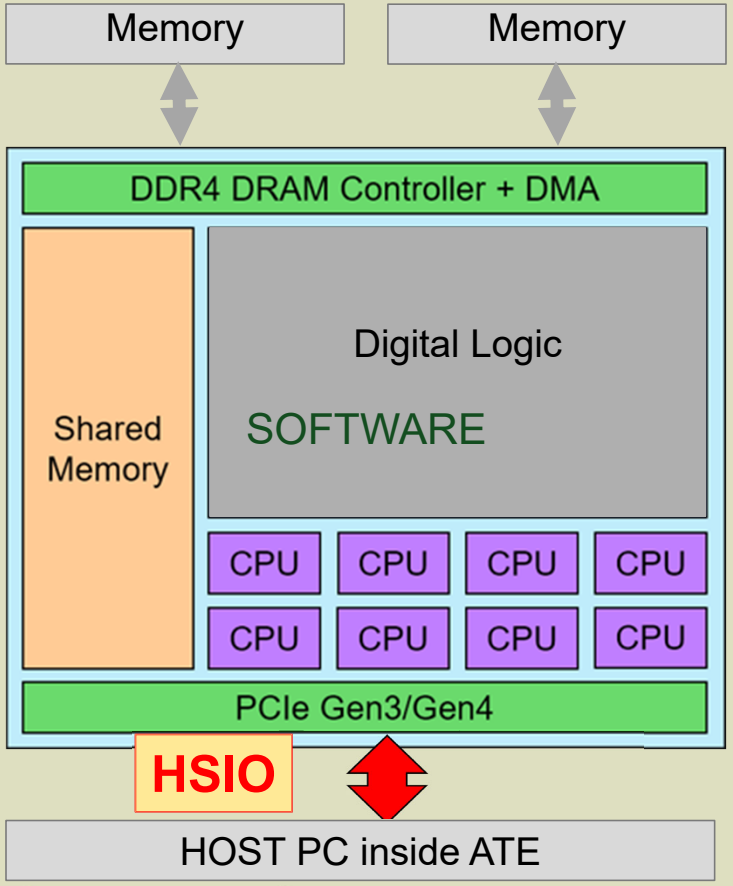
The Expanding Role of HSIO in Device Testing



Many devices today have HSIO interfaces on them.

External loopback testing of HSIO is wasteful:

- It does little confirm test margins.
- It delays testing of HSIO enumeration until SLT causing nearly completed parts to be scraped.
- It thwarts a high-speed path into the DUT to perform other testing – forcing used of inferior interfaces.

Using the HSIO interface in its native way, three different types of tests are possible:

- **SW-based, bare-metal functional test (PSS Enabled)**
- **SLT-Like functional testing on ATE (Shift Left)**
- **Scan-over-HSIO**

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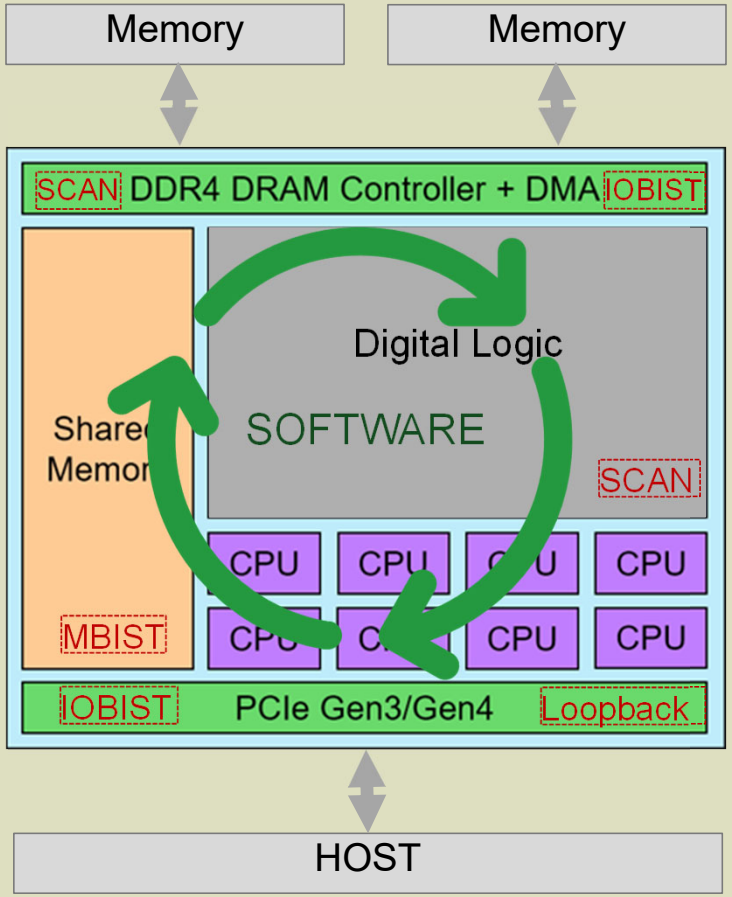
MOTIVATION

SW-BASED, BARE-METAL FUNCTIONAL TEST (PSS)

Need to Re-invent Functional Testing on Production ATE



Complex devices have many cores

- They work together in the application
- They do not work together on the tester
- SCAN, BIST etc. are core-based tests

Good defect coverage of the cores, but:

- Device software is not part of the test
- No interaction between the cores and host

⇒ Test Coverage Gap for functional mode

How to close this gap ?

- Complex functional test cases across cores
- System-like interaction with the external Host
- Software – Device Firmware and Host SW

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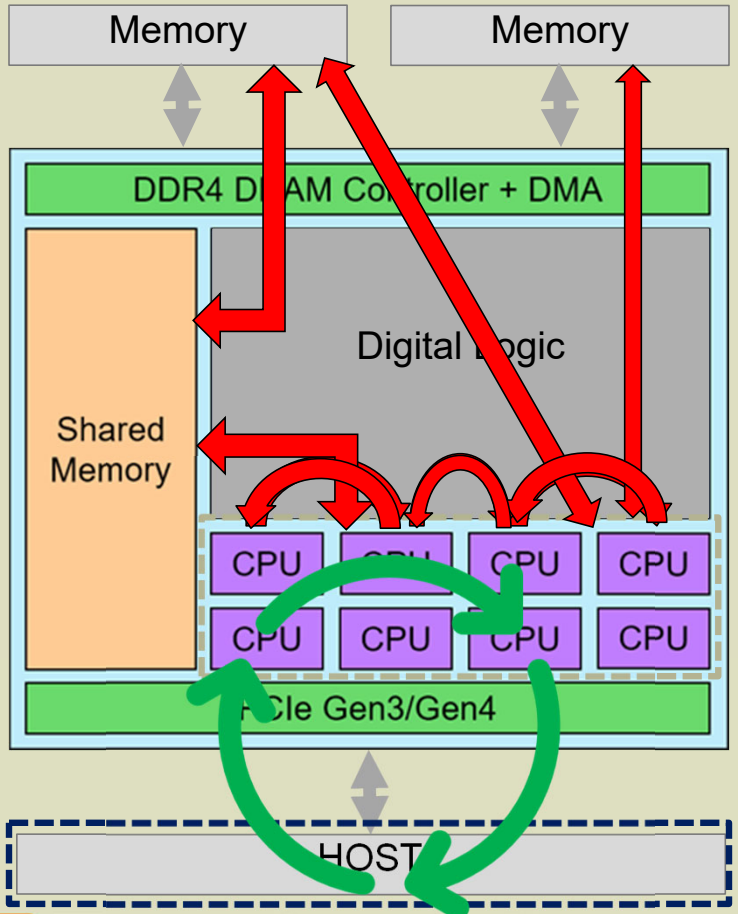
Software-Based Functional Test Closes the Coverage Gap



Software for a real functional test is

(1) Device firmware which runs on the DUT

(2) Supporting software which runs on the HOST

Both need to work together for full operation

(1) Device firmware

- Enables functional operation
- Drives interaction of cores and host
- Typically booted from the host

(2) HOST software

- Operating system with custom drivers
- User application software

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Software-Driven Functional Test: The Big Picture

Forward flow – systematic approach for predictable TTM and TTQ

Leverage pre-silicon test content & methodology:

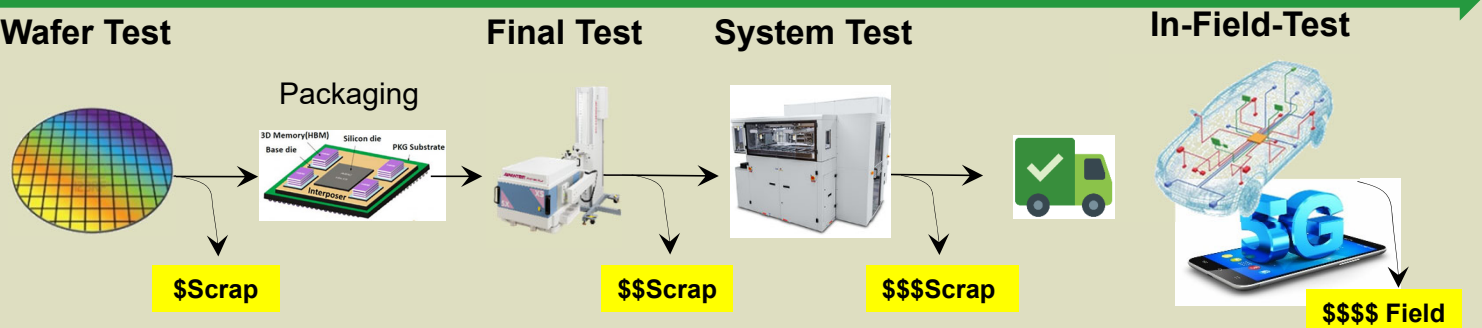
- Software test cases from EDA (i.e., Cadence)
- Example format: PSS (portable stimulus)

Bring-up & debug of full software stack ON WAFER

- Boot device, run (modified) application software
- Use standard debug tools (i.e., Lauterbach)

EDA flow (PSS) cadence

Emb. SW Debug in PSV / ATE LAUTERBACH DEVELOPMENT TOOLS



ATE & SLT with functional access over PCIe / USB

Backward flow – if required due to excessive SLT yield-loss and field returns

Add test coverage as early as possible:

- Targeted “Bare Metal” (no OS) tests
- Sub-set of system level test cases

Diagnose SLT and field returns:

- Correlation between different insertions now possible
- Example: structural / functional (SCAN vs SW-based)

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APPROACH - NEXT GENERATION ATE SYSTEM

BOOTING AND EXECUTING PORTABLE STIMULUS STANDARD BASED FUNCTIONAL TESTS ON AN ATE (AUTOMATED TEST EQUIPMENT) SYSTEM

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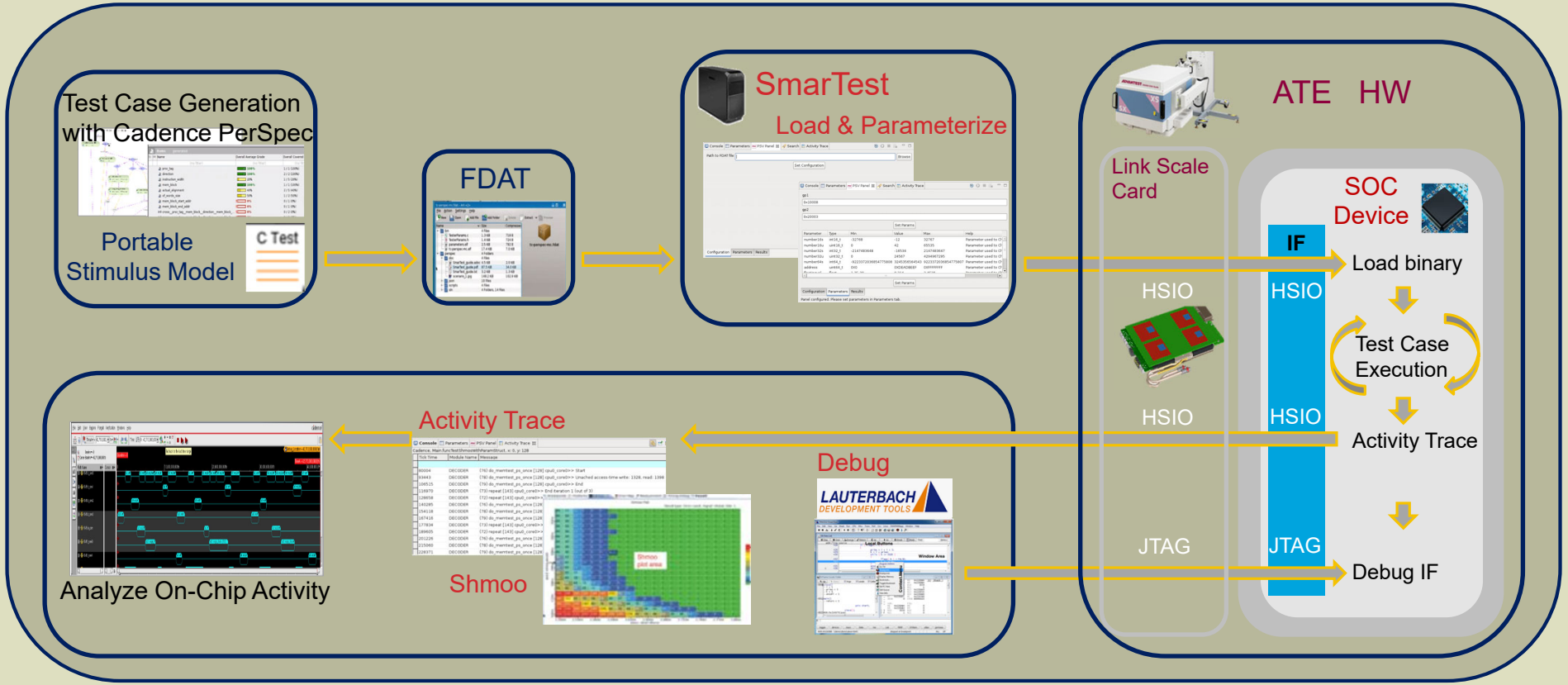
Full Integrated Functional PSS Driven SoC Validation Flow



PSS Model Overview

Portable Stimulus Standard (PSS) defined accellera standard

▪ Platform	platform independent description of test scenario intend for improved re-use
▪ User	abstract modelling of test intention to create valid use cases / scenarios
▪ Software	functional software driven approach for SoC verification, validation and testing

PSS Tooling

▪ Language	supporting accellera standard
▪ Test Case Creation	create valid test cases with constraint-random capabilities out of the PSS model
▪ Coverage	enable coverage of complex SoC beyond individual blocks
▪ Portability	powerful test generation engines creating test cases e.g. for UVM or embedded test use cases

Multiple aspects to consider planning the PSS model

– Framework	user / compiler, toolchains / available HW / internal policies / debug / model maintenance
– Message	output handling (fast-messages concept) – interface (streaming/dump required to be clarified)
– Functional add-ons	(cache coherency, stress tests, power modeling) compared to pure traditional testing
– Technology library	integration e.g. coherency, power … and more
– Post-Si control knobs	for tester infrastructure to enable variants of functional behavior
– Peripheral control	combinations of external physical and internal functional parameters
– Coverage	metric introduction – generation time coverage and runtime-coverage addons
– Documentation	of model and use instructions
– Regression	preparation/setup and execution
– Statistical	data collection preparation – alignment with messaging

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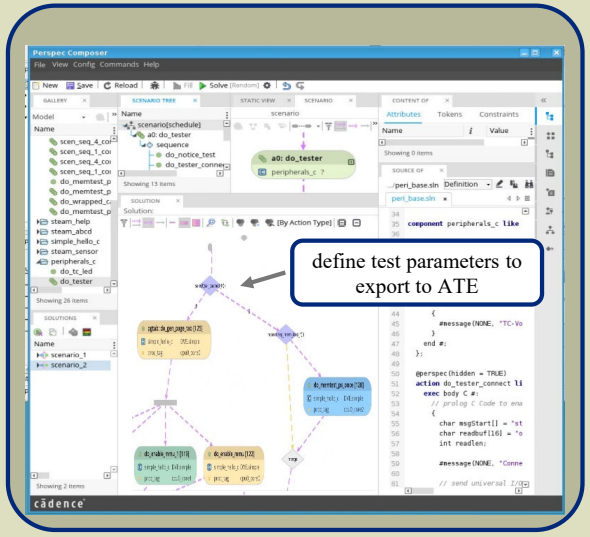
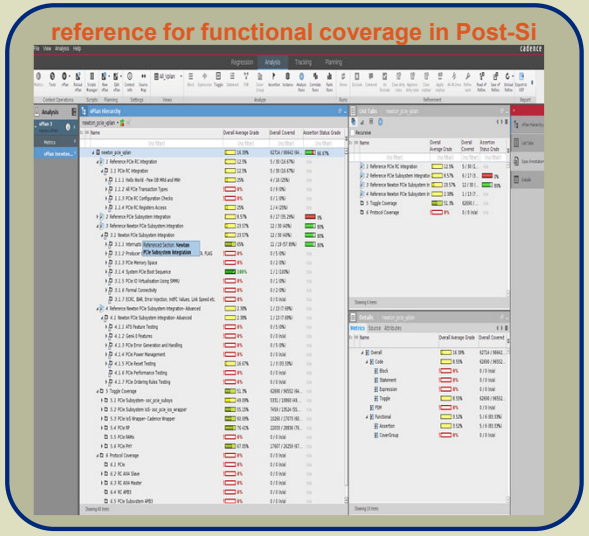
Interactive Approach - PSS Model Controls Post-Silicon

- **PSS model: operator-based control infrastructure will be provided for post-si**
  - Typical control knobs: address, iteration counts, un/cache decisions … and more
  - Could be simple value deployment or complex conditional statements (runtime)

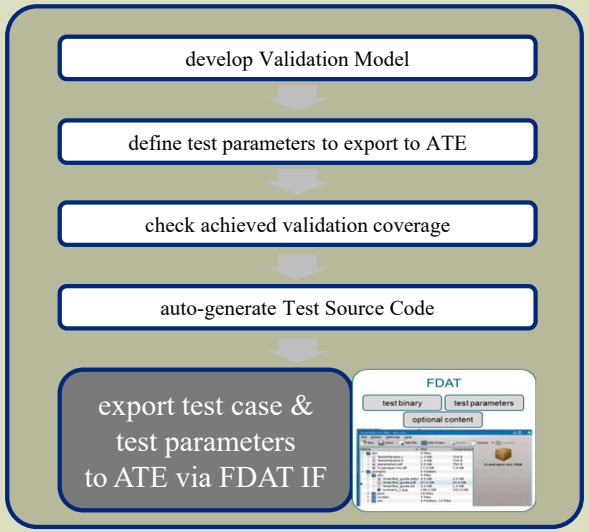
PSS model developed in PSS tool



Coverage Metric gen-time or runtime



Workflow in PSS tooling



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Key Capabilities of The New ATE Instrument

What is needed ?

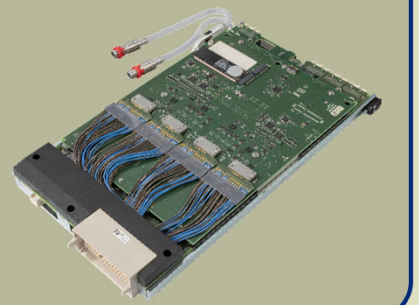
- Functional HSIO support
- Local processing power (Host)
- Enough local memory
- HW integrated in the test head
- Open SW environment

Target capabilities

- USB / PCIe full protocol stack
- Host processor for local processing
- Local memory for test data
- Multi-site capable
- Fully integrated

„Link Scale USB“

„Link Scale PCIe“



V93000 Smart Scale
V93000 EXA Scale

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APPROACH – PSS TEST CASE GENERATION

LEVERAGING POWERFUL TEST CONTENT FROM SILICON VALIDATION

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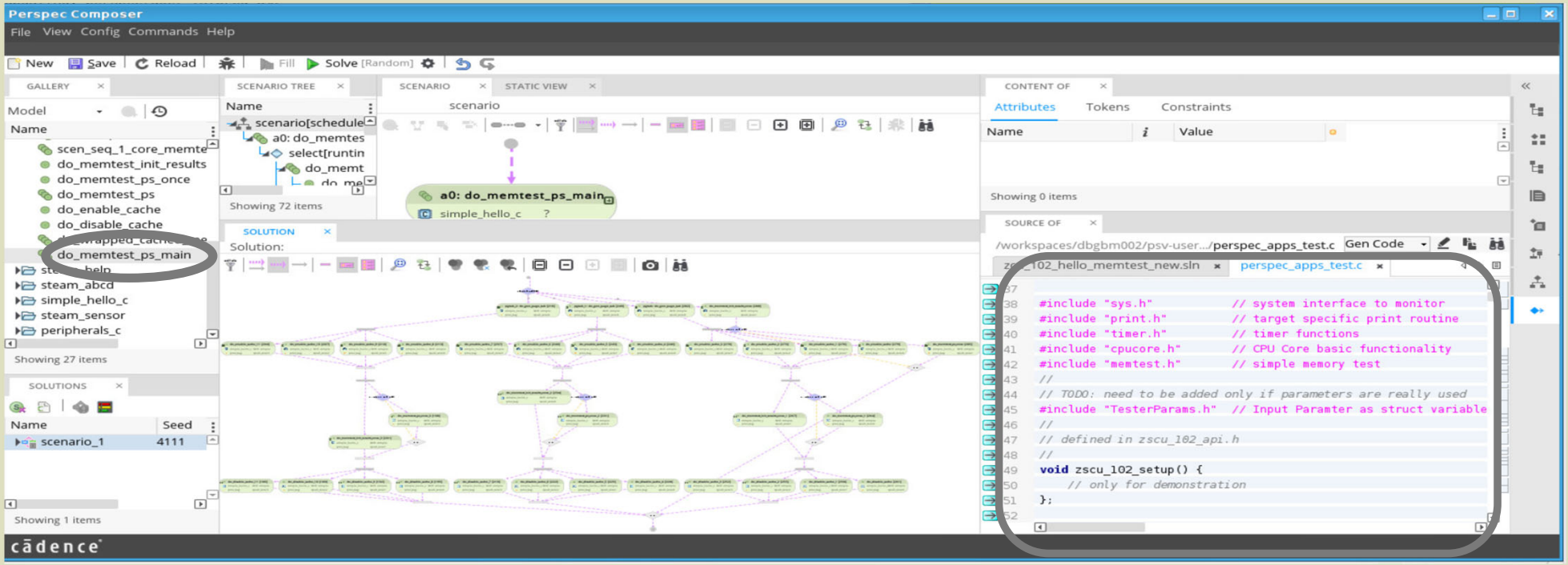
Portable Stimulus Standard with Cadence Perspec System Verifier



Test intent – captured in abstract PSS model (library) already
C-Code (instrumented for Post-Si) – generated in batch/gui mode

APPROACH – PSS TEST CASE EXECUTION ON ATE

A SMARTEST PLUG-IN FOR PSS TEST CASE EXECUTION AND RESULT RETRIEVAL

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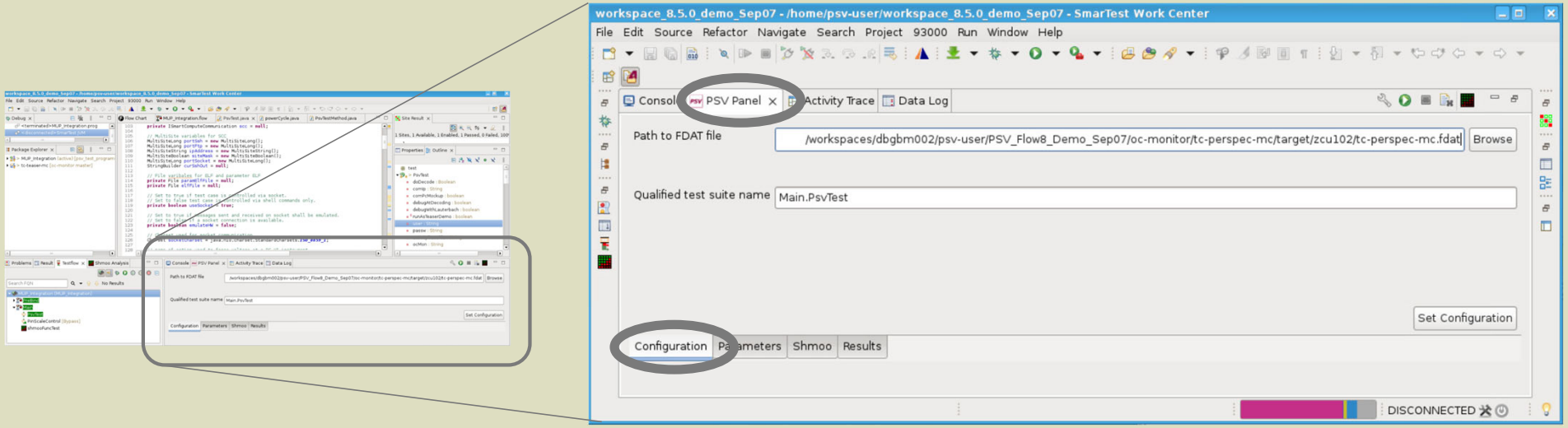
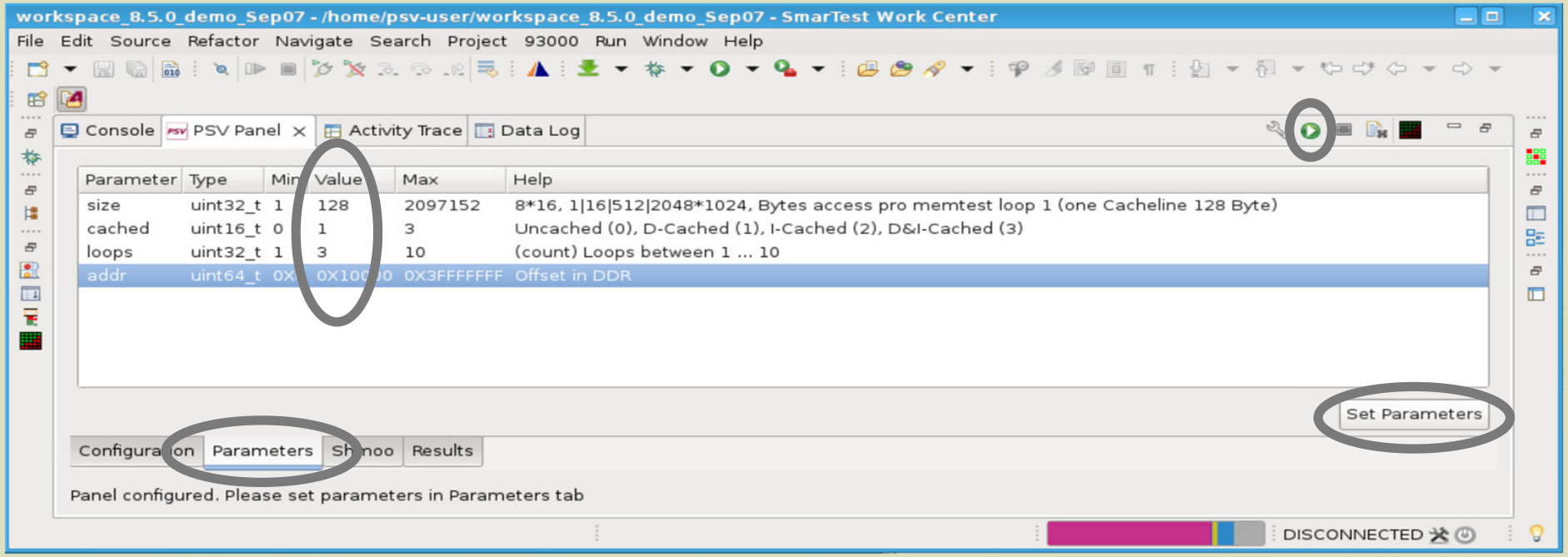
Test Control Panel as Prototype Plugin



No Pattern conversion anymore – instead, use of FDAT that contains PSS test case executable.

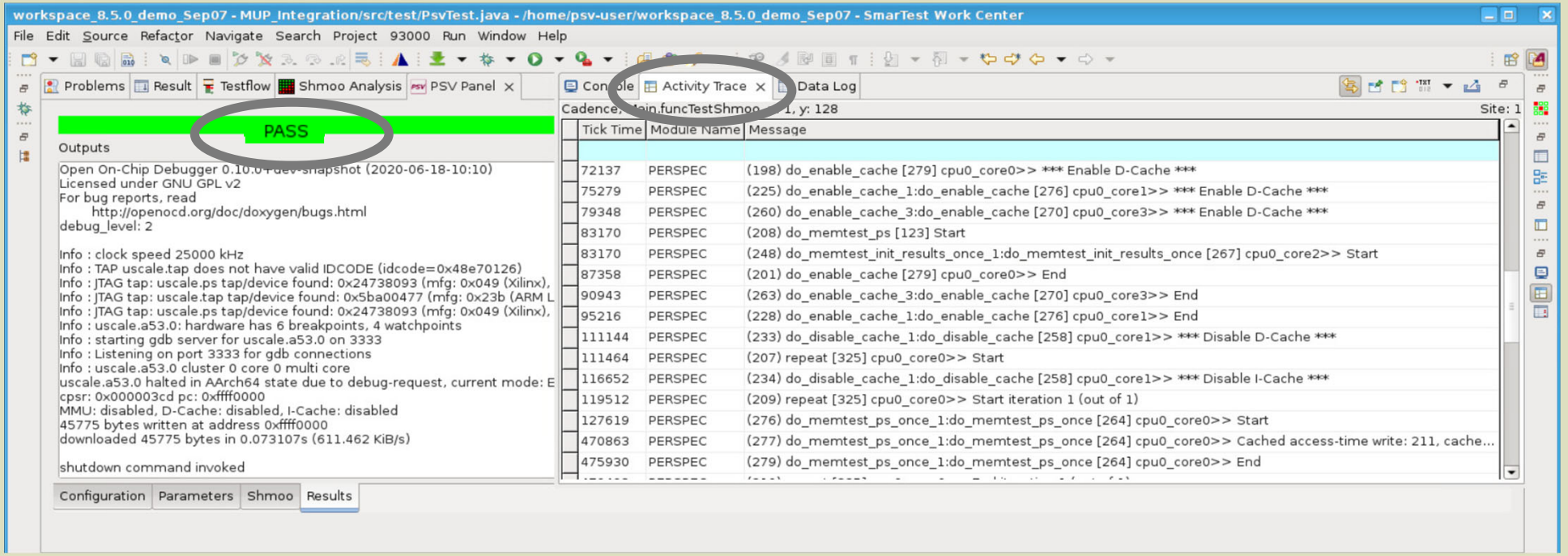
Simplified GUI, for test case handling and execution of FDAT content.

Dynamic Parameter Passing to Test Case



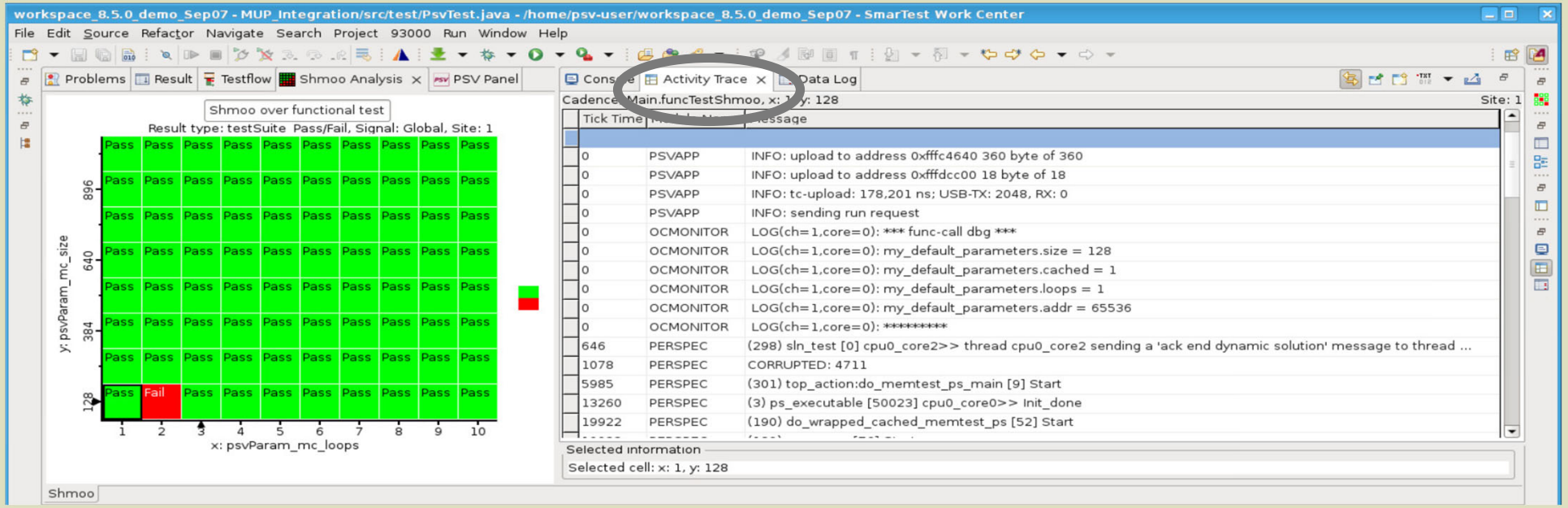
On the fly parameter modification and execution without test case re-compilation. PSS model was prepared accordingly.

Results and Activity Trace – Events Executed on DUT



Execution and high-speed download of PSS related result log. First level of debug.

Shmoo Results Over Parameter Variations



Fully featured Shmoo analysis tool.
Overview on DUT characteristic accross full parameter range with complete set of result logs.

Test case binary loaded only once, parameter exchange with each test execution.

APPROACH – ANALYSIS AND DEBUGGING

DIVING ONE LEVEL DEEPER

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First Analysis with Cadence Perspec Analyzer Environment

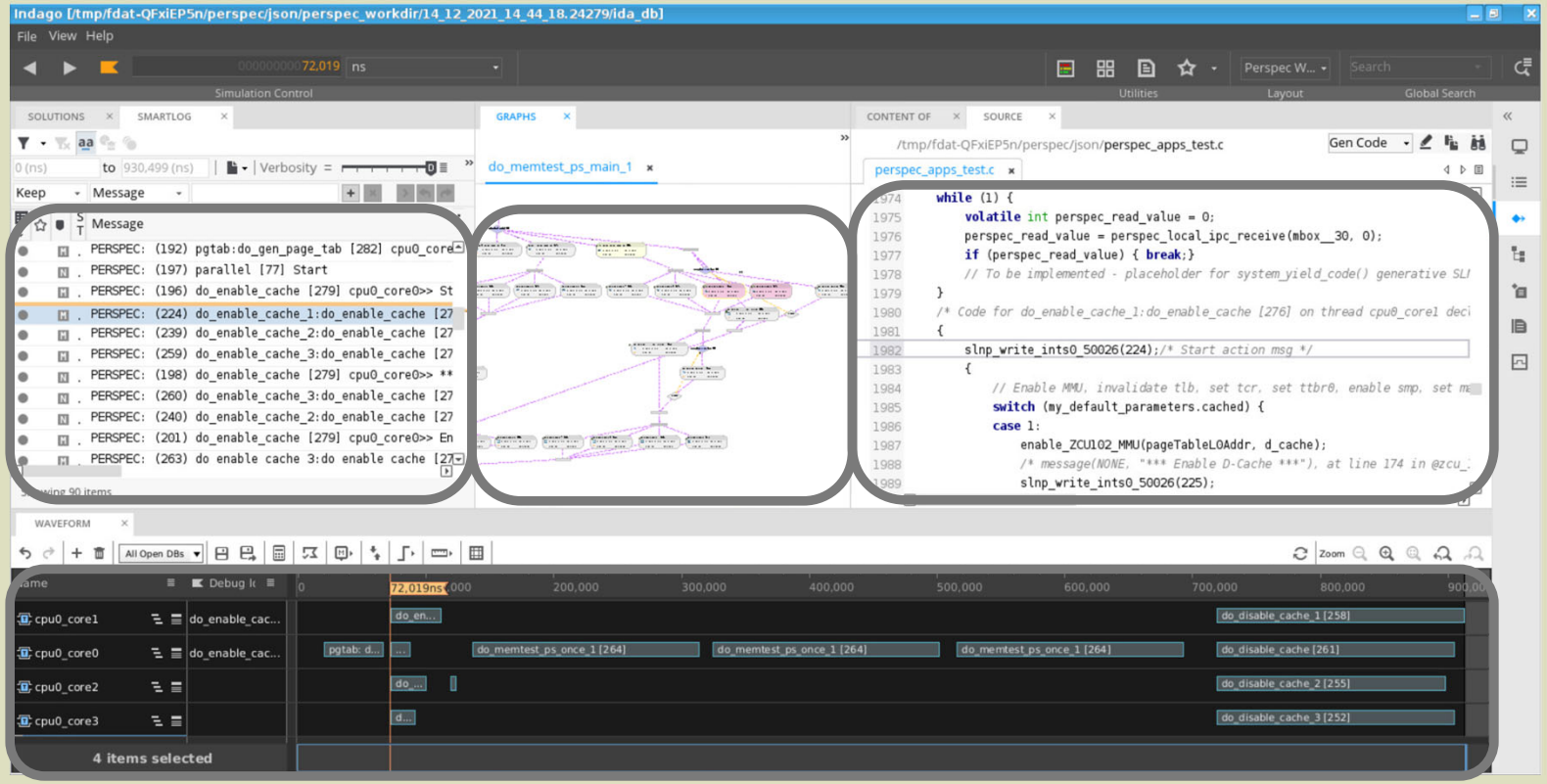
Post execution analysis:

Activity Trace

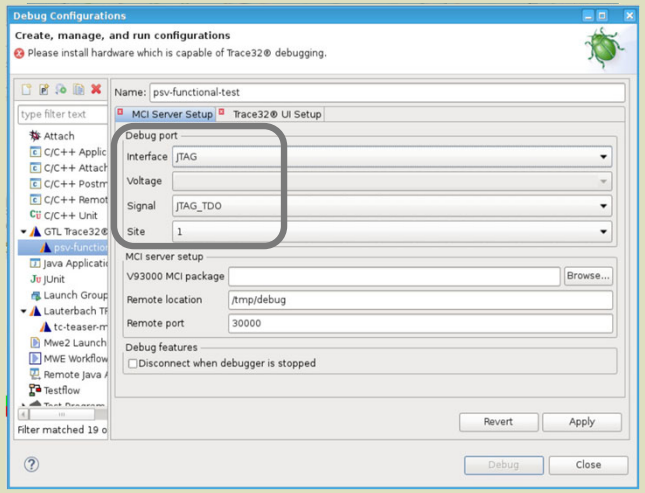
Test case model

C - Code

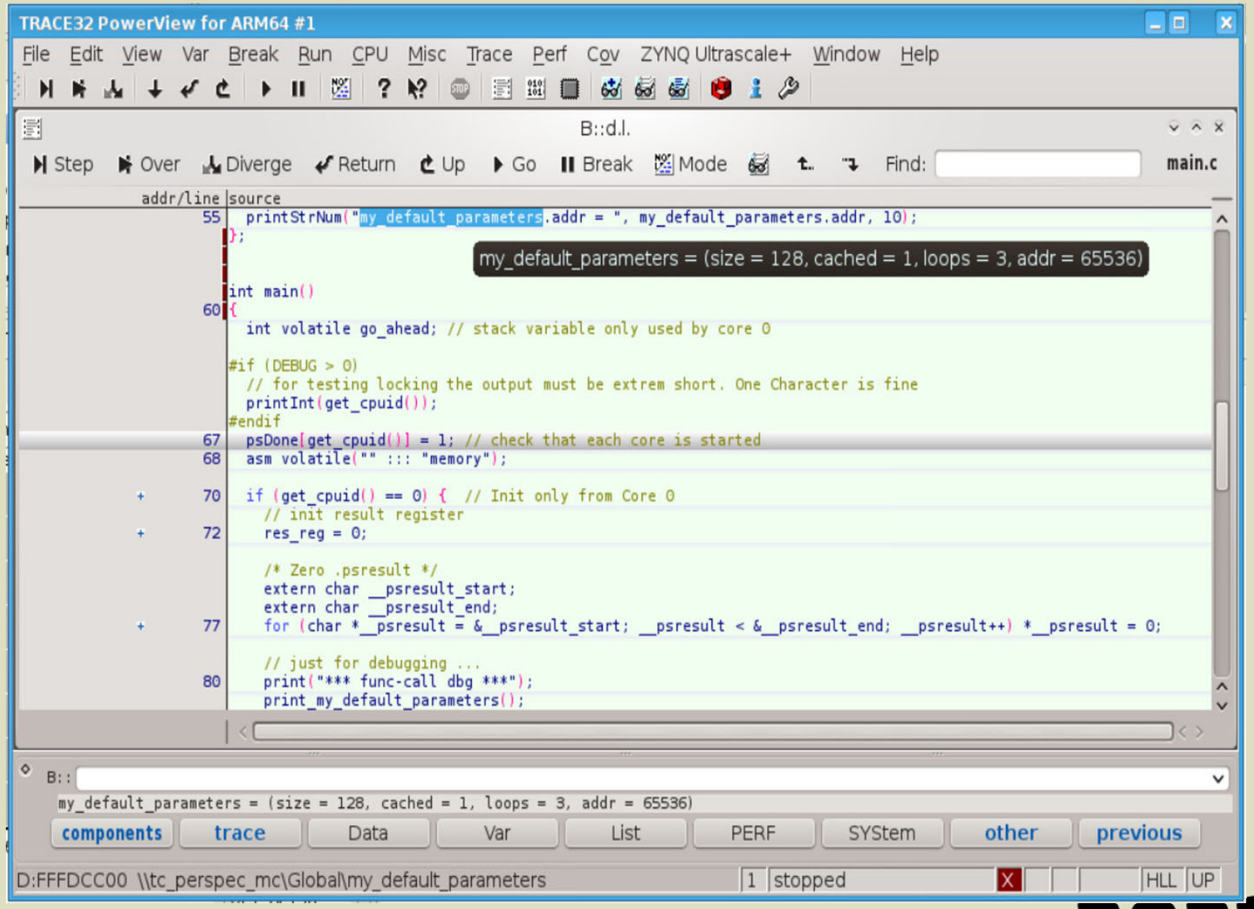
Activity over Time on multiple cores



Next Level of Debug – SW Debugger Configuration Panel



Integrated Lauterbach panel for instant and real time on target debugging



APPLICATION – PSS TEST DEVELOPMENT IN ACTION ON DUT VIA ATE

HW SETUP AND DUT VALIDATION CAPABILITIES

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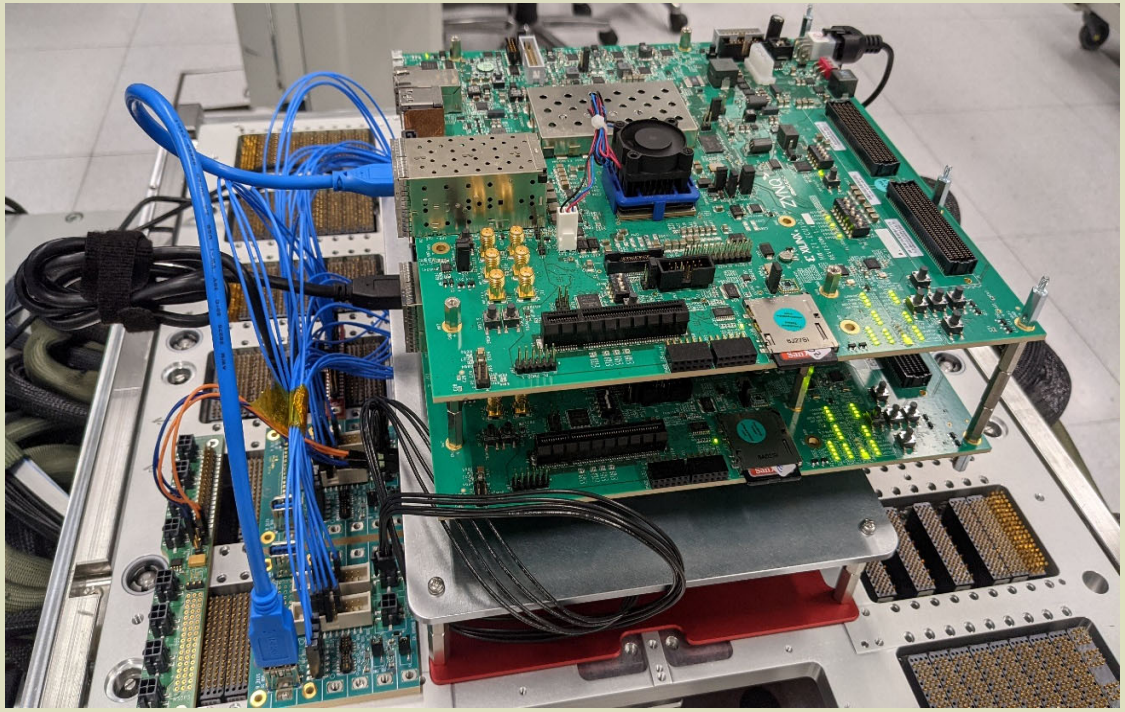
Functional Test Evaluation Setup

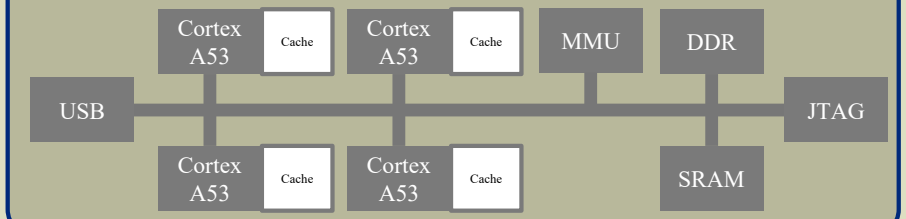
- Xilinx Eval Board as Validation Device on the V93000 tester
- HSIO connection to the Link Scale card in the test head
- Device boot and HSIO enumeration done by an image that is loaded via JTAG
- HSIO connection to exchange all test data (test case binary, parameter, results, traces, monitoring, …) with fallback possibility to JTAG
- Debug capability over JTAG



Application – validation results achieved with ARM based FPGA

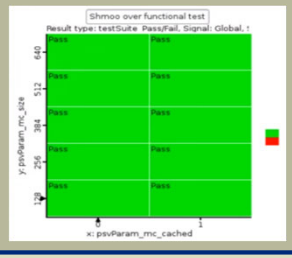
DUT: Xilinx Zynq-UltraScale+-MPSoC ZCU 102

FPGA: configuration used as DUT

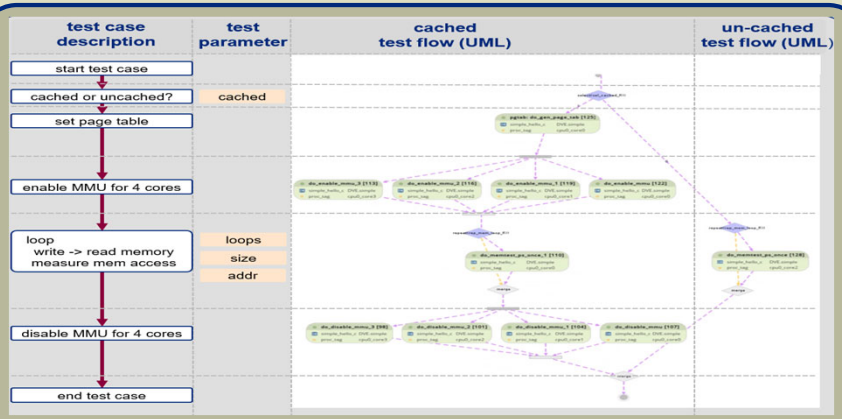


Shmoo: memory access size [byte] over cached / uncached

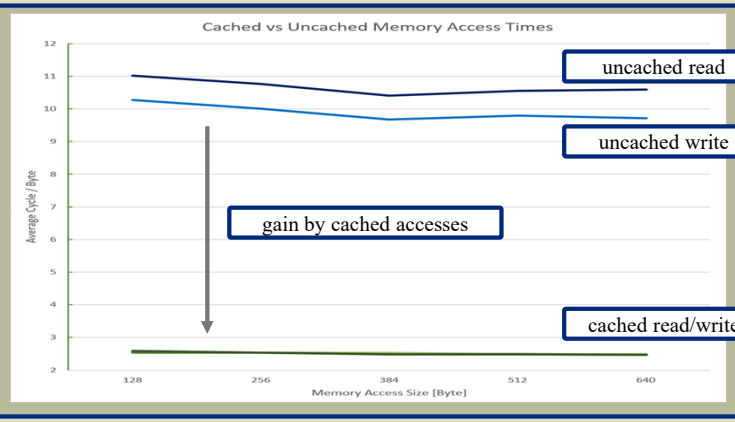
executed: multicore test scenario



Implemented multicore test scenario



Memory access times post-processed from Activity Trace



Complex Devices and Use Cases are supported

Parameter variation and automation supporting design evaluation

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CONCLUSION

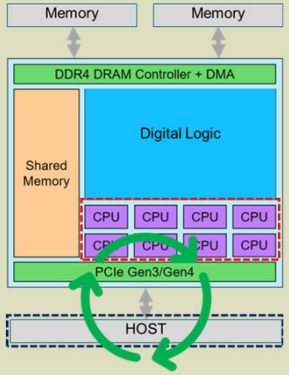
PORTABLE STIMULUS TEST DEVELOPMENT AND EXECUTION ON ATE SYSTEMS

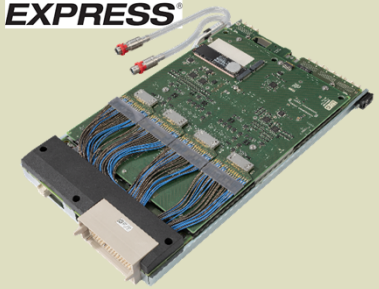
Conclusion

Link Scale cards enable new test methodologies

Software-based functional test

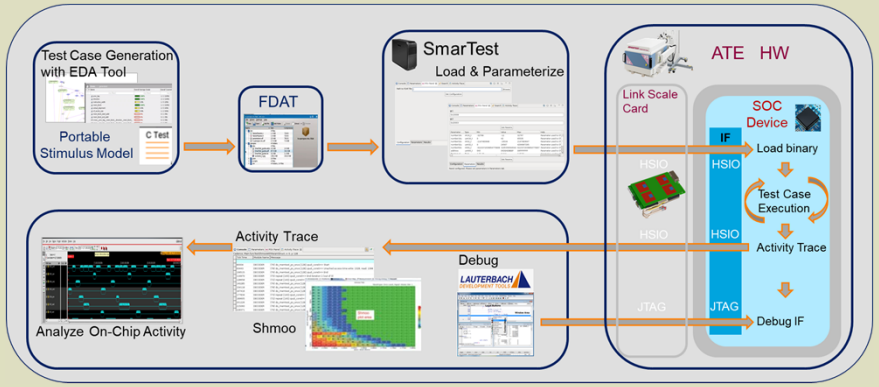
- Closing a test coverage gap
- Driving higher product quality
- Enabling known-good-die





Functional test generation with Perspec enables

- Fast turnaround time – from test case creation to execution and analysis in a matter of minutes
- No extra steps for file conversion
- Ease of test case execution
- Parameterization & Characterization
- Execution trace capture & evaluation in EDA



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