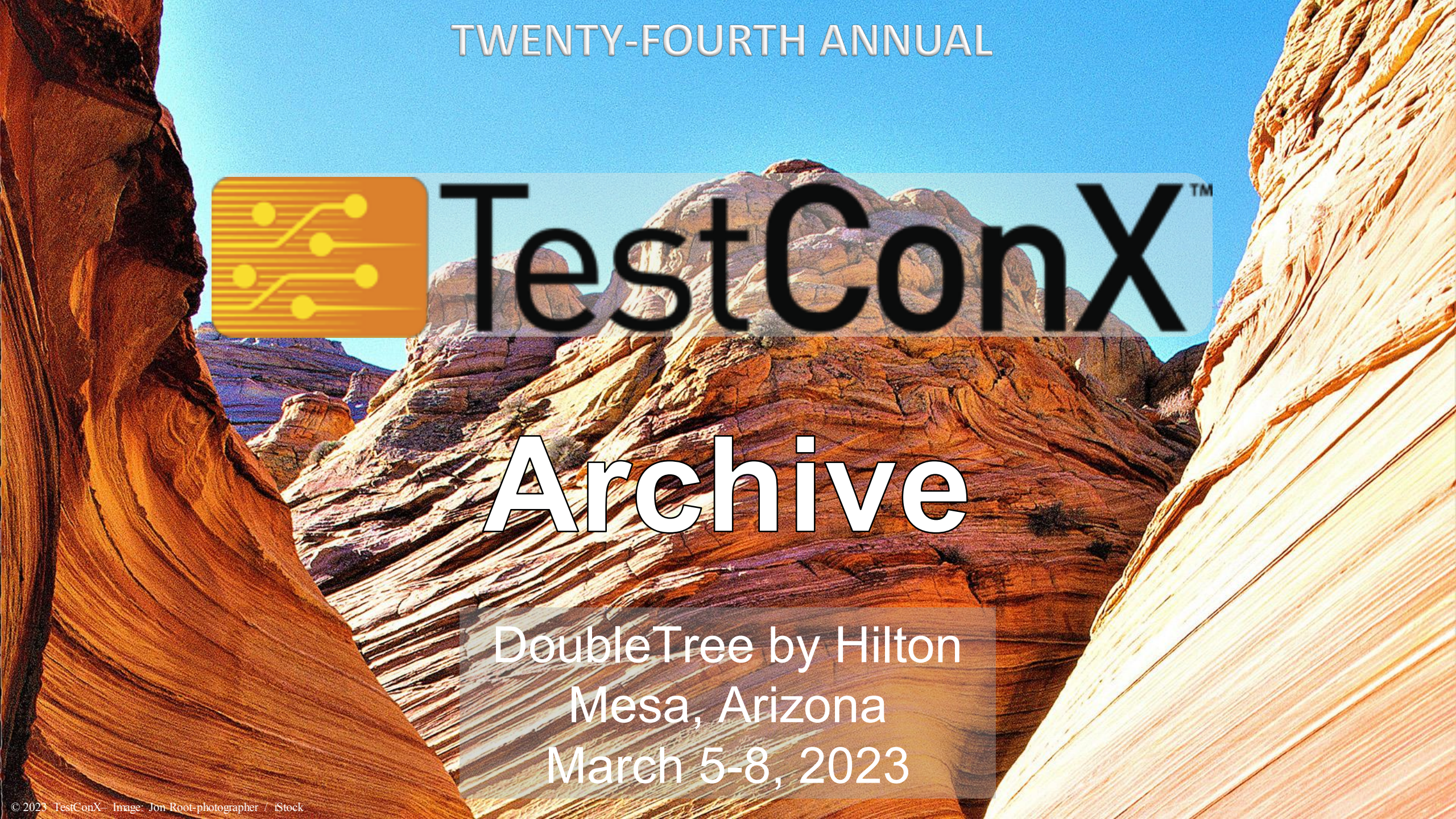

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Design for Stress

João F. F. Gonçalves
Infineon Technologies Germany AG

TestConX™

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Contents

- Trends in Automotive
- Design for Stress as a process
  - Main principles
  - Main target
  - In Infineon Development flows
- Design for Stress successes
  - Case Study
  - Summary

Trends in Automotive – "# of transistors & area"

1 Increasing # of semiconductors & complexity

Traditional <> Modern ICE

500 ~ 600 <> 1500 ~3000

~x2

Smart(er) EVs

Up to ~5000

Main Drivers:

- Infotainment
- Sensors (MCU, Power, Sensor, Connectivity)
- Memory (1 2 3)
- Autonomy
- Safety/Security
- Charging

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Trends in Automotive – "Mission Profiles"

2 Longer and more active Mission Profiles

Traditional <> Modern ICE

Typ: 10000h ~ 30000h Active

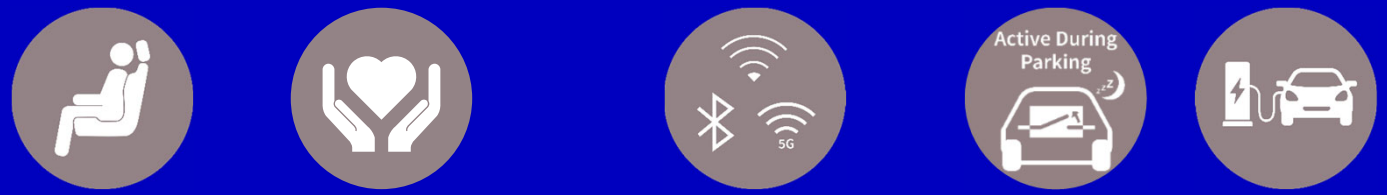
>x10

Smart(er) EVs

Up to 24/7 (~131.4kh)

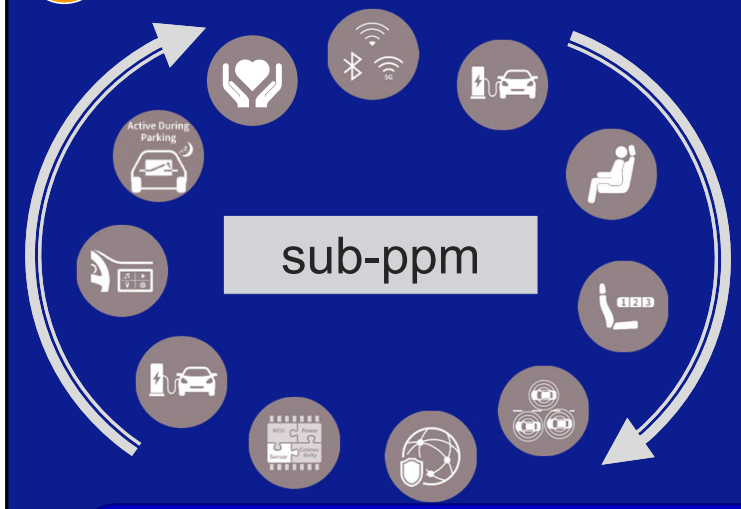
Main drivers:

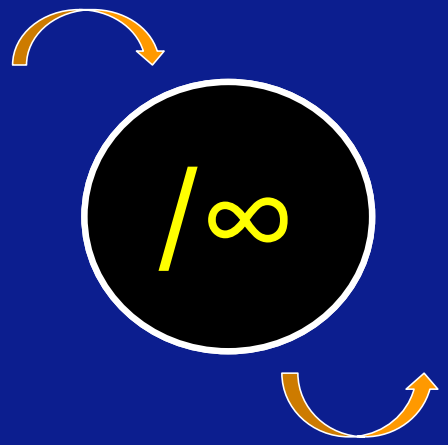
Driving | Preconditioning | Communication | Parking | Charging



Trends in Automotive – "Quality"

3 Trends#1 & Trend#2 lead the trend to even better Quality





„From enthusiasts to demand"

# of incidents / ppb

Main drivers:

>>> ALL OF US <<<

Trends in Automotive – "The rise of DfS"

Why did we create Design for Stress process?

… complexity of hybrid* technologies

… considers the new trends & challenges

… provides a framework

… design and test products

… optimum costs

… high(er) quality targets

* power & logic combined

Design for Stress main principles

1 **Target Extrinsic branch of failure curve (of dielectric materials*) + bit more**

* Bathtub model considered as sufficiently good approximation

**Early Life Failure Rate

Design for Stress main principles

2 **Focus is on electrical activation of defects. This…**

… enables easier outlier detection.

… offers flexibility.
e.g.: flexible stress times

Voltage Acceleration	Temperature Acceleration
(e.g.: linear E model)	(e.g.: Arrhenius law)

$$AF_V = e^{\frac{\gamma}{d_{oxide}} \cdot (V_{stress} - V_{use})}$$

$$AF_T = e^{\frac{E_a}{k} \cdot \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)}$$

Design for Stress main principles

3 **Do it faster, cheaper, and targeted**

- **Faster:** High voltage with reduced stress times
- **Cheaper:** use Automated Test Equipment (ATE) instead of BI ovens
- **Targeted:** Test pads on Wafer test levels for dedicated stress

replace BI in production

Design for Stress main principles

4 **Increasingly complex products need (DfS) guidelines that provides:**

V_{stress} T_{stress}

- Max. stress and temperature levels
- Sufficient stressed area
- Acceptable unstressed area

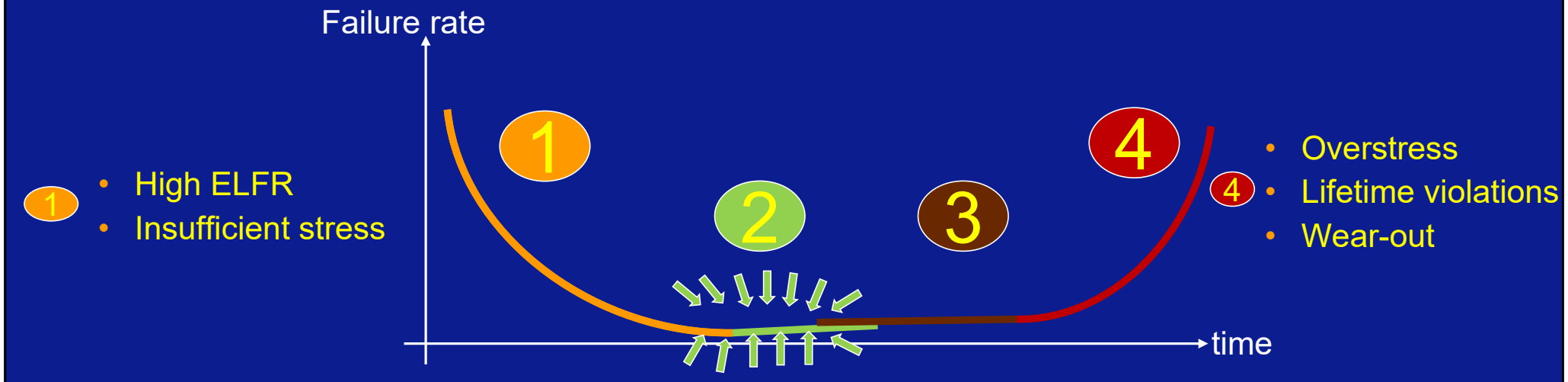
Area [%]

- Stress times acc. targets & mission profiles

t_{stress} V_{use} T_{use}

DfS Targets

Main target: Design and stress products at optimized costs, towards Zero Defect. Area-2*



1
- High ELFR
- Insufficient stress

2
- DfS Targets
- Optimum stress levels
- Optimum stress times

3
- Unnecessary DfT (area)
- Lower ESD protection
- Too long stress times (€)

4
- Overstress
- Lifetime violations
- Wear-out

* Not Area-51!! ☺

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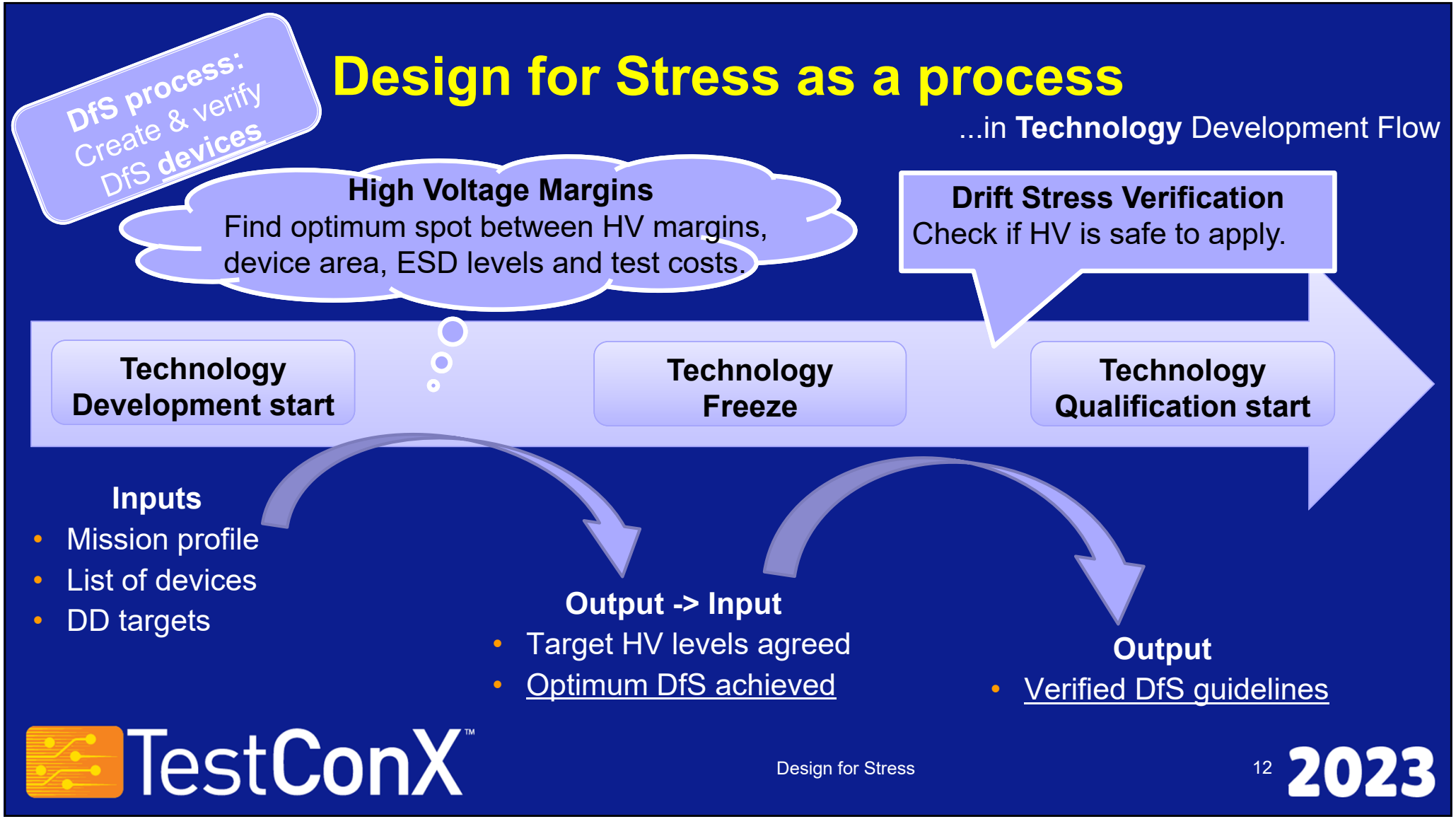
DfS process:
Create & verify
DfS devices
Design for Stress as a process
...in Technology Development Flow
High Voltage Margins
Find optimum spot between HV margins, device area, ESD levels and test costs.
Drift Stress Verification
Check if HV is safe to apply.
Technology Development start
Technology Freeze
Technology Qualification start
Inputs
Mission profile
List of devices
DD targets
Output -> Input
Target HV levels agreed
Optimum DfS achieved
Output
Verified DfS guidelines
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12
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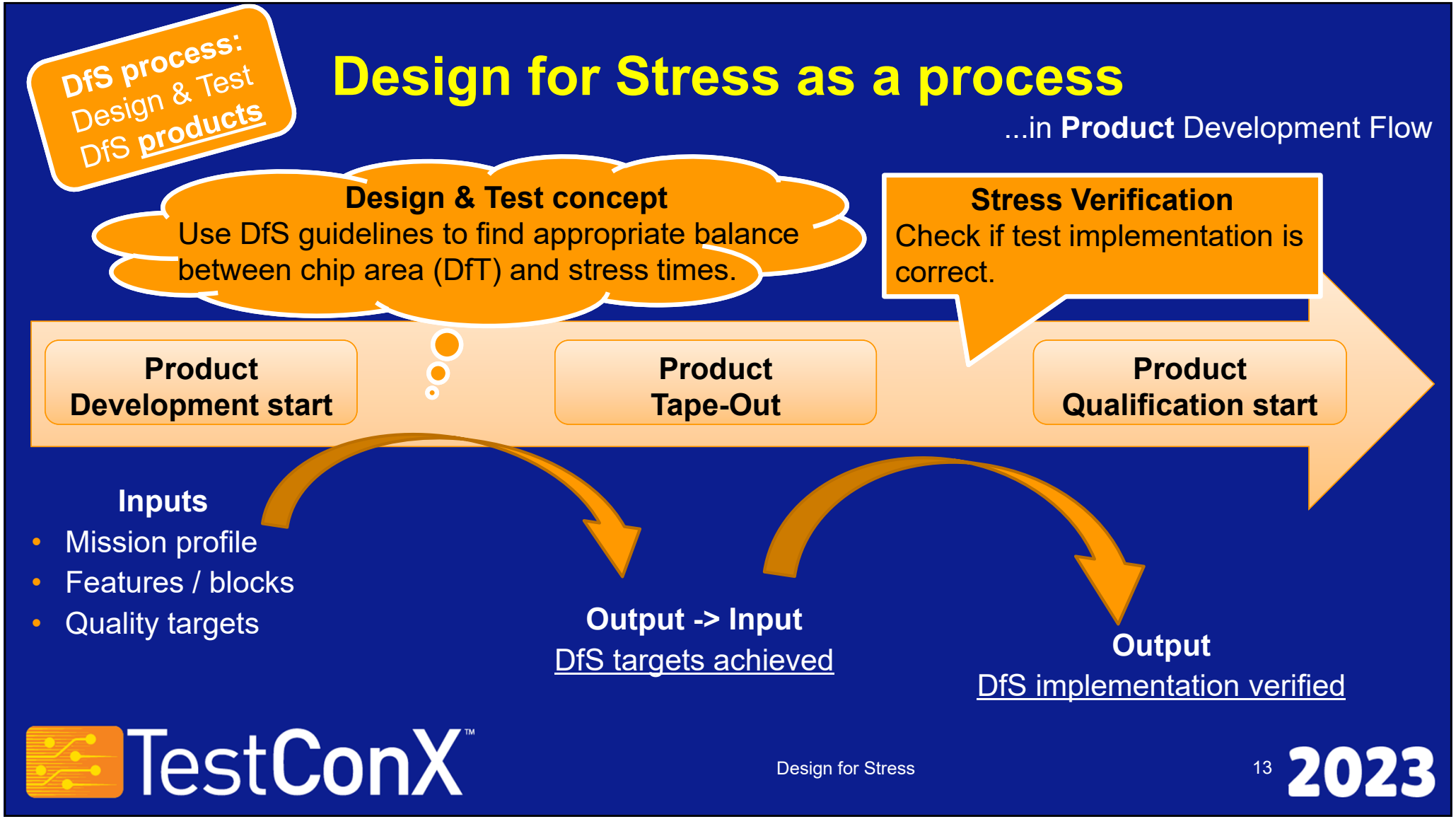
DfS process:
Design & Test
DfS products
Design for Stress as a process
...in Product Development Flow
Design & Test concept
Use DfS guidelines to find appropriate balance between chip area (DfT) and stress times.
Stress Verification
Check if test implementation is correct.
Product Development start
Product Tape-Out
Product Qualification start
Inputs
Mission profile
Features / blocks
Quality targets
Output -> Input
DfS targets achieved
Output
DfS implementation verified
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13
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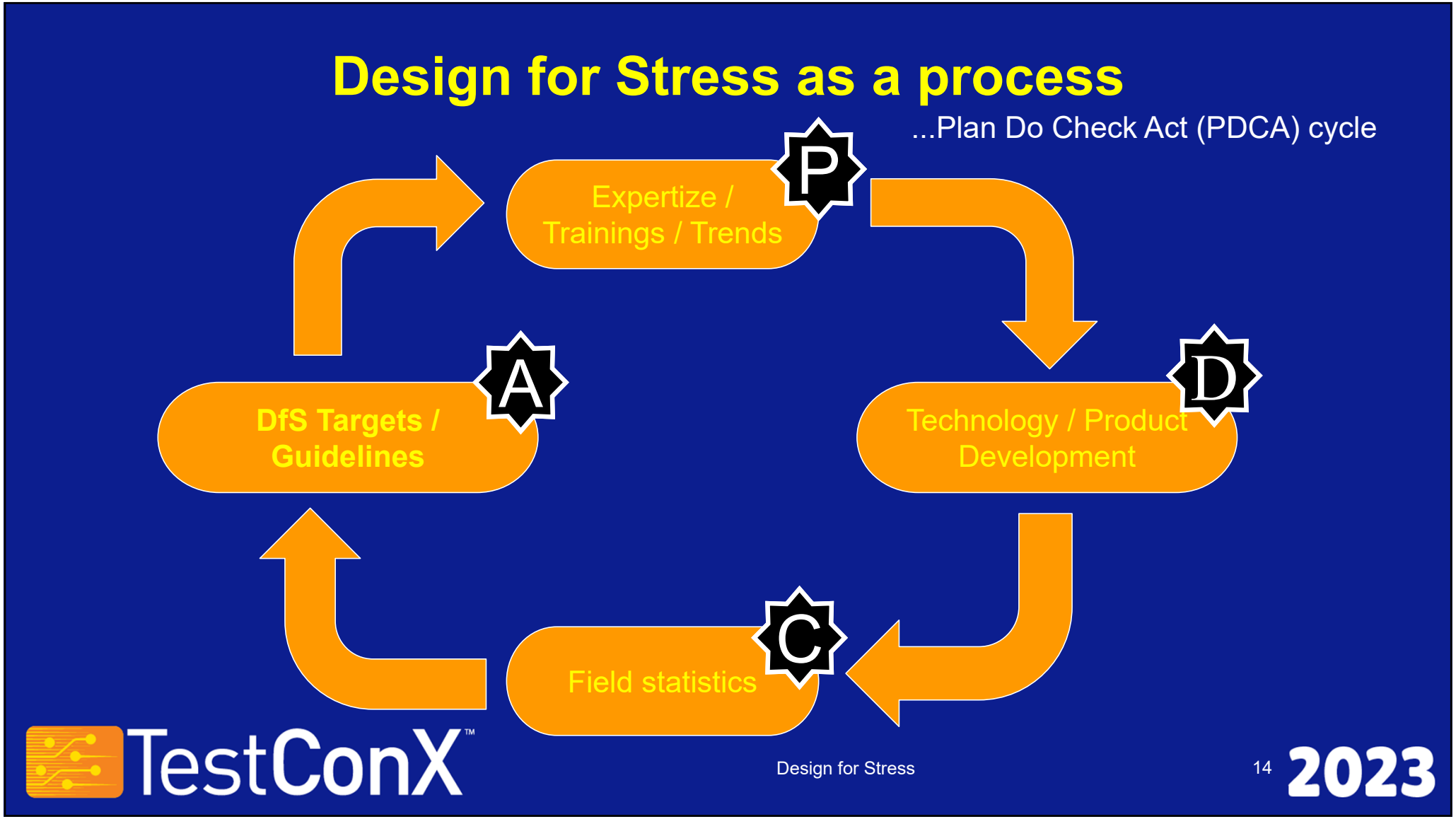
Design for Stress as a process
...Plan Do Check Act (PDCA) cycle
Expertize / Trainings / Trends
P
Technology / Product Development
D
Field statistics
C
DfS Targets / Guidelines
A
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14
2023

Design for Stress successes - Case Study

BI Study execution – Logic stress@wafer test

Pre-BI stress condition	...without DfS		...with state-of-art DfS
Test Temperature	-40°C	~x30k	125°C
Max. Stress voltage [V]	Max. @cold (1.7V*) Lim.: Hot Carrier Injection	~x200k	Max. @hot (2.5V*) (ESD, max. HV margin)
Stress times	(50ms*) Lim.: Hot Carrier Injection		Reach DfS Targets (300ms*)
Detection on ATE	Delta IDDQ (5uA*) (pre vs. post stress)		Absolute limits (100uA*) (post stress only)
BI Study results (3h)	> 0 failures		0 failures

AF** increase ~x6B

* example values representing DfS approach

** Acceleration Factor

Design for Stress successes - Case Study

- 1st time pass in BI Studies leading to faster execution times (2~3x.)
  - Decreased # of failure analysis & discussions needed.
  - No FE process changes needed.
  - No BI Study repetition needed.
- DfS volumes field performance is <40 ppb @ 90% CL*
- DfS contributes to Infineon ‘s position as a profitable quality leader.

* for dielectric defects.

Design for Stress successes - Summary

- Implemented in Infineon **development flows.**
- **Trained** product development teams to apply optimum DfS.
- More than **30 products** released with DfS process.
- **Excellent field performance and high customer satisfaction.**
- Smoother and **faster BI Study** executions.
- Field data monitoring allows further **optimization** of stress times.