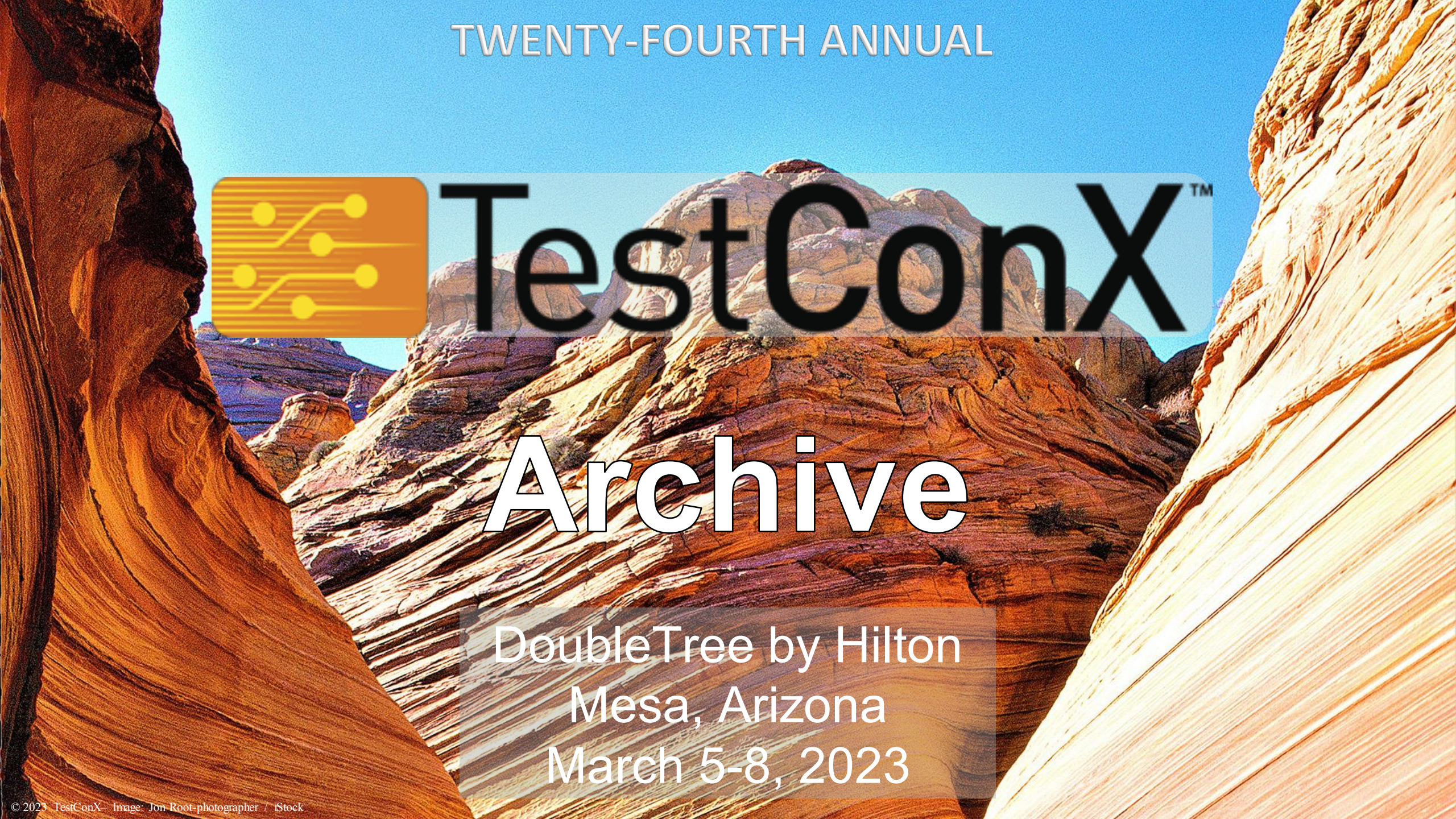


With Thanks to Our Sponsors!

Premier

HiCon

Honored

GLOBAL INNOVATION ISC

WIN SOLUTION

LEENO Total Interface Solutions

TSE

With Thanks to Our Sponsors!

Distinguished

Johnstech™

smiths interconnect

MICRO CONTROL COMPANY SINCE 1972

CTFE Align & Smart Contact

ADVANTEST®

Industry Partners

SWTEST

MEPTEC THE NEXT GENERATION

COPYRIGHT NOTICE

www.testconx.org

Verification of Solution Options for 28G SI Validation

Noel Del Rio - NXP Semiconductors

Dan Hwang - HiCon Co., Ltd.

Paul Schubring - HighRel, Inc.

TestConX™

Mesa, Arizona • March 5-8, 2023

Contents

- Problem Statement & Motivation
- Process Overview
- System Configuration
- Socket Technology Description
- Simulation and Measurement Results
- Discussion
- Conclusions

Problem Statement

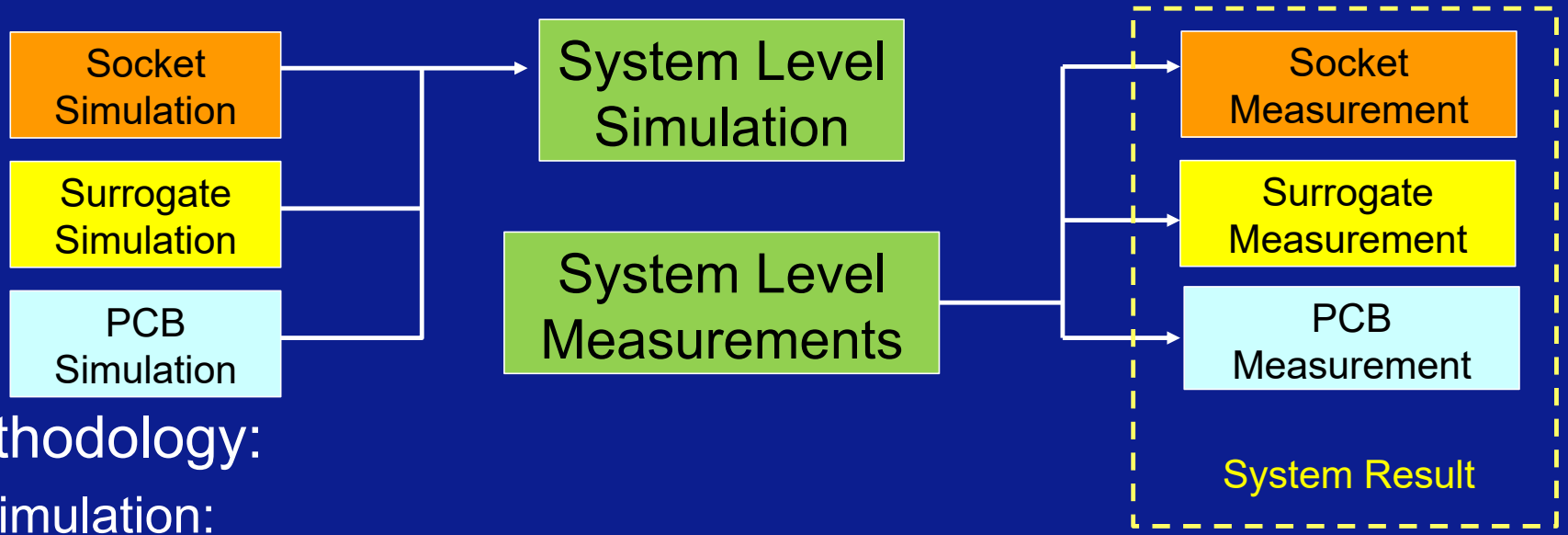
- The technology treadmill never slows
  - Speed / Pitch / Power demands introduce greater and greater technical challenges for test hardware
- Key challenge is to develop cost effective hardware solutions to address these issues
  - Validating that solutions meet design requirements is becoming more difficult and cost prohibitive
- More and more, simulations are becoming the primary way to 'validate' hardware performance
  - Reduce development lead time
  - Reduce hardware validation costs
- Can simulation results be trusted as reliable predictors of real-world performance?

Motivation

- With significant reliance on simulations, it is good to periodically check that the weight given to simulation results is justified
- 'Trust but verify'
- 'Doveryai, no proveryai'
  - Russian proverb:
    A responsible person always verifies everything before committing himself to a common business with anyone, even if that anyone is totally trustworthy

Image: Public Domain

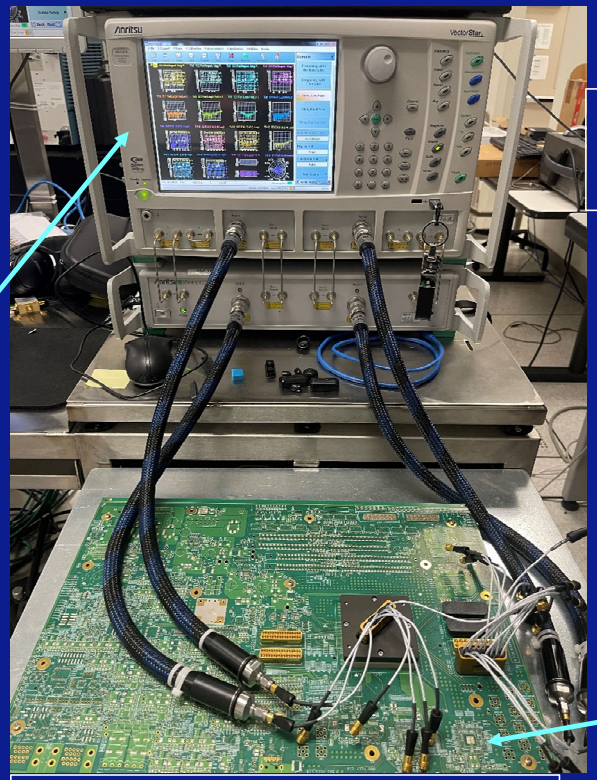
Verification Process



Methodology:

- Simulation:
  - Simulate socket, surrogate, & PCB Individually
  - Combine into system level simulation
- Measurement:
  - Measure complete system performance
- Validation: Compare to simulation and measurement results

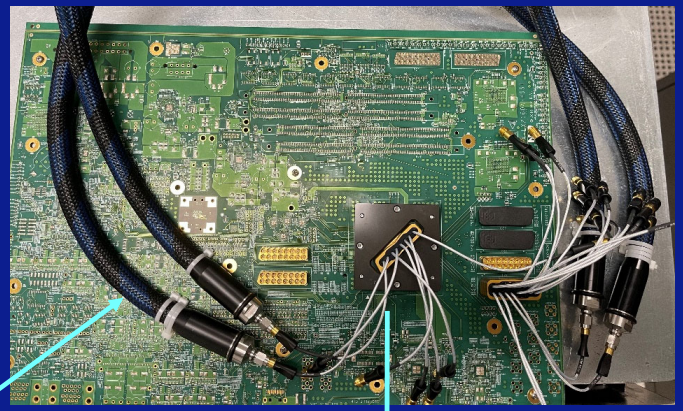
Verification System Configuration



70GHz VNA

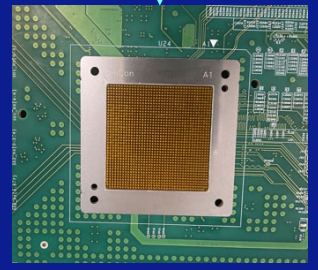
Test Bench Setup

VNA Validation Lab setup



Phase Matched Cables

Application Board



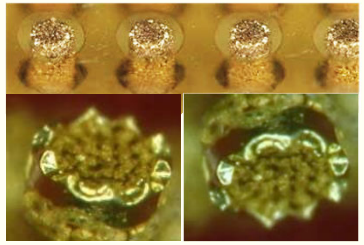
HiCon Socket

NXP Application Board Test Set up

Verification Hardware - Sockets

- Sockets used are 1mm pitch, 1521pin, 40mm 28G device
- Interconnect technologies for evaluation:
  - HiCon HyBrid™ (HBR) contact pin
    - See Bridging the Gap, Part 1 (TestConX) 2020 for complete introduction
  - HiCon HSRR contact pin
    - See Bridging the Gap, Part 2 (TestConX) 2022 for complete introduction

HyBrid™ (HBR) Technology Overview

	HiCon HyBrid pin (HB)
Image	
DC Resistance	≤ 80mΩ
Force	≤ 40g
Pitch Capability	> 0.8mm (Available down to 0.20mm)
Mechanical Cycles	~ 100K
Temperature Range	-40°~125℃
C.C.C	> 3A
Key Features	Stamped Pin + Conductive Powder

Specifications for
1mm version

HBR Contact Features:

- Combines elastomer and mechanical pin technology in one
- Support 0.20mm minimum pitch
- Same electrical performance as traditional elastomer technology
- Mechanical component provides extended mechanical life

Free Height	1.24mm	0.95mm	0.8mm	0.6mm	0.6mm	0.6mm	0.5mm
Model							
Diameter	0.32mm	0.32mm	0.32mm	0.24mm	0.2mm	0.15mm	0.12mm
Pitch	1.0~0.8 mm	0.75~0.8mm	0.65~0.4mm	0.45~0.4mm	0.35~0.3mm	0.25 mm	0.2 mm

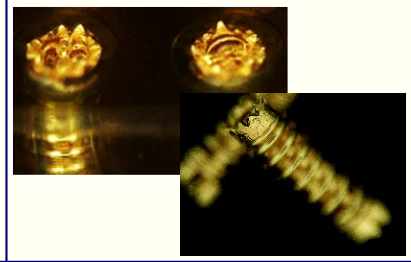
TestConX™

Verification of interconnect solution options for 28G Si validation

8

2023

HSRR Technology Overview

	HiCon Stamped Pin (HSRR)
Image	
DC Resistance	≤ 80mΩ
Force	Available in 16~26g
Pitch Capability	> 1mm ~ 0.25mm
Mechanical Cycles	≥ 100K
Temperature Range	-50°~150℃ and 180℃
C.C.C	> 3A
Key Features	Fully stamped - Robust & Economical

Specifications for 1mm version

HSRR Features:

- Fully stamped solution
- Support 0.25mm minimum pitch
- Similar electrical performance as HyBrid contact
- Greater mechanical stroke
- Greater temperature range (150°C and higher)
- High current
- Increased mechanical life
- Available test heights: 0.36 – 2mm
- Elastomer and plastic versions available

Free Height	1.2mm	1.0mm	0.8mm	0.6mm	0.5mm
Model					
Diameter	0.38mm	0.32mm	0.27mm	0.20mm	0.155mm
Pitch	1.0~0.6mm pitch	1.0~0.5mm pitch	0.65~0.4mm pitch	0.4~0.3mm pitch	0.3~0.25mm pitch

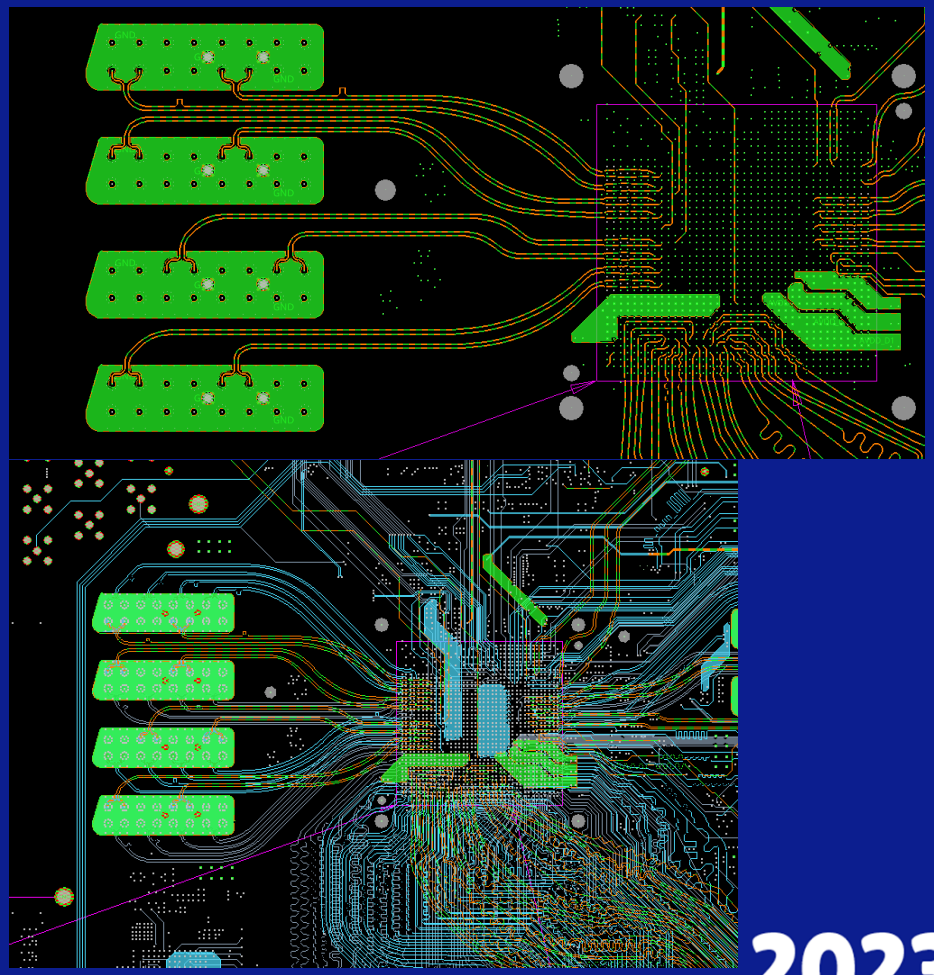
Available HSRR Pins (Elastomer Version)

TestConX™

Verification of interconnect solution options for 28G Si validation

Measurement Setup

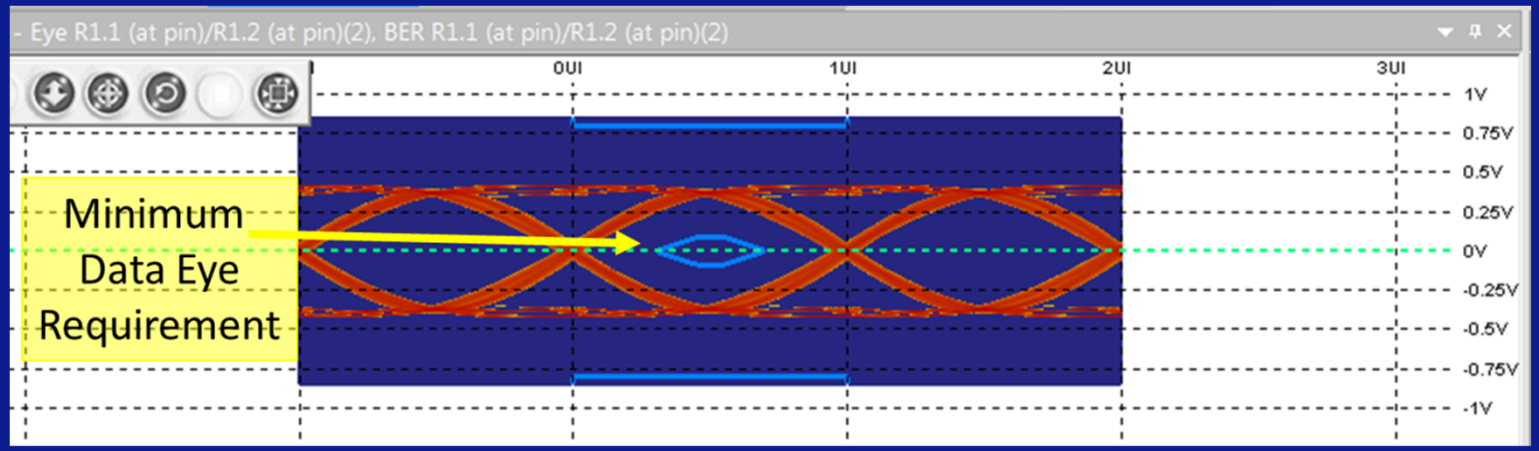
1. VNA DC to 30Ghz @ 3Mhz resolution or steps
2. HiCon LX2 Test Socket
3. 1mm pitch / 1517BGA Surrogate Package
4. Differential Measurements: 8 Potential Channels for Measurement
5. Room Temperature using 70Ghz VNA
6. No LX2 functional test
7. HyperLynx simulator on one lane, PRBS31 at 28G data rate



TestConX

Verification of interconnect solution options for 28G Si validation

Data Presentation Method

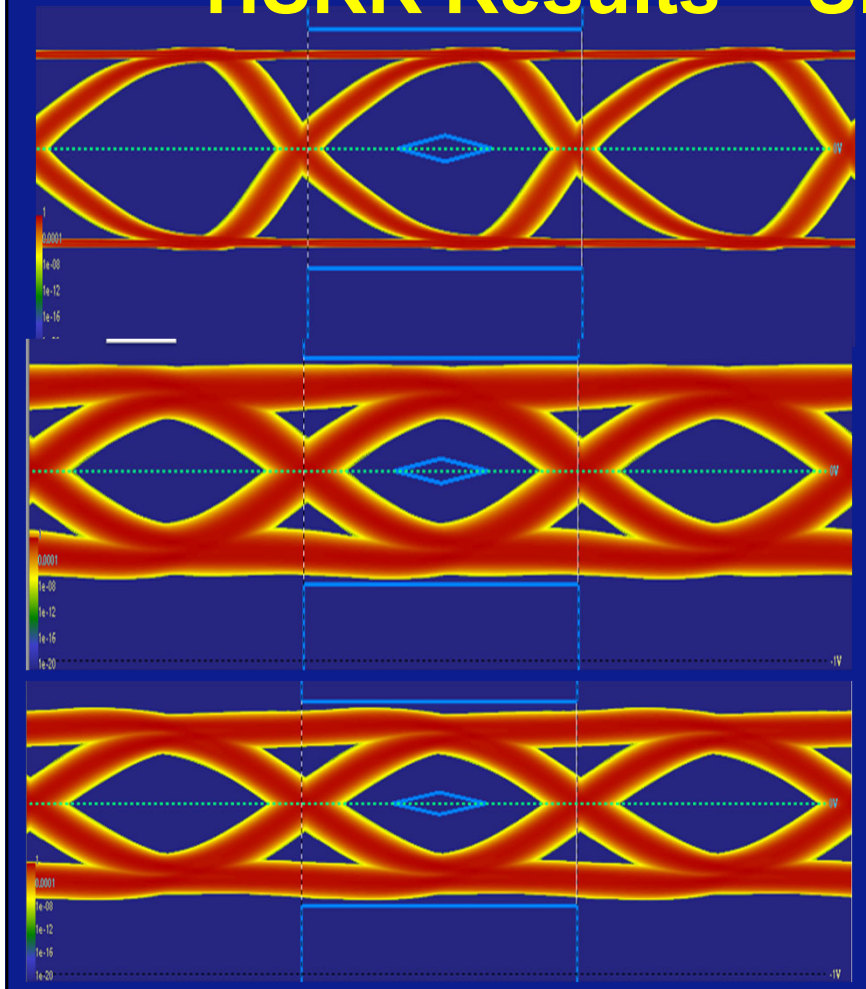


X-axis:
Unit Interval

Y-axis:
Amplitude

- Data output will be plotted as with a data eye
- Format is easy to interpret as there is a minimum data eye requirement needed for the application and it is easy to judge performance relative to the data eye

HSRR Results – Simulation vs. Measurement



HSRR 1.2 Test Board Simulation
Data Eye 28G PRBS31
UI=0.800 ps
Amplitude = 0.800 V

Simulation: Test Socket Extracted from Test Board

HSRR NXP App Board
VNA Measured
Lane SD1 T1, 7-inch trace
Eye 28G PRBS31
UI=0.701 ps
Amplitude = 0.504 V

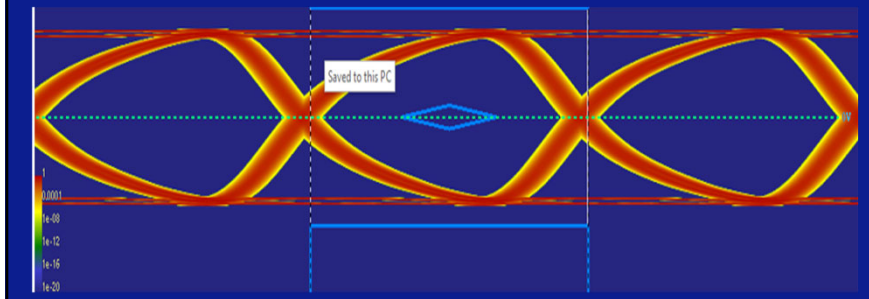
HSRR NXP App Board
VNA Measured
Lane SD1 R0, 7-inch trace
Eye 28G PRBS31
UI=0.649 ps
Amplitude = 0.491 V

NXP Application Board

VNA Measured PRBS-31 28G

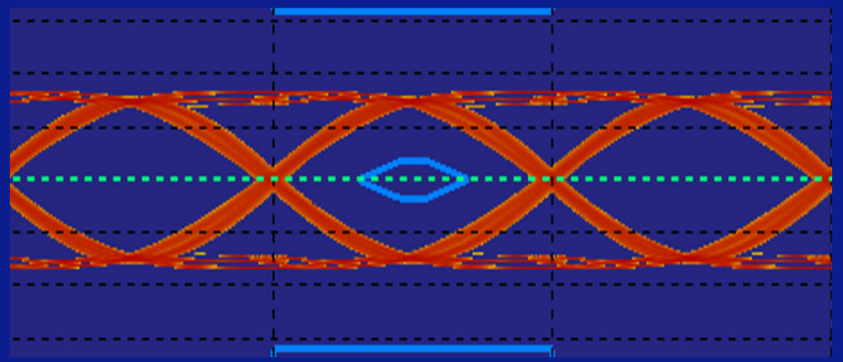
7-inch trace (Adds 0.6dB/inch) + cabling not de-embedded

HBR Results – Simulation vs. Measurement



HBR Simulation Test Board
Data Eye 28G PRBS31
UI=0.829 ps
Amplitude = 0.764 V

Simulation: Test Socket Extracted from Test Board



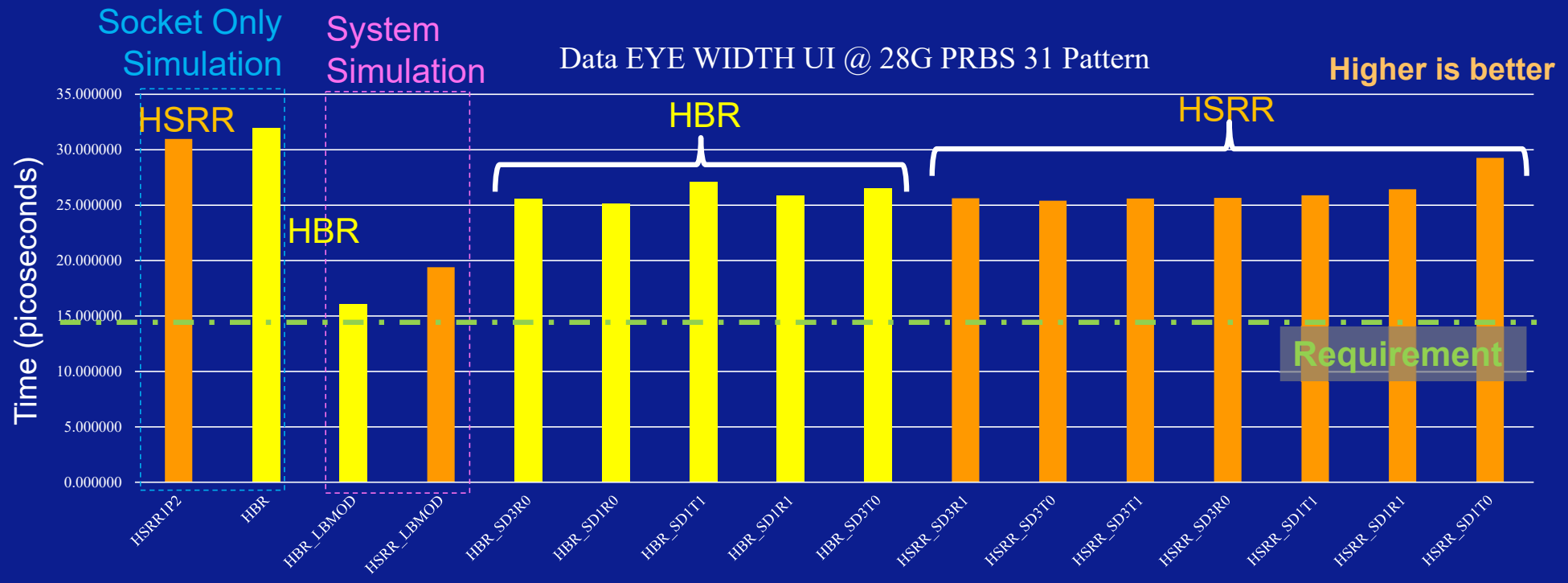
HBR NXP App Board
VNA Measured
Lane SD3 R0, 7-inch trace
Eye 28G PRBS31
UI=0.760 ps
Amplitude = 0.601 V

NXP Application Board

VNA Measured PRBS-31 28G

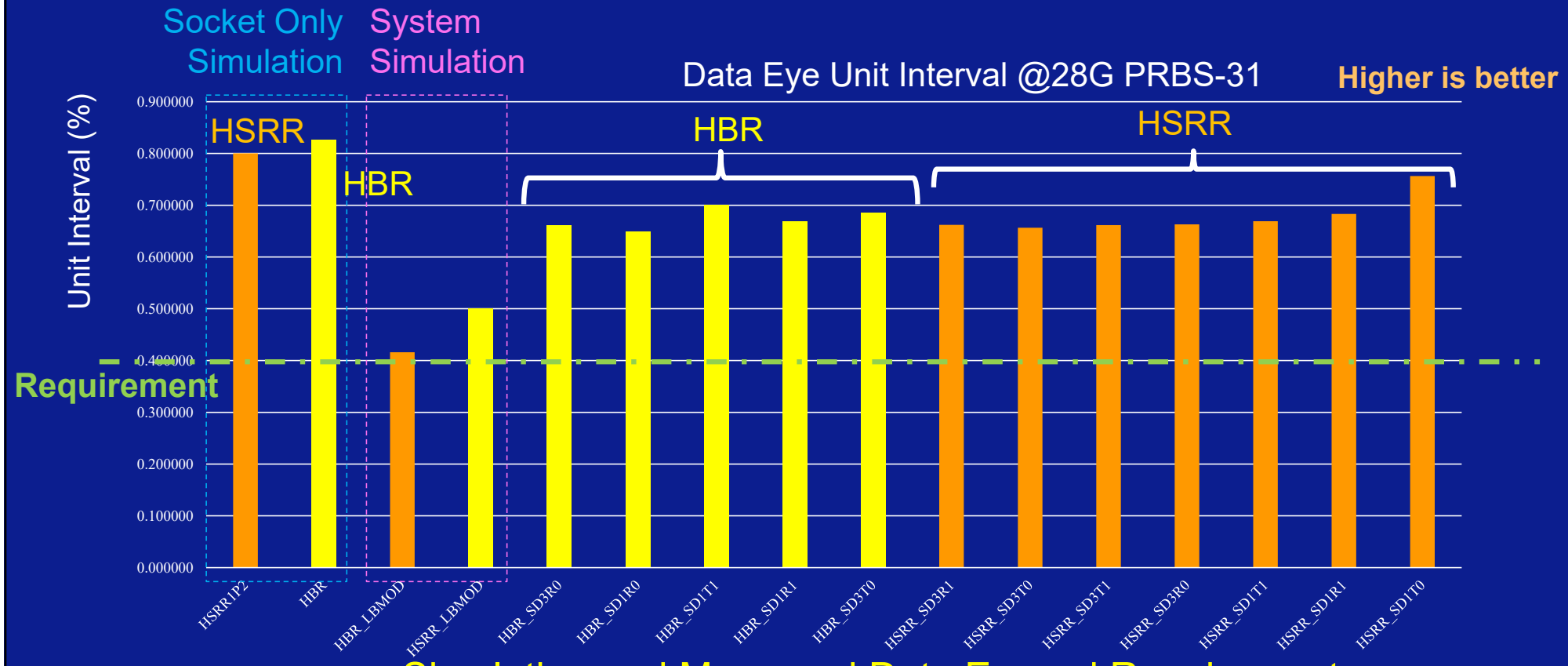
7-inch trace (Adds 0.6dB/inch) + cabling not de-embedded

Measurement Results: Data Eye Unit Interval (Time) – Full System



PRBS31 Test Pattern = Worst Case / Most Challenging Pattern

Measurement Results: Data Eye Unit Interval (%) – Full System



Simulation and Measured Data Exceed Requirement

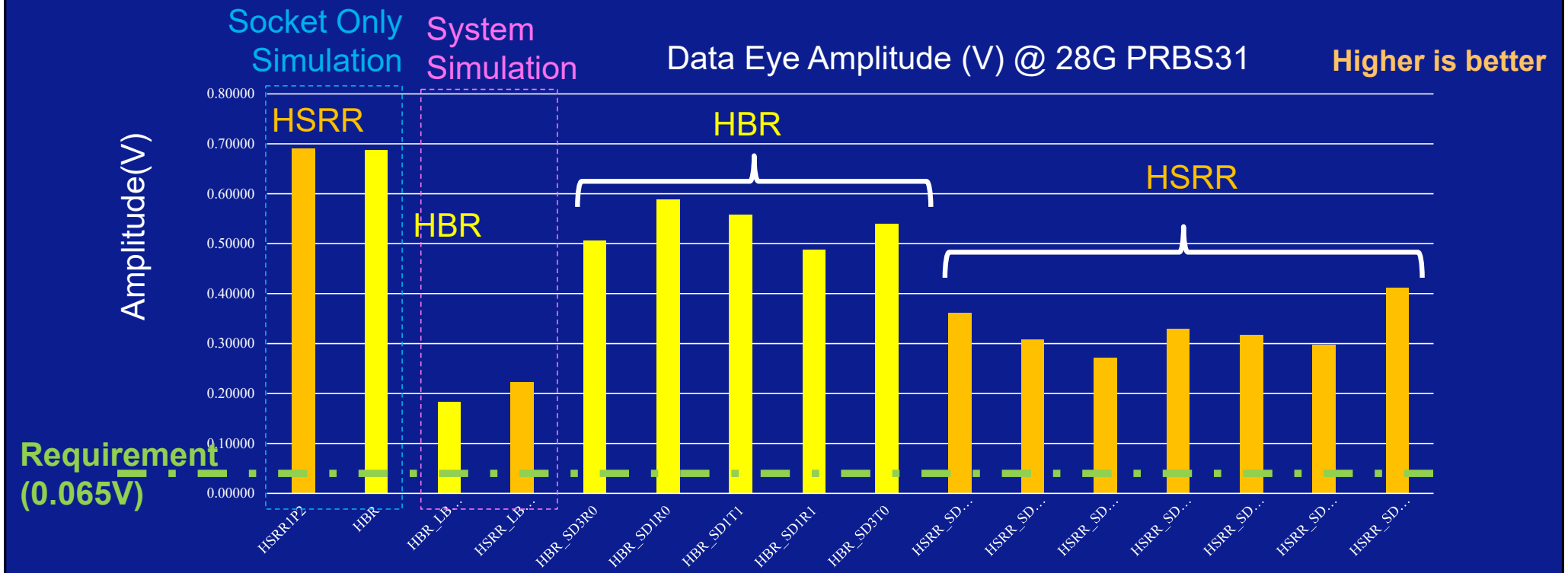
TestConX

Verification of interconnect solution options for 28G Si validation

15

2023

Measurement Results: Data Eye Amplitude – Full System



Discussion of Results

- A total of 12 measurements were performed on two different sockets and compared to the entire system simulation
- All 12 measurements were found to offer a conservative estimation of the actual system performance
  - This is not always the case!
- Experience and understanding the performance of the components in the system are helpful in improving simulation accuracy
  - Impedance can play a large role on measurement results
  - PCB trace lengths contributed a significant amount to the measured data
  - Measuring individual components and correlating to component simulations is beneficial

Conclusions

- With increasing complexity and costs of test hardware, simulations are a valuable tool to reduce development costs, lead time, and delivery first time right solutions
- Both the HiCon HSRR and HiCon HyBrid™ (HBR) contact technologies showed significant margin for 28G testing
- Correlation of simulation to measurement results showed good results and provided a conservative predictor of actual performance
- This is not always the case:
  Remember: 'Doveryai, no Proveryai' - Trust but Verify!