TWENTY-FOURTH ANNUAL

TestConX™

Archive

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Mesa, Arizona
March 5-8, 2023

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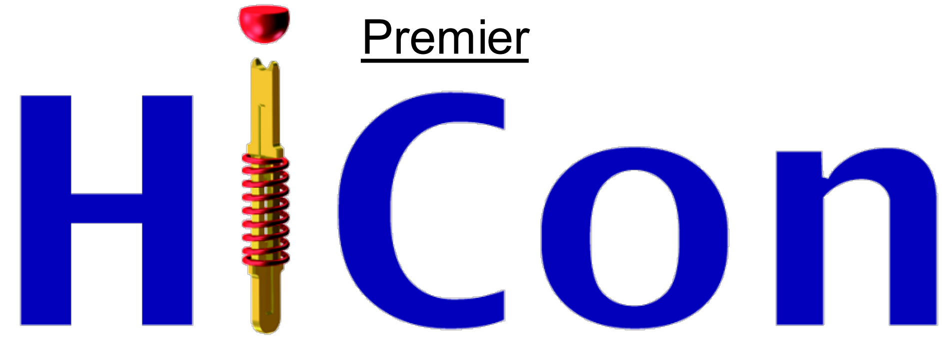

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Transmission Line of RF, Serdes I/O Test Hardware Signal Path

Noel Del Rio

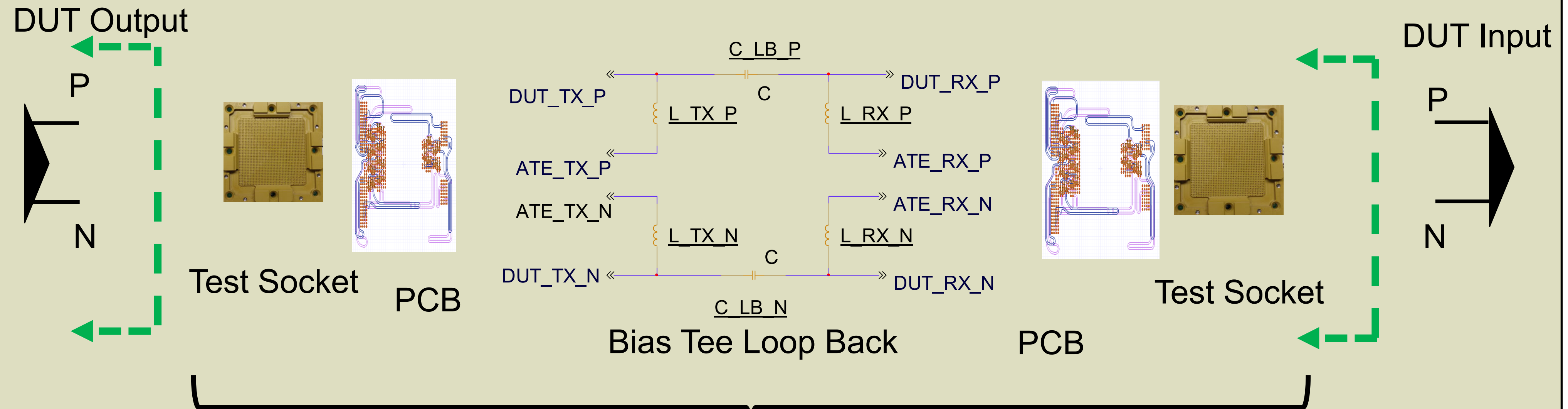
NXP Semiconductor

Mesa, Arizona • March 5–8, 2023

Agenda:

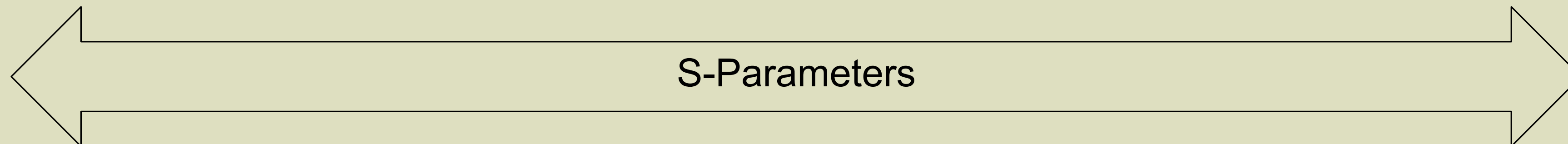
- Signal Path Segments
- Serdes Receiver Data Eye Mask
- LC Loop Back
- RC Loop Back
- RF Differential Switch
- Test Socket or Interposer
- PCB and related structures
- Closed Loop hardware design flow
- Test hardware performance measurement results
- Conclusion

Test Hardware Signal Path



TX Impedance =100 Ohms

RX Impedance =100 Ohms



Transmission Line of RF, Serdes I/O Test hardware Signal Path

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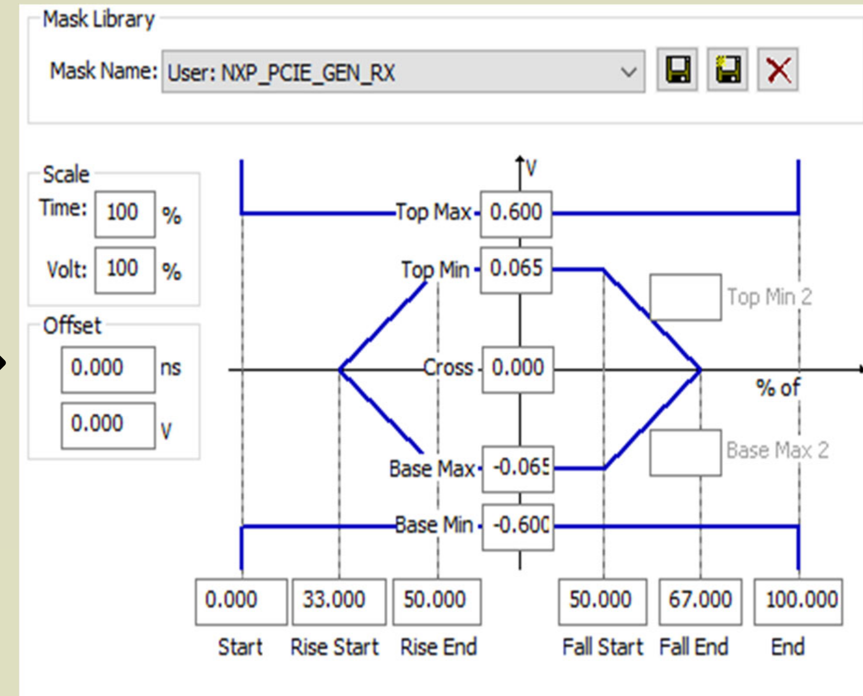
Serdes receiver data eye-mask

DUT Receiver Data Eye mask specifications

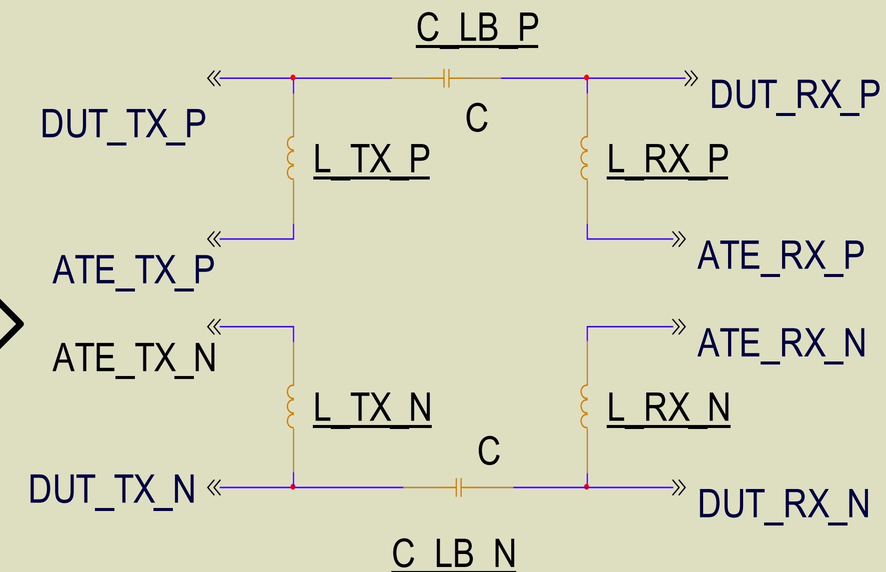
- Unit Interval (UI) of a transmission cycle.
- It defines the minimum level required at the input of the receiver.
- It defines the minimum data eye-width in a transmission cycle.
- It defines the phase relation of the signal in UI.
- The data eye masks accounts for signal integrity issues related jitter, attenuation, crosstalk, device associated defects.



LC Loop Back Circuit

Serdes Loop Back Circuit

- Electrical link. A transmission line from DUT transmitter drivers to DUT receivers to facilitate self-test at specified data rate.
- A bypass-capacitor is required to eliminate the transmitter common-mode at the receiver input.
- The Inductor provides electrical link to ATE channel to facilitate structural, functional, and parametric type test.
- Inductor provides a high impedance isolation between DUT pin and ATE channel



LC loop back(SD2D1) insertion loss profile

28G HW Pass Region

Power dBm

3dBm HW Budget

Short, low impedance @ Low Frequency

16G HW Pass Region

30 GHz

Frequency GHz

Transmission Line of RF, Serdes I/O Test hardware Signal Path

LC loop back impedance profile

Good impedance profile from TX to RX

Impedance Ohms

10 Ohms HW Budget

Transmission Line of RF, Serdes I/O Test hardware Signal Path

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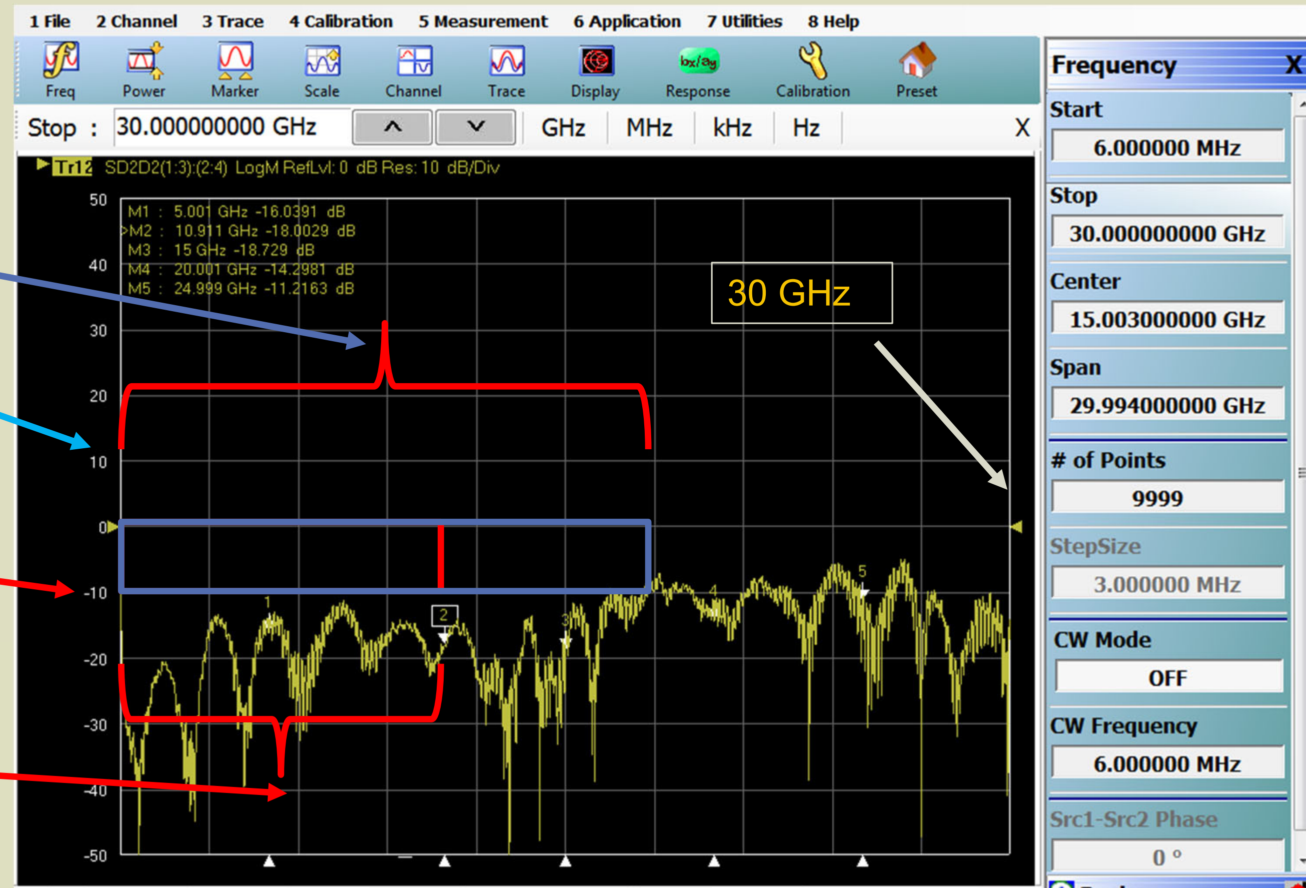
LC return loss (SD2D2) profile across frequency

28 G HW Pass Region

Power dBm

-10dB HW Budget

16 G HW Pass Region



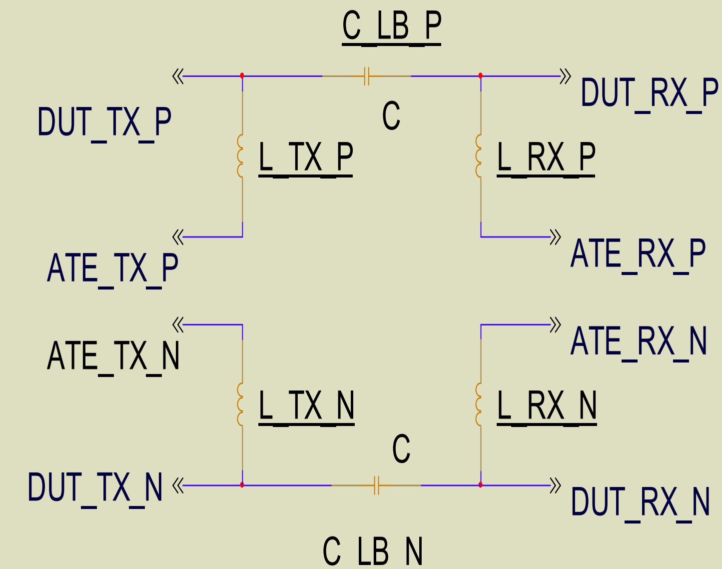
Frequency GHz

Transmission Line of RF, Serdes I/O Test hardware Signal Path

8 2023

LC loop back characteristics

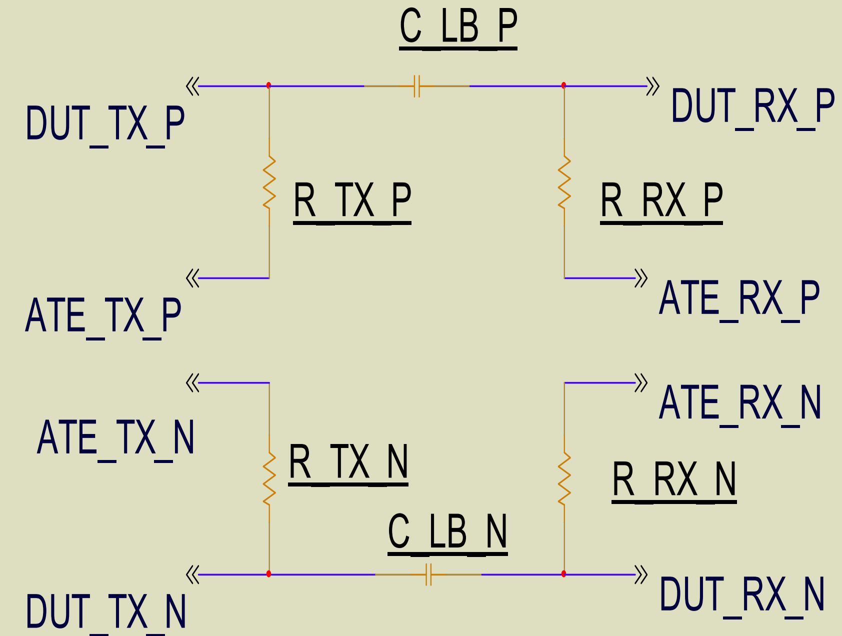
- Insertion Loss (S21, D2D1) starts at negative or very low power level at low frequency range. Inductive short at low frequency is ideal for parametric type testing
- Validated inductor broadband performance can contain impedance-change from TX-output to RX-input to required range(e.g. 10 ohms window)
- High reliability loop back circuit.
- Next to RC in small footprint for high I/O count devices (e.g. 64 Serdes lanes)
- Coil variability and non-linearity is common as a function of frequency



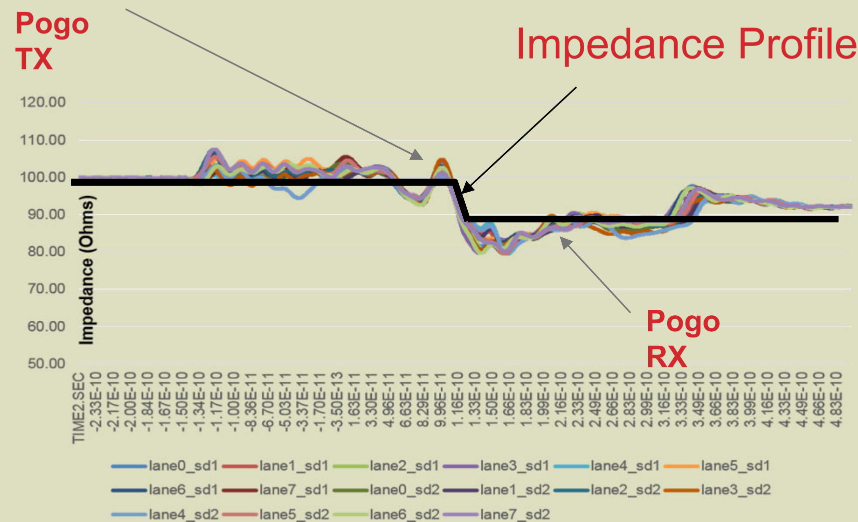
RC loop back circuit

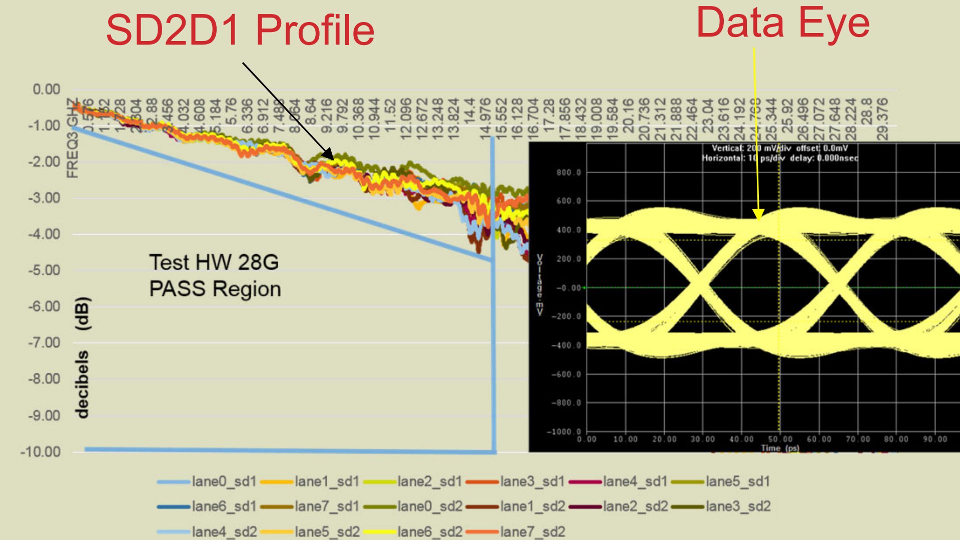
Serdes Loop Back Circuit

- Electrical link. A transmission line from DUT transmitter drivers to DUT receivers to facilitate self-test at specified data rate.
- A bypass-capacitor is required to eliminate the transmitter common-mode at the receiver input.
- The resistor provides a high impedance isolation between DUT pin and ATE channel



RC impedance profile, insertion loss profile, and data eye

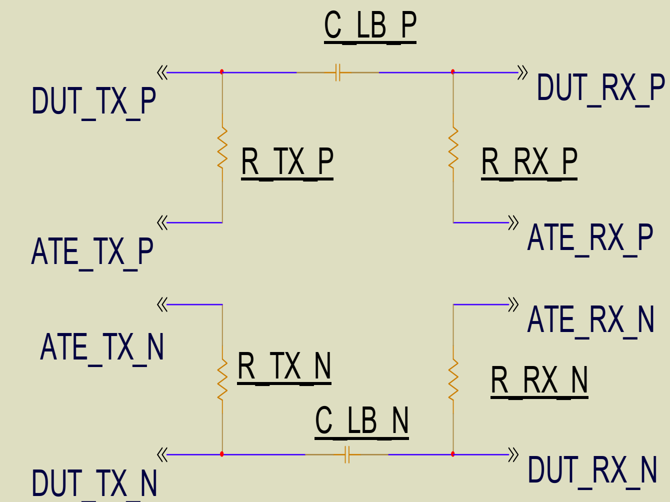




Transmission Line of RF, Serdes I/O Test hardware Signal Path

RC loop back characteristics

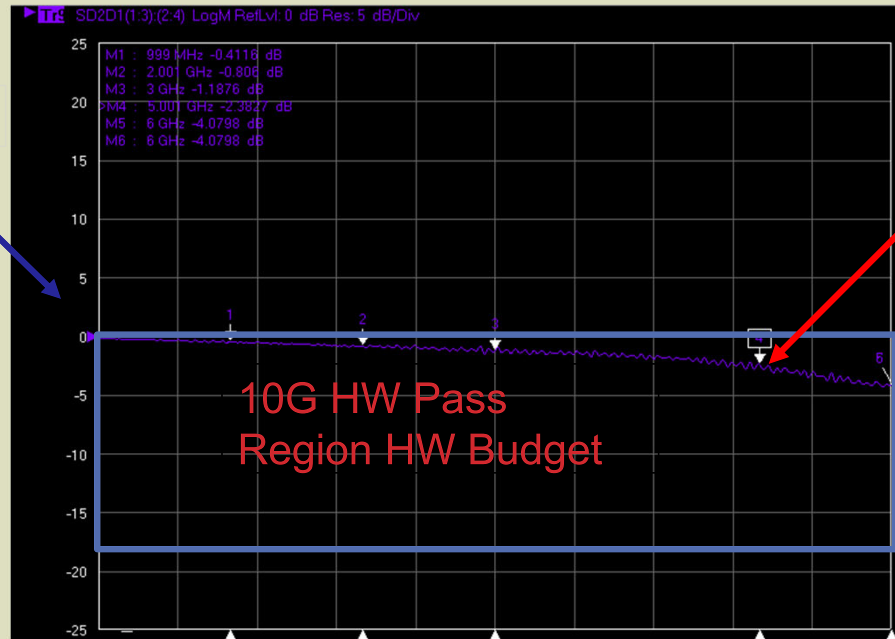
- Step function impedance profile from TX-output to RX-input defined by the resistance value of the filter
- Insertion loss starts are preset value at dc or frequency zero. Insertion loss start value is defined by the resistance of the filter
- Excellent linearity for the insertion loss(S21, D2D1) curve
- High reliability and less exposure to component failure
- Small footprint for high Serdes lane count (e.g. 64 lanes)
- Parametric test is a challenged with ATE-access limited by the series resistance



RF differential switch loop back

Measured Insertion Loss D2D1

Power (dBm)



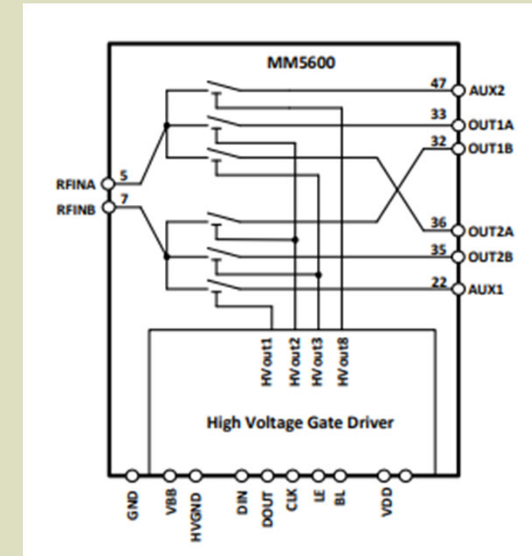
Frequency (GHz)

RF Differential Switch

1. Low loss
2. Wideband performance better linearity
3. Small package mems switch that match differential trace

RF switch loop back characteristics

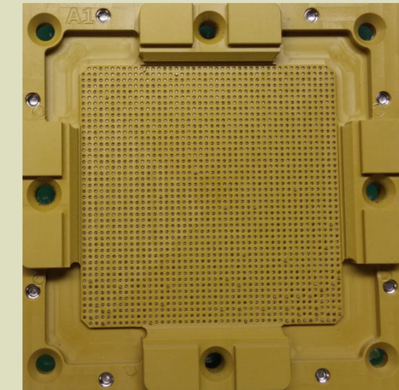
- Can support functional and parametric test with less constraints
- Broadband performance is dictated by switch specification
- Good Linearity for the insertion loss (S21, D2D1) curve
- RF switch life as declared by vendor
- MEMS RF switch small package footprint is ideal for match differential pair routing that don't require change on trace spacing



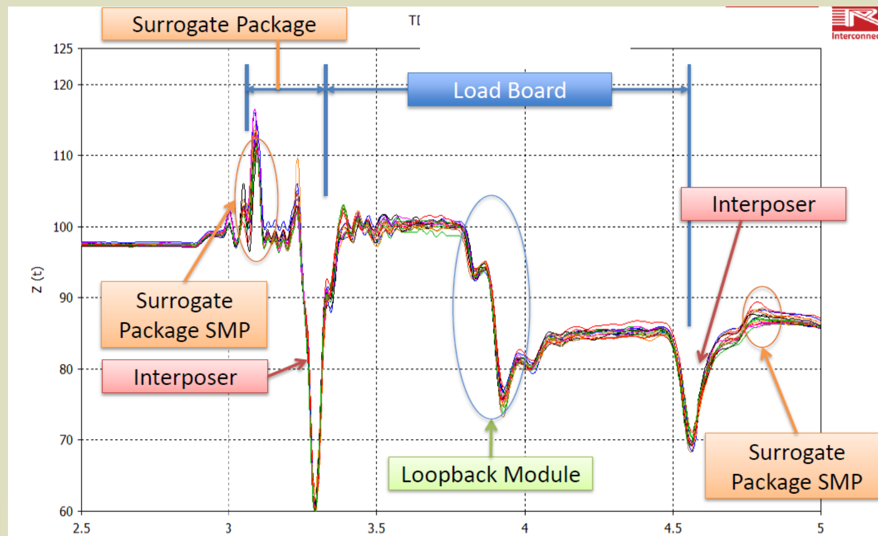
Test socket or interposer

Test Socket

- Electrical connection between the DUT, ATE, and associated resources to facilitate testing.
- A very short transmission line from sub millimeter to less than 4 mm for high data rate application
- The signal path segment that degrades as a function of insertion cycle
- Come in different types like pogo, membrane, coax as a function of application



Test Socket discontinuity or impedance non- compliance



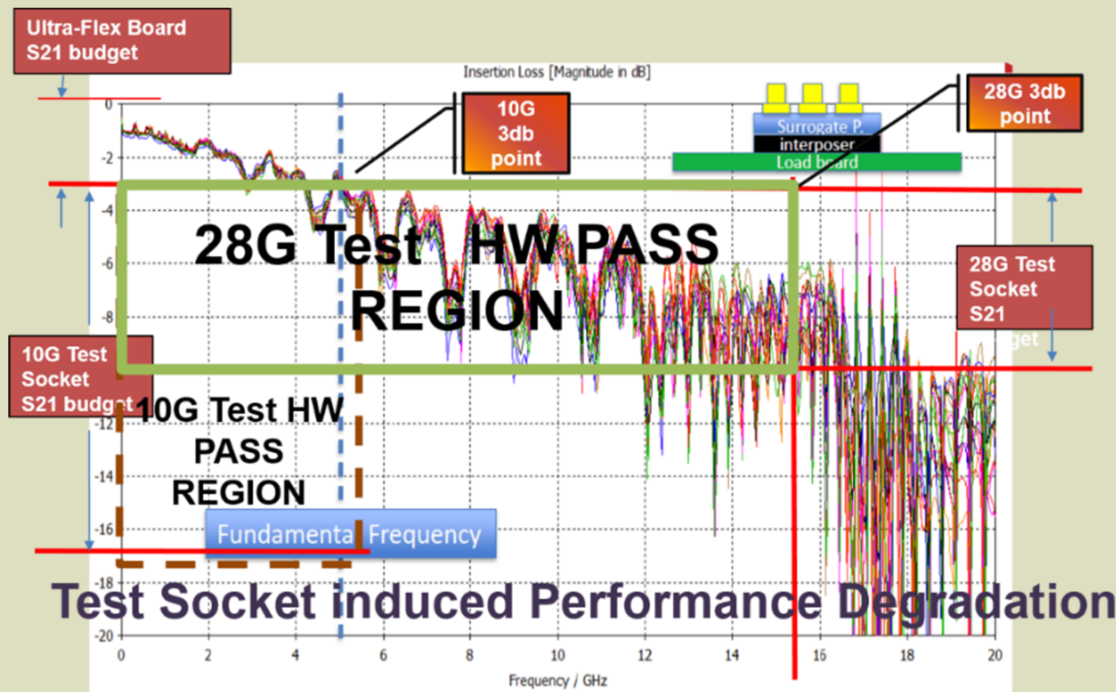
Test Socket Impedance Drop

Test Socket TDR

Test socket discontinuity

- Measured differential impedance approaching 60 ohms
- It is important to measure test socket compliance to impedance requirements
- Simulation results are not assurance of real-world compliance to specifications.

Test Socket discontinuity or impedance non- compliance



15 Ghz

S21 Non-linearity

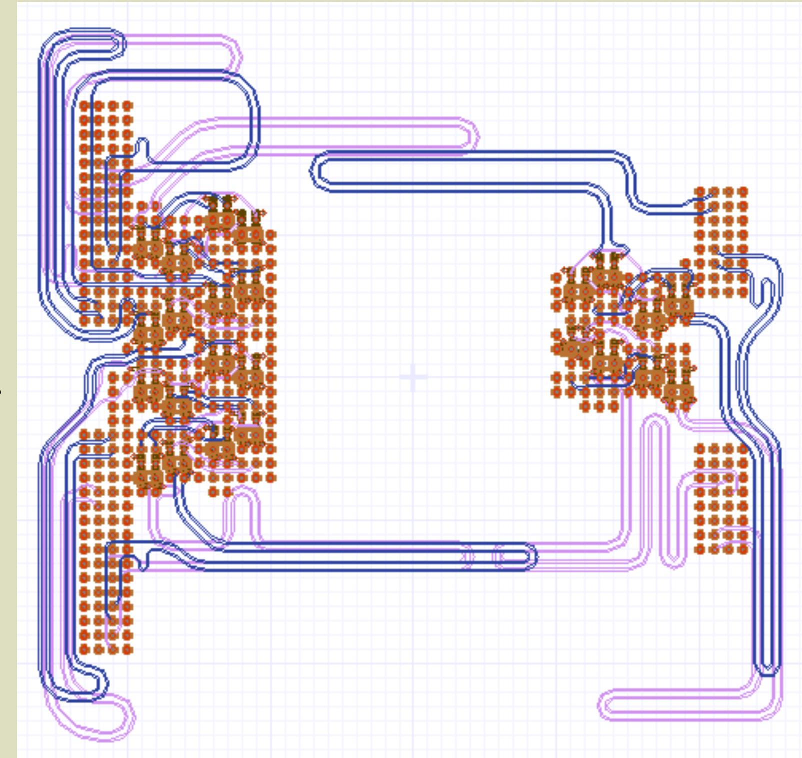
- Resonance due to test socket discontinuity
- Increasing occurrence at higher frequency

Transmission Line of RF, Serdes I/O Test hardware Signal Path

PCB(layout, trace, via, pad, dielectric)

PCB

- Electrical link of the different segment of the signal path
- Physical geometries have profound impact on transmission line performance in frequency and time domain
- PCB Interconnects such as vias, pads are the common source of discontinuity
- Dielectric constant and physical geometries of the structure dominates the signal loss along the signal path



Trace length loss per length as a function of frequency 1.000 Oz 3.000 mils stripline, DK=3.000

Trace Loss per length as a function of frequency

- Dielectric loss curve
- Resistive loss curve as function of trace geometries such as width, and thickness

Transmission Line of RF, Serdes I/O Test hardware Signal Path

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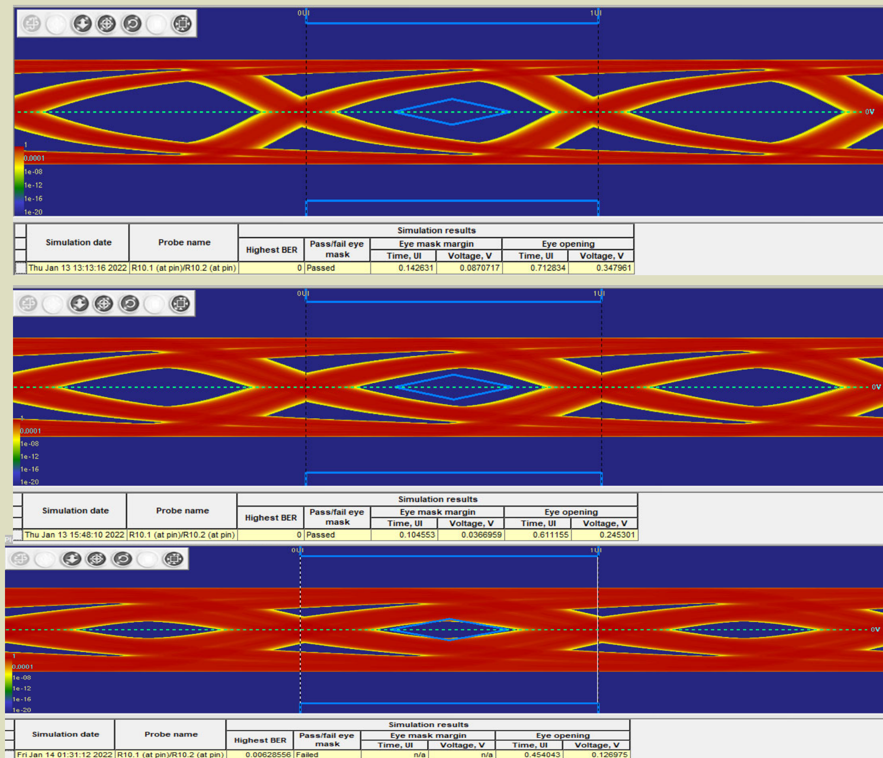
Transmission line loss using pattern prbs-31 @ 25G Load board Trace length loss at 2,3,4 inches



Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Thu Jan 13 13:13:16 2022	R10.1 (at pin)/R10.2 (at pin)	0	Passed	0.142631	0.0870717	0.712834	0.347961

Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Thu Jan 13 15:48:10 2022	R10.1 (at pin)/R10.2 (at pin)	0	Passed	0.104553	0.0366959	0.611155	0.245301

Simulation date	Probe name	Simulation results					
		Highest BER	Pass/fail eye mask	Eye mask margin		Eye opening	
				Time, UI	Voltage, V	Time, UI	Voltage, V
Fri Jan 14 01:31:12 2022	R10.1 (at pin)/R10.2 (at pin)	0.00628556	Failed	n/a	n/a	0.454043	0.126975

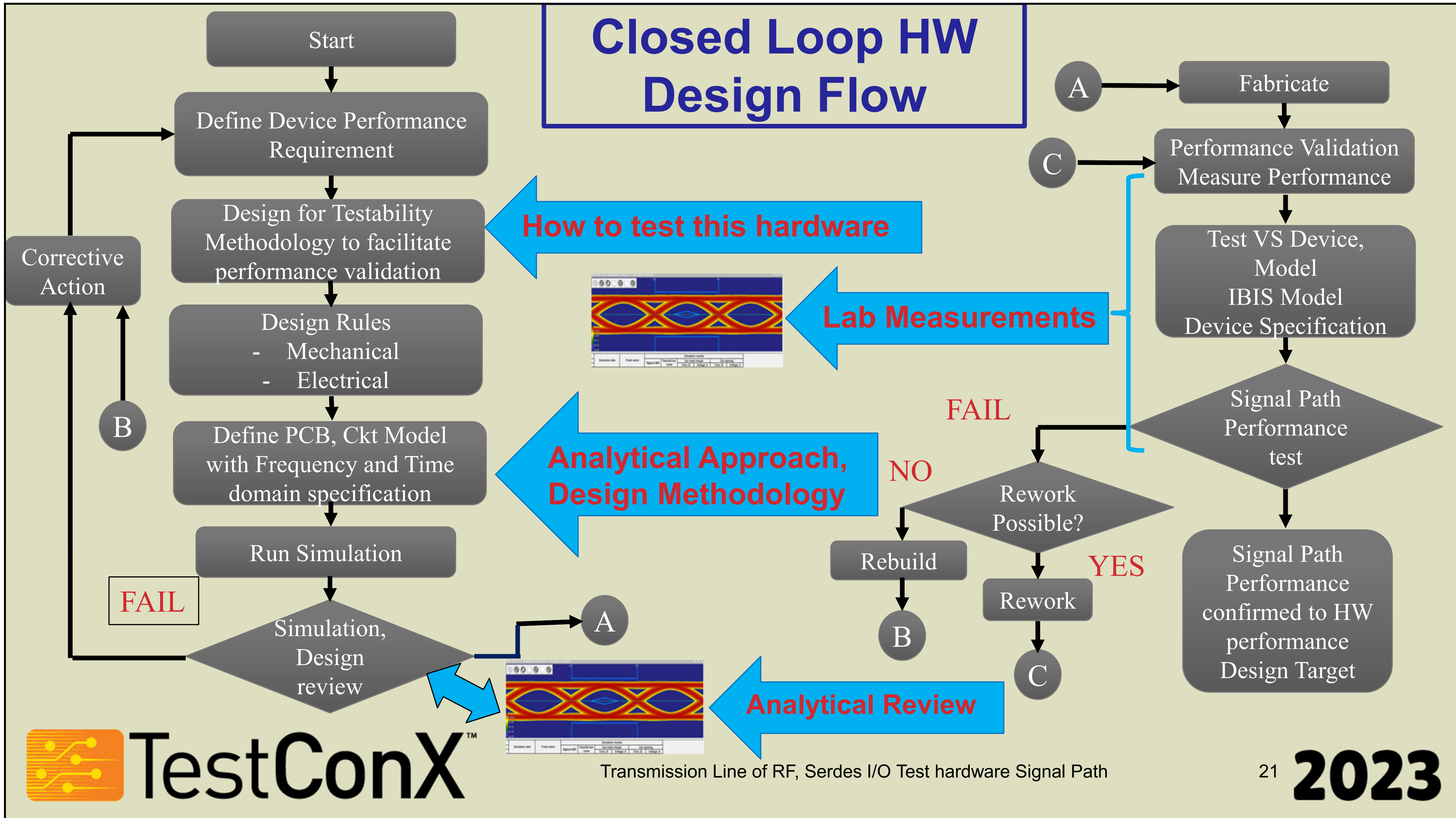
2 Inches trace length

3 Inches trace length

4 Inches trace length

Shrinking Data Eye as function of trace length

- LC Loop back circuit
- Same dielectric
- Same thickness
- Same width
- Trace length specified on TX and RX segment


Closed Loop HW Design Flow
Start
Define Device Performance Requirement
Design for Testability Methodology to facilitate performance validation
Design Rules
- Mechanical
- Electrical
Define PCB, Ckt Model with Frequency and Time domain specification
Run Simulation
Simulation, Design review
FAIL
Corrective Action
B
A
How to test this hardware
Lab Measurements
Analytical Approach, Design Methodology
Analytical Review
A
Fabricate
C
Performance Validation Measure Performance
Test VS Device, Model IBIS Model Device Specification
Signal Path Performance test
FAIL
NO
Rework Possible?
YES
Rebuild
Rework
B
C
Signal Path Performance confirmed to HW performance Design Target
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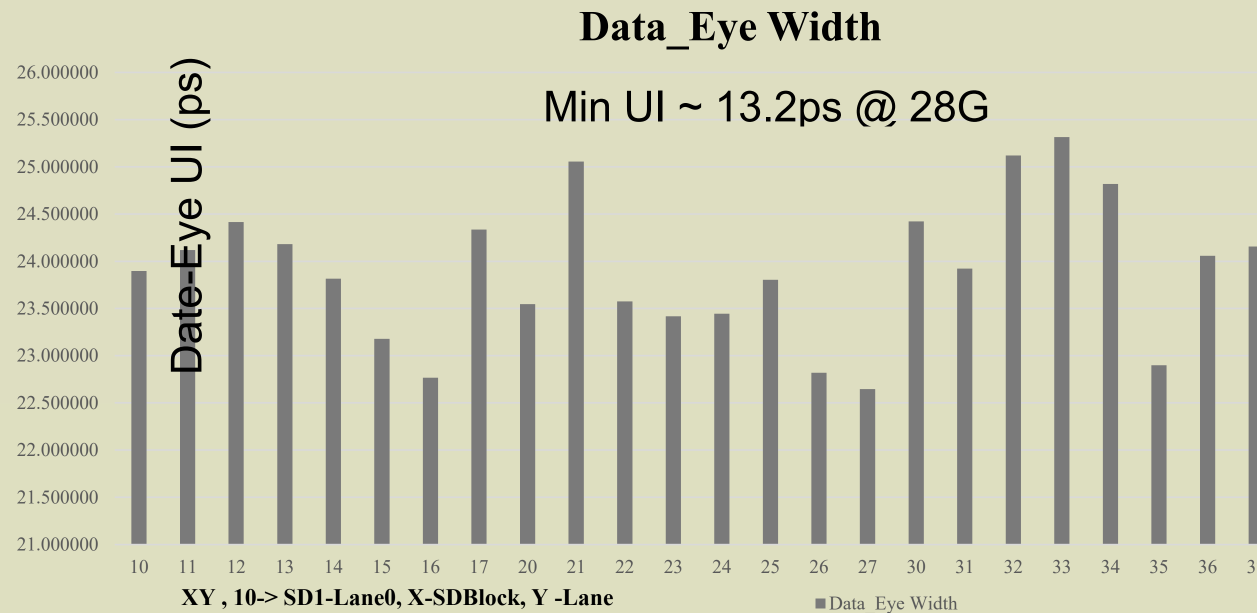
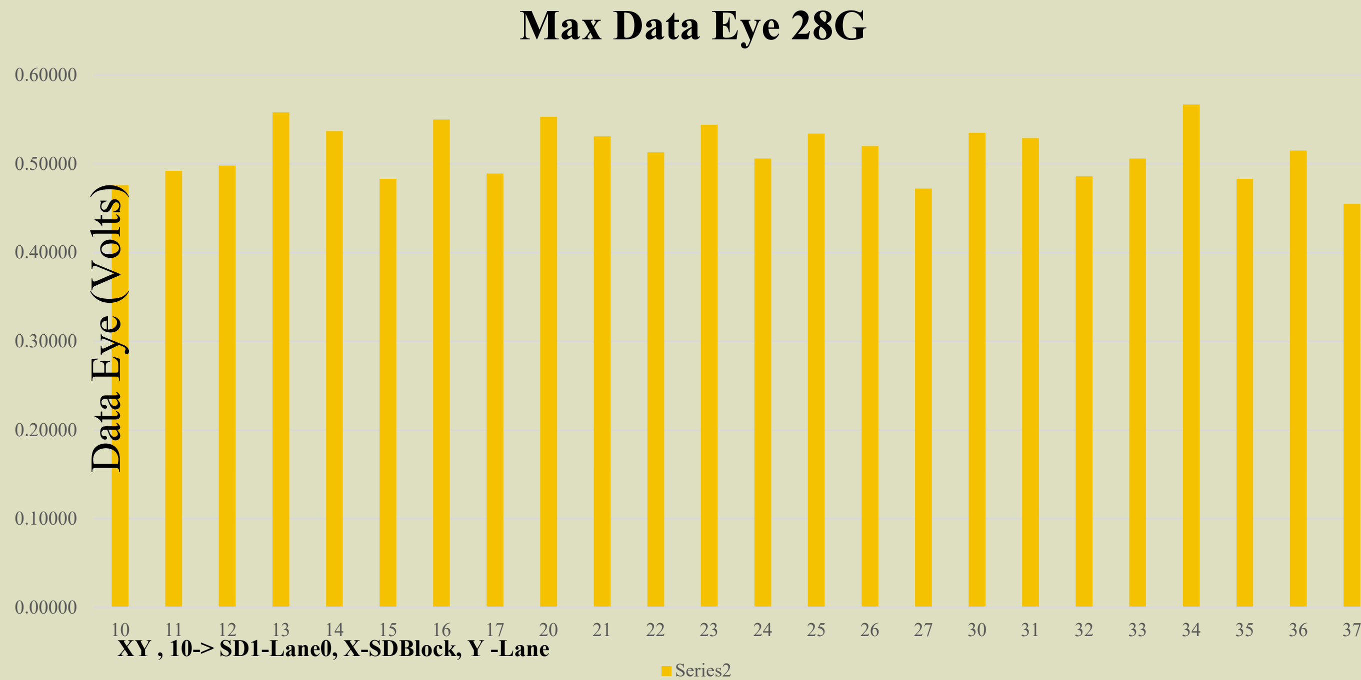
Load board data eye width CJPAT 28G UI(ps) profile per lane



General Stat	PS
Max	25.314498
Min	22.646151
Average	23.905164
STD	0.7471016
Mask	12.000000

Transmission Line of RF, Serdes I/O Test hardware Signal Path

Load board data eye amplitude(V) K28.5 @ 28G profile per lane



General Stat	PS
Max	0.5670000
Min	0.4550000
Average	0.5138333
STD	0.0304112
Mask	0.1750000

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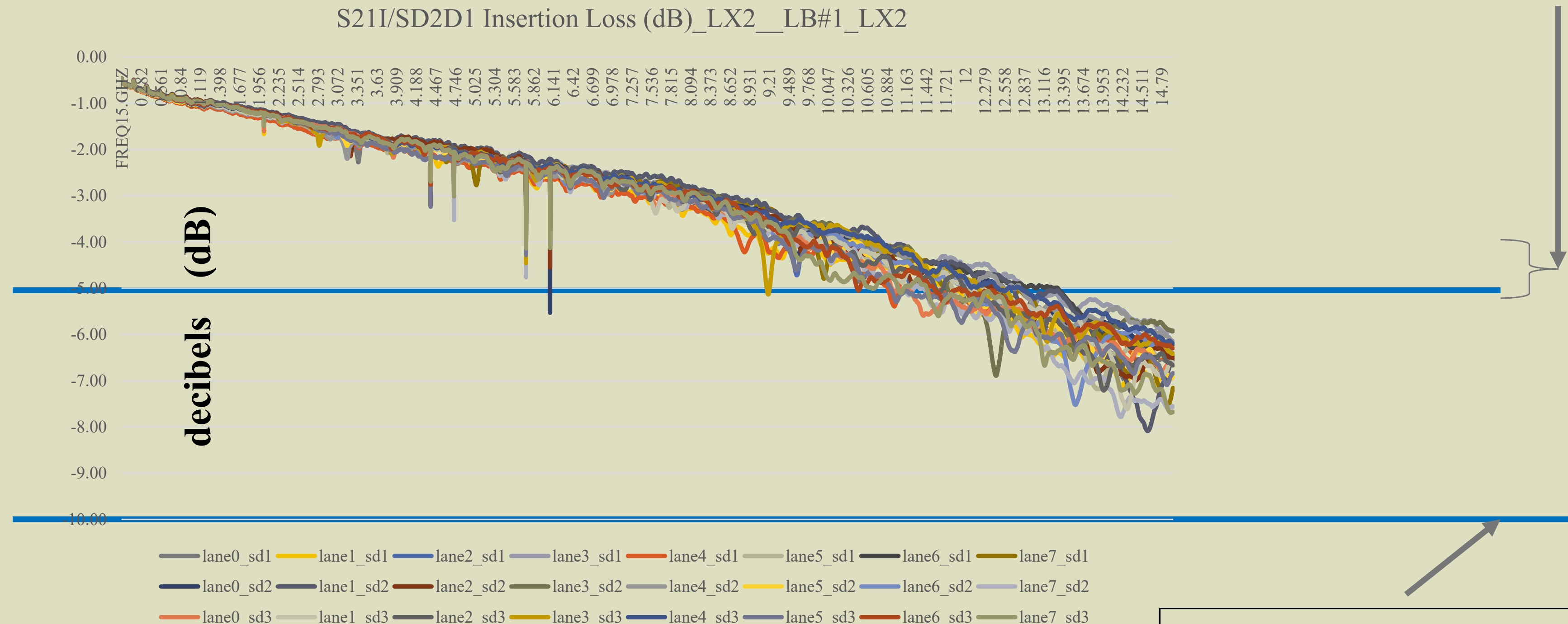
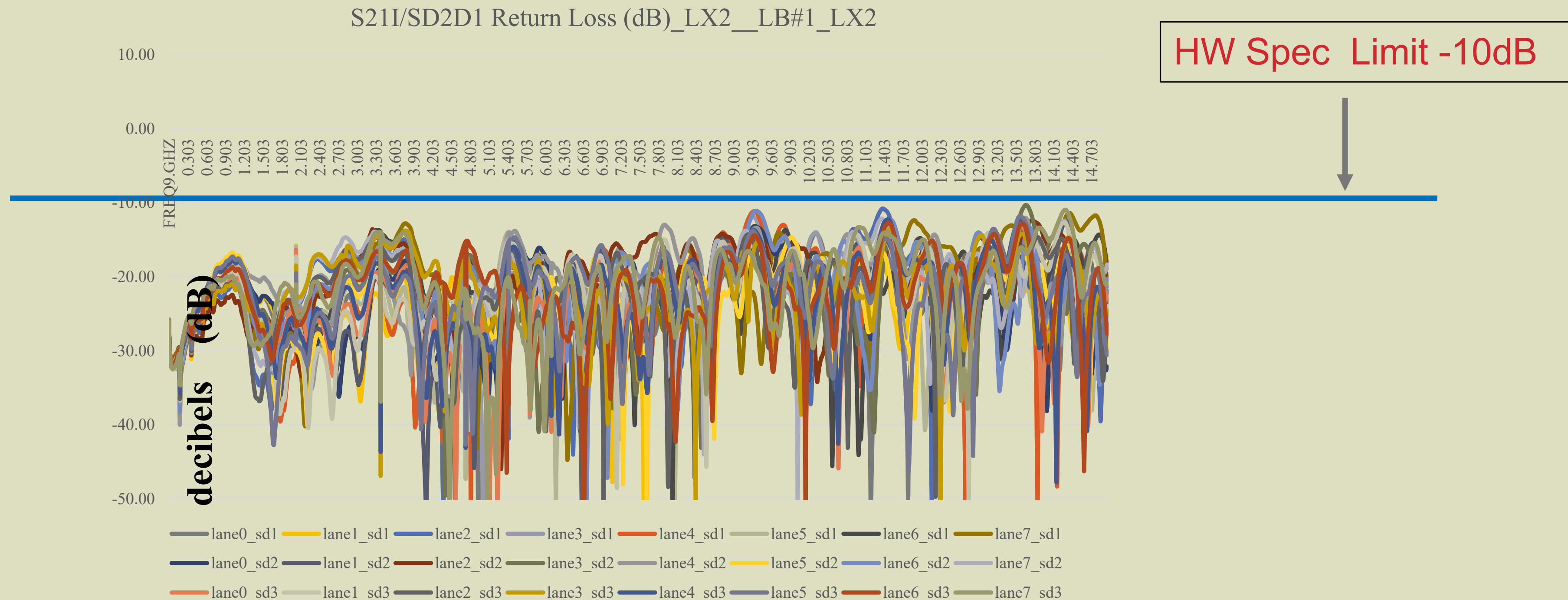
Load board insertion loss profile 24 lanes



Load board return loss profile 24 lanes



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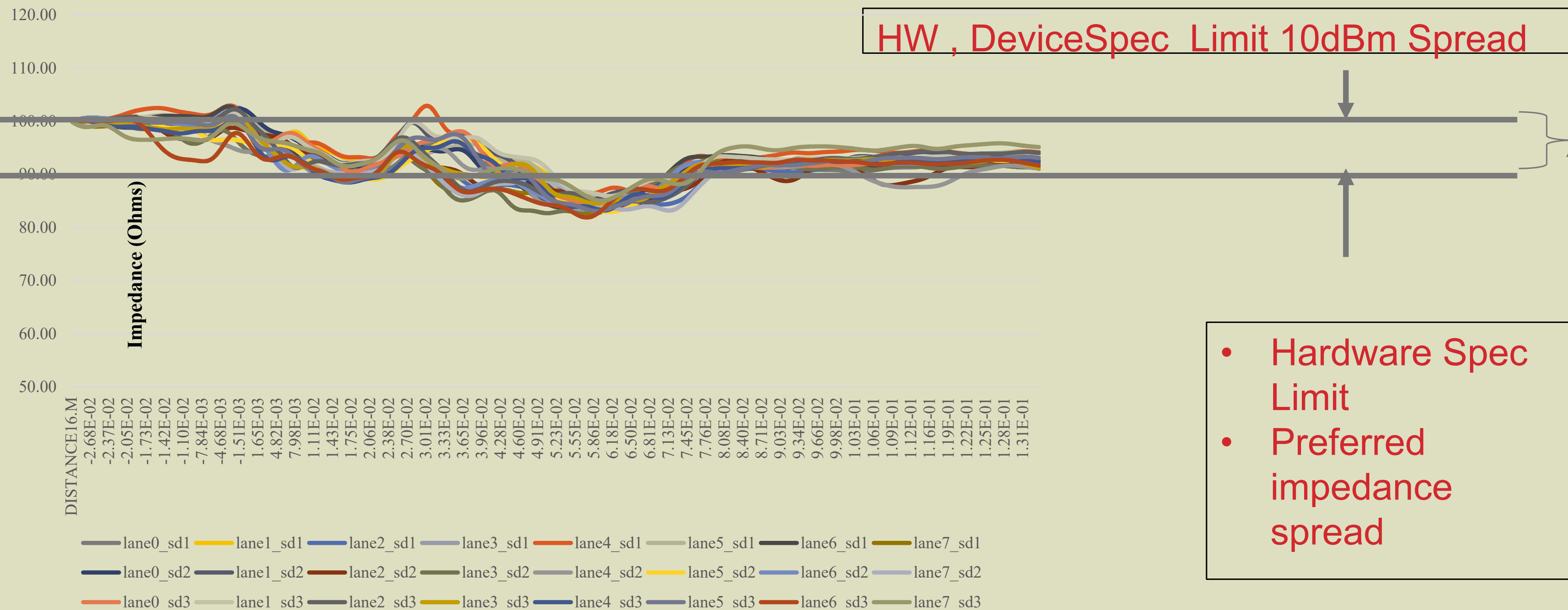
Load board Impedance Profile 24 lanes



Transmission Line of RF, Serdes I/O Test hardware Signal Path

Conclusion

1. Analytical approach to test hardware design provides for objective assessment of the complete signal path. That is on frequency domain, and time domain.
2. Closed-Loop test hardware design ensures device signal path capability to meet device performance requirements
3. It is an objective process with defined performance target and validated for real-world compliance(Measured).
4. Cost effective hardware design and deployment process