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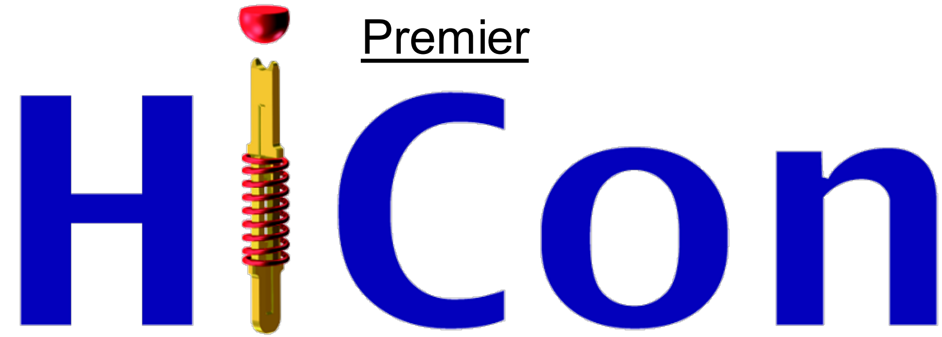

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Design Considerations for Ultra-High Current Power Delivery Networks (PDN)

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Mesa, Arizona • March 5–8, 2023

A Review: Power Delivery Network (PDN)

- Also called as a Power Distribution Network

DUT Socket Pogo pins, Elastomers, Interconnects

Hi-Speed Capacitance

Bulk Capacitors

Device Under Test (DUT) Pads, Solder balls, Substrate Planes, vias, Wire bonds, die pads

Voltage Regulator Module (VRM)

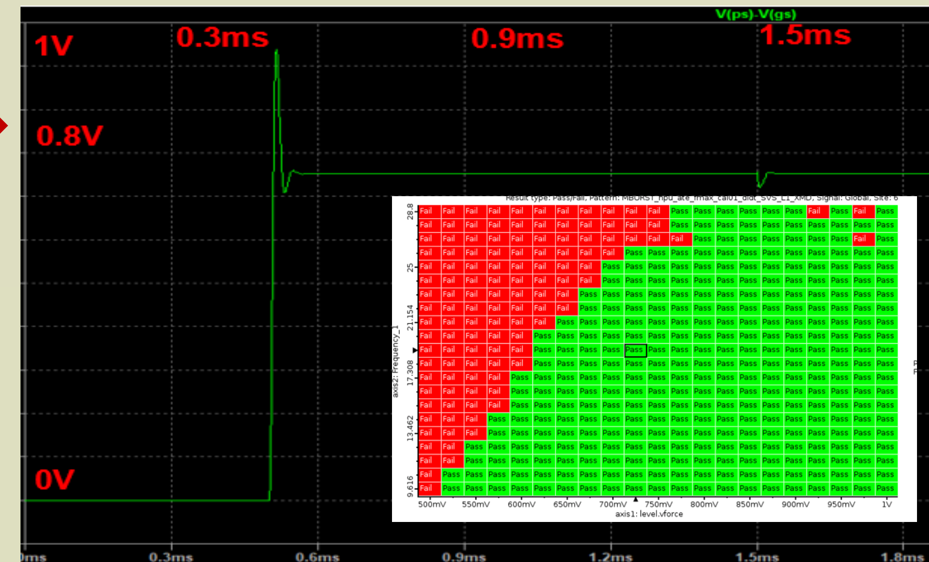
Printed circuit DUT Board Pads, Vias, Power and Return planes

DC Sinks

A localized network to distribute power and return currents

Why Optimization of the PDN is Critical

- Optimized PDN means more power is transferred from VRM (Voltage Regulator Module) to DUT (Device Under Test)
- Ensures a constant supply voltage within a narrow tolerance band
- Prevents power supply ripples under loads



- Clean power supply means higher yields
- Optimized Power delivery ensures a healthy decoupling scheme which provides low impedance on a wide frequency range

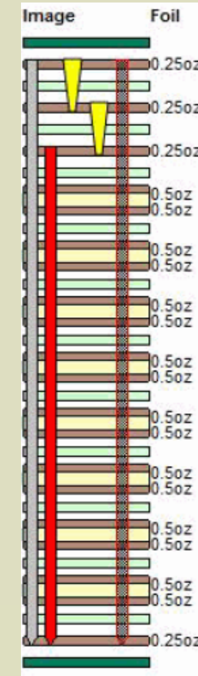
Ultra High Current Power Dissipation

- More and more high current applications
- I^2R – Power dissipation equation – Slightest resistance have pronounced power dissipation at higher currents
  - A 5% drop on the device power for a 2.5kW device is 125W!
    - As the voltage drop increases, the power dissipation gets worse with increased thermal concerns due to higher DC resistance

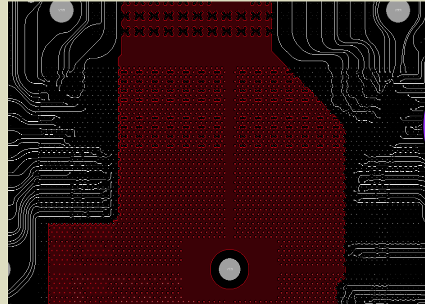
	2009	2022/23	2025
Device type	**CPU, GPUs, Server-side Processing**	**AI, CPUs, GPUs, Multi die probes**	**3D stacked devices, AI accelerators, PI Intense CPU/GPU devices**
~Current (A) & Voltage (V) specs	400A, 1V	2000A, 0.8V	3000A, 0.75V
~5% Drop (V)	0.05V	0.04V	0.0375V
Power dissipated due to DUT board resistances	20W	80W	112.5W

PDN Optimization – What to focus on?

- Prioritize the supplies
  - Not every supply can be optimized to achieve tight targets. Tradeoffs may be required
- Plan the DUT board stacking
  - Plan stacking based on the DUT power dissipation
- Vias are inductive!
  - DUT vias usually accounts for the highest inductance in the PDN path
    - Plane inductance is negligible when compared with via inductances



Where to Start? – Board Stacking



Replicating power in signal layers improve IR-Drop

Thin dielectrics PWR:GND

Barrel plating

Conductive epoxy fill

2.118 oz, TOP,
5.04 mils, Er = 2.97
0.963 oz, L02PN_GND1
2.58 mils, Er = 3.11
2 oz, L03PN_PWR1 VDD
5 mils, Er = 2.95
0.963 oz, L04PN_GND2
2.58 mils, Er = 3.11
2 oz, L05PN_PWR2
5 mils, Er = 2.95
0.963 oz, L06PN_GND3
2.58 mils, Er = 3.11
2 oz, L07PN_PWR3
5 mils, Er = 2.95
0.963 oz, L08PN_GND4
2.58 mils, Er = 3.11
2 oz, L09PN_PWR4 VDD
5 mils, Er = 2.95
0.963 oz, L10PN_GND5
2.58 mils, Er = 3.11
2 oz, L11PN_PWR5
5.14 mils, Er = 2.95
0.444 oz, L12PN_GND6
0.444 oz, L38PN_GND15
2.58 mils, Er = 3.11
0.963 oz, L39PN_PWR15
4.78 mils, Er = 2.97
0.963 oz, L40PN_PWR16

Critical power near device

Cu plane area?

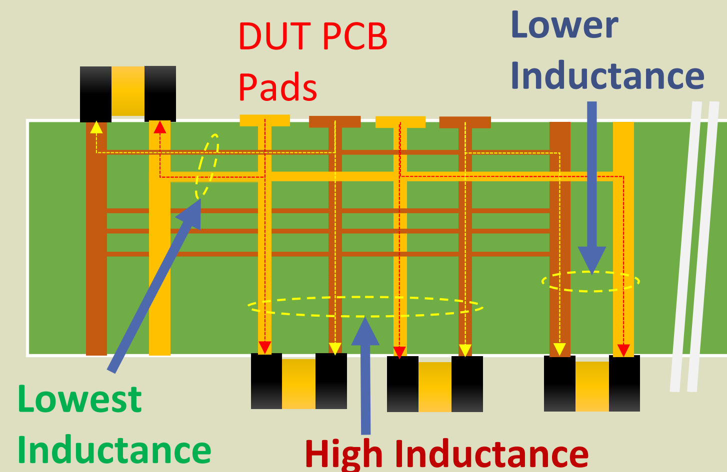
>= 2Oz Cu cores

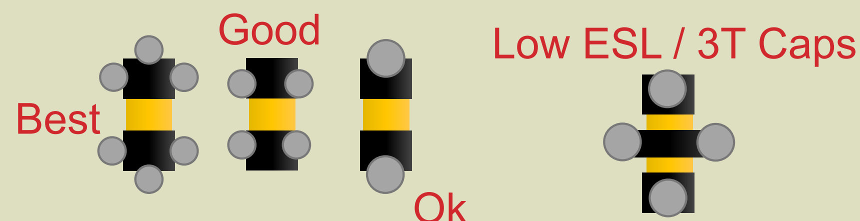
.. and Replicate

Thicker copper and large copper areas acts as heat sink, especially return planes

Optimizing Layout for a Better PDN Design

- Move or replicate critical power closer to DUT to reduce via inductance
- Increase cap via size, use multiple vias at capacitor pads
- Put high speed caps on the top side of the board
- Use low ESL [Equivalent Series Inductance] caps
- Increasing DUT via size → Use as large as DFM (Design rules for Manufacturing) allows → Limited by device pitch
- Increasing DUT power vias → Limited to DUT pitch

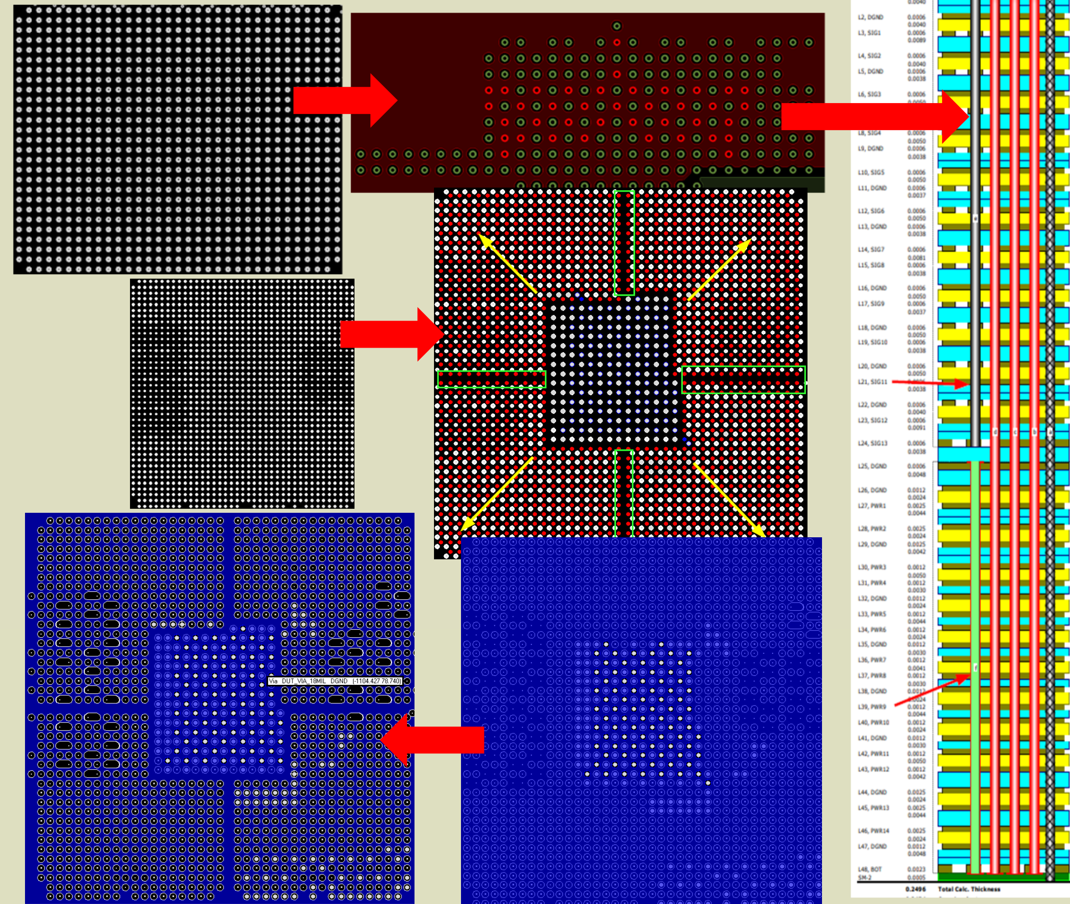




Via Placement Optimization

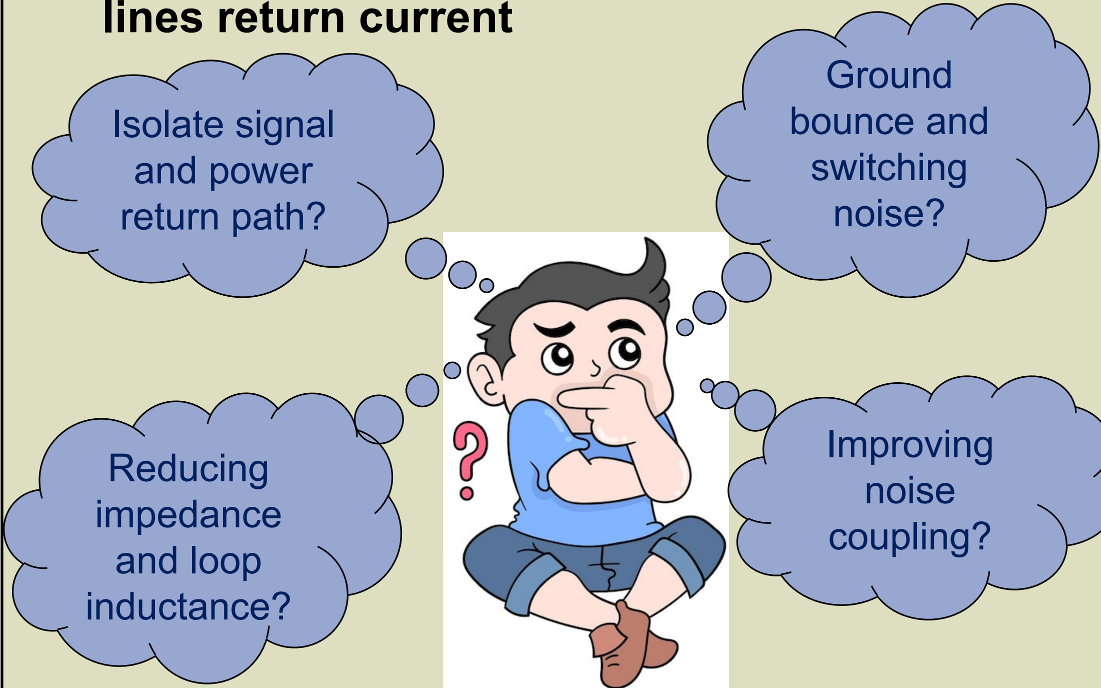
Copper web at DUT increases IR Drop and plane inductance

- Reduction is possible with use of a blind via to eliminate the Swiss cheese effect
- **Trade off:** Via lengths becomes larger
- For smaller vias, this means more via inductance
- **Good for:** Large number of bigger vias (PWR+GND)
- **Alternatively:** Power can be replicated closer to DUT to reduce via inductances
- **Larger BGA pitches:** Smaller signal Via offset can create a channel for copper flow to the DUT core power [larger vias]



Important Consideration: Return Path!

PDN return path is mostly shared with signal lines return current



GND : PWR : GND	GND : PWR : PWR : GND
Better noise isolation	High power stack density
Better power impedance	Adequate power impedance
More GND – Better IR drop on return path	Fewer GND – Higher drop on return path
Lower power stack density	Poor noise isolation
Use for: Most cases ideally. Particularly high current, noise sensitive and critical supplies	Use for: Layer constraints due to DUT pitch. Low current and non-critical supplies
Use Thin dielectrics between PWR/GND	*Use Thin dielectric between PWR/GND and thicker (~2x) between PWR:PWR*

Running simulations / analysis early in the design cycle will ensure a product with acceptable performance

PDN Power Integrity Analysis

PI Analysis

Pre-Layout

Target Impedance

Decoupling Strategy

Design Layout

Post-Layout

DC Analysis

Current density and via currents

Voltage-Drop including *return path & combined return path*

AC Analysis

Impedance vs. Freq plots

Target Impedance met?
- Decoupling Optimization
- Layout Optimization

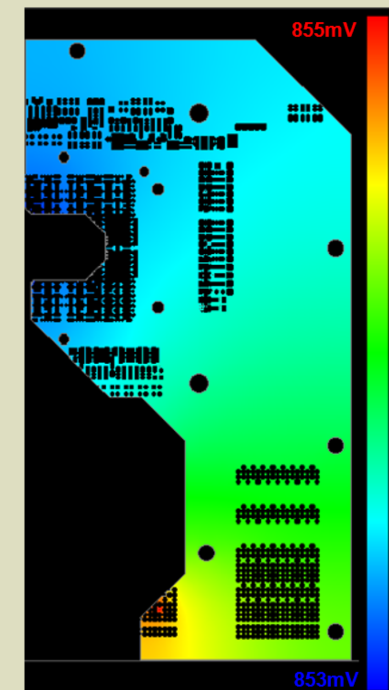
Thermal Analysis

Board temperature rise with increasing currents through printed circuit board structures

PDN Optimization

DC analysis – Behavior of the DUT board at DC

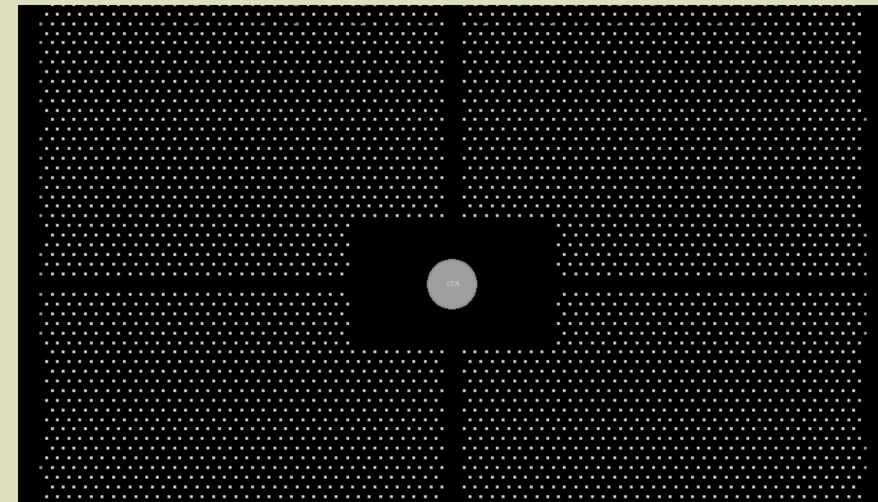
- Analyze voltage drop, current density and via currents due to electrical resistances on the board current path
- Good for identifying bottle necks due to copper depletion
- Usually improved by increasing copper area, replicating Power planes and increasing copper weights on stacks.



Case Study – 2.4kW Device DC Analysis

Design Considerations
IR Drop Optimization

- Package design with a channel to provide better current flow
  near the core
- Calculate Cu area/weight w.r.t power supply current
- 2 Oz Cu layers
- Multiple high current power supply layers
- 1mm design pitch allowed bigger 14.5 mil drill power and return vias
- Power shapes added in signal layers based on the available space



IR Drop Simulation Results

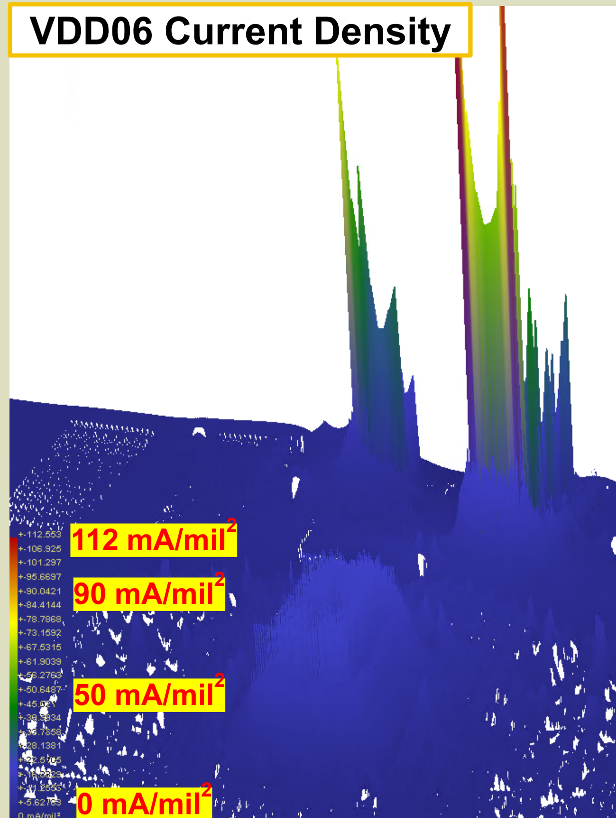
Simulations met required IR-Drop targets due to optimization

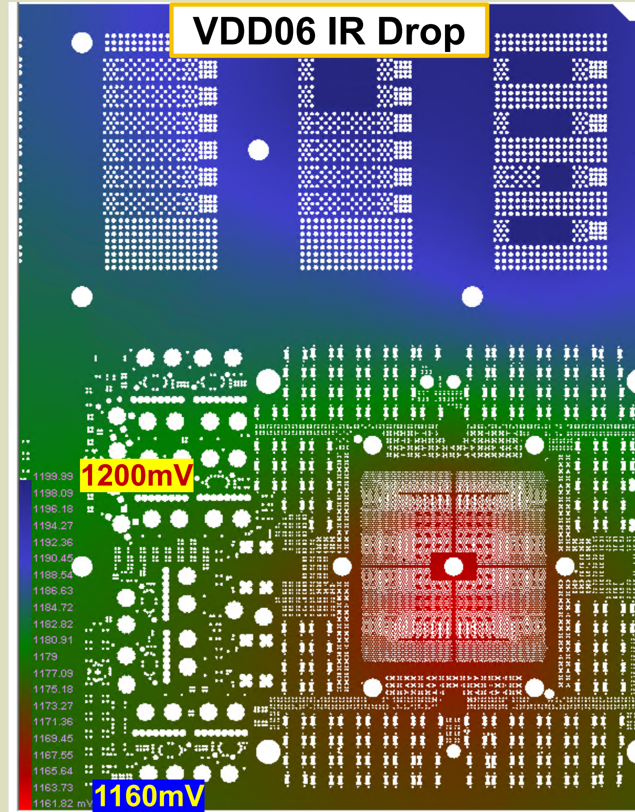
Power	VDD_01	VDD_02	VDD_03	VDD_04	VDD_05	VDD_06	VDD_07	VDD_08	VDD_09	VDD_10
Voltage (V)	0.75	0.75	**0.75**	1.1	1.1	**1.2**	1.2	**1.35**	**1.35**	**1.35**
CURRENT (AMP)	12	40	**115**	36	65	**440**	38	**150**	**290**	**290**
TARGET (mV)	40	55	**50**	40	50	**55**	50	**40**	**55**	**55**
IR DROP (mV)	18.1	52.8	**42.2**	28.6	46.1	**50.1**	48.4	**40.3**	**38.6**	**45.7**
PWR (Watt)	9	30	**86.25**	39.6	71.5	**528**	45.6	**202.5**	**391.5**	**391.5**
PWR Dissipation (Watt)	0.22	2.11	**4.85**	1.03	3	**22.04**	1.84	**6.05**	**11.19**	**13.25**

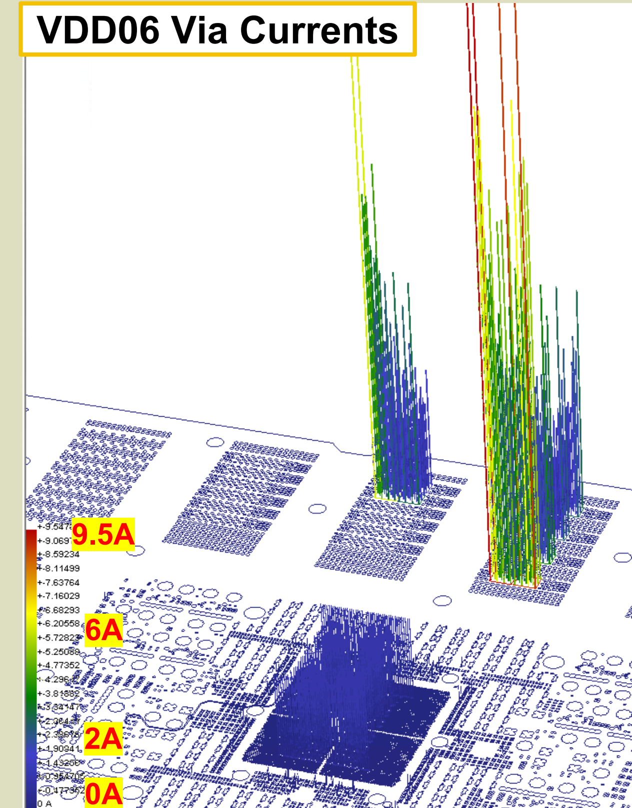
Power	VDD_11	VDD_12	VDD_13	VDD_14	VDD_15	VDD_16	VDD_17	VDD_18	VDD_19	VDD_20
Voltage (V)	**1.35**	1.2	1.1	1.8	1.8	3.3	3.15	1.1	1.8	1.8
CURRENT (AMP)	**290**	40	40	32	10	1.5	1	2	2	2
TARGET (mV)	**55**	55	50	50	50	50	50	50	50	50
IR DROP (mV)	**41.6**	37.5	52.4	36.4	30.3	10.9	16.1	10.8	19	37.4
PWR (Watt)	**391.5**	48	44	57.6	18	4.95	3.15	2.2	3.6	3.6
PWR Dissipation (Watt)	**12.06**	1.5	2.1	1.16	0.3	0.02	0.02	0.02	0.04	0.07

Total PWR = ~2.4kW, Dissipation(PCB) = 83W (<3.5%)

DC Analysis Plots

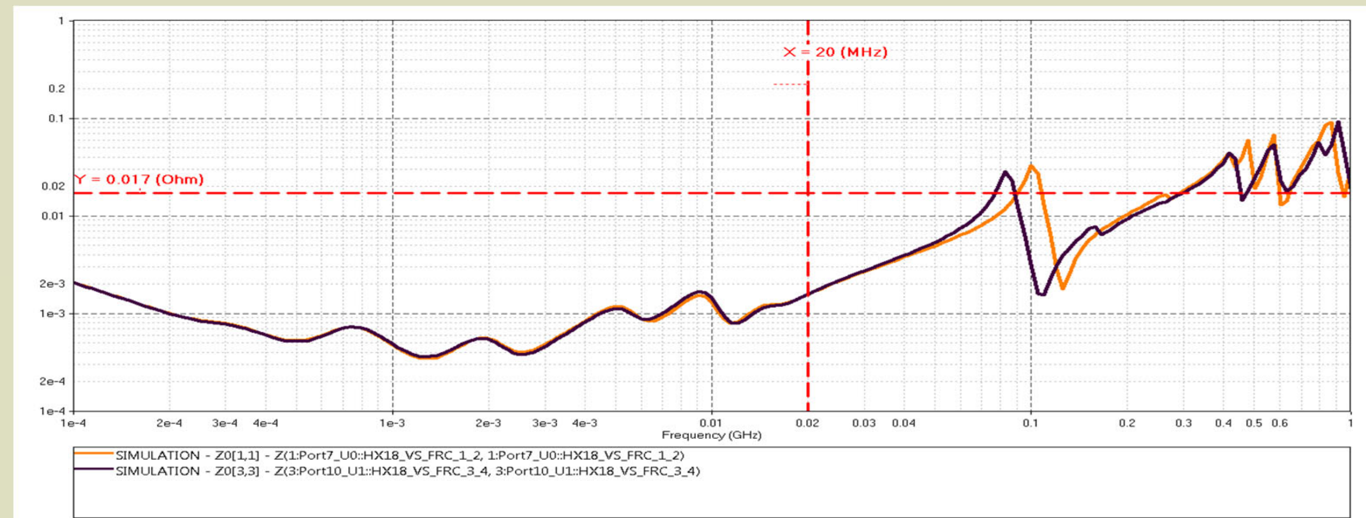






PDN AC Optimization

- AC analysis – How does the load ripples at varying Frequency
  - Impedance analysis is used widely to create effective decoupling strategy
  - Can be described as resistance as it relates to frequency
  - Analysis of how the DUT board supplies behave with switching currents at frequencies



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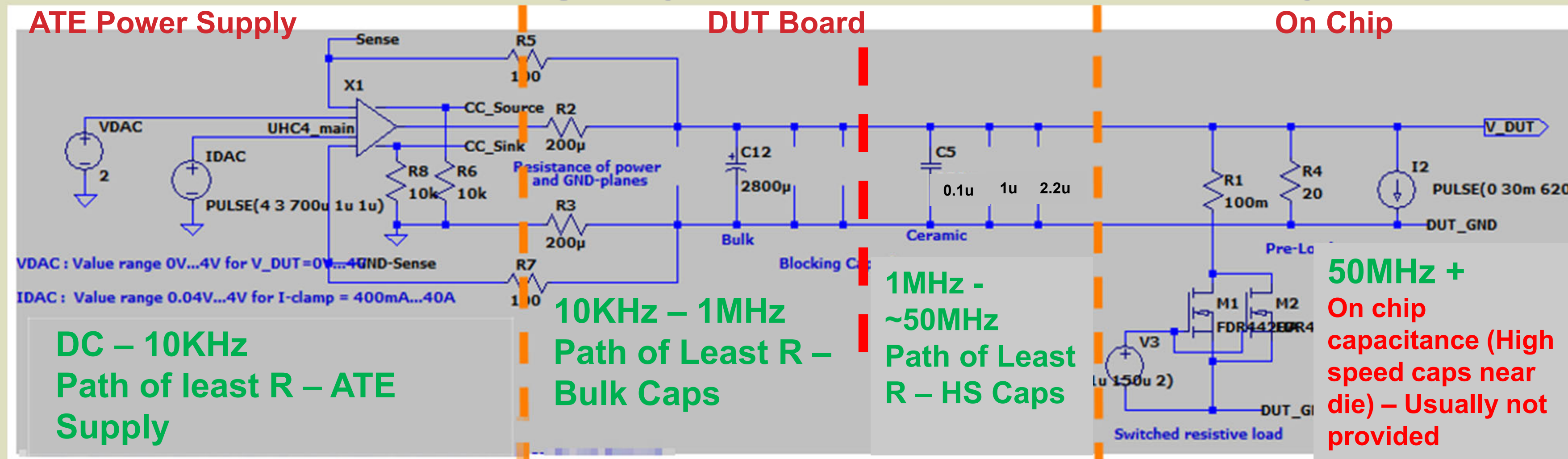
Power Integrity: Impedance Analysis



Impedance continues to be the major problem in the PDN design

- At DC, we are talking about electrical resistance offered on the current path
- As the frequency increases, the path to least resistance is the capacitor
  Generally: [Higher, bulk capacitance = Lower frequency, Lower capacitance, Ceramic = Higher frequency]

Supply Target Impedance

- Target Impedance is required for each power rail
- Target Impedance for power supplies needs to factor in:
  - Maximum Ripple voltage tolerable by the chip (e.g., 5% of Vdd)
  - Maximum Transient current (e.g., 50% of Imax)

$$Z_T = \frac{(V_{DD} \times \%Ripple)}{I_{Transient}}$$

- $I_{Transient}$ while an important spec is not always known. General rule of thumb for estimation:

$$I_{Transient} \sim 0.5 \text{ x } I_{max}$$

- Keeping Target impedance much lower than specs means an overdesigned PDN which will result in higher cost

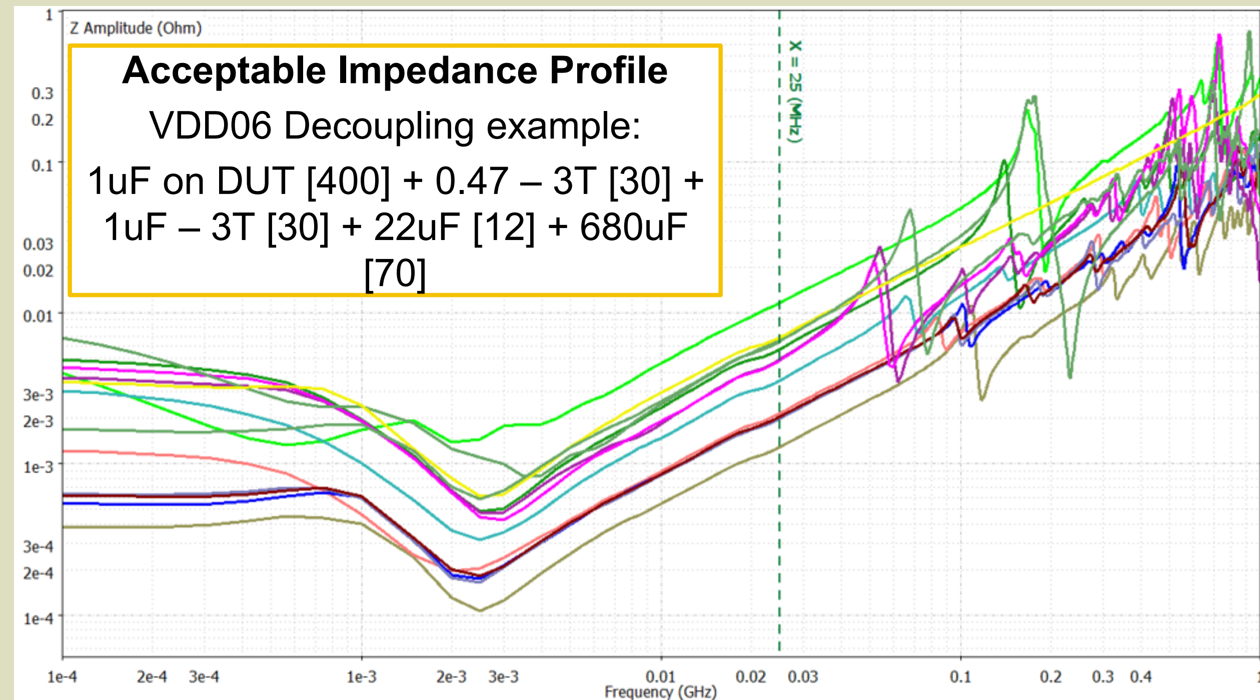
E.g., For a 10A, 0.75V V_{DD} supply, with a 5% ripple specs and $I_{Transient}$ as 50% of I_{max}, Target impedance is **7.5 mΩ**

Case Study: 2.4kW Device AC Analysis

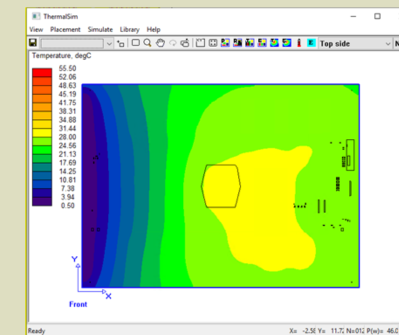
Design Considerations: Impedance Optimization

- Optimization of capacitor values to improve impedance response across frequency
- Optimizing capacitor vias for reduced mounting inductance.
- Moving critical Power layers closer to the DUT
- Maximized via drill size
- 3T low ESL caps

Curve	25 (MHz)
Z1[1,1] - (1::VDD_04, 1::VDD_04)	0.0115987 (Ohm)
Z1[2,2] - (2::VDD_05, 2::VDD_05)	0.00355183 (Ohm)
Z1[3,3] - (3::VDD_06, 3::VDD_06)	0.00128634 (Ohm)
Z1[4,4] - (4::VDD_07, 4::VDD_07)	0.00571647 (Ohm)
Z1[5,5] - (5::VDD_08, 5::VDD_08)	0.00215037 (Ohm)
Z1[6,6] - (6::VDD_09, 6::VDD_09)	0.00201183 (Ohm)
Z1[7,7] - (7::VDD_10, 7::VDD_10)	0.00198917 (Ohm)
Z1[8,8] - (8::VDD_11, 8::VDD_11)	0.00203586 (Ohm)
Z1[9,9] - (9::VDD_12, 9::VDD_12)	0.00490472 (Ohm)
Z1[10,10] - (10::VDD_13, 10::VDD_13)	0.00481301 (Ohm)
Z1[11,11] - (11::VDD_01, 11::VDD_01)	0.00669294 (Ohm)
Z1[12,12] - (12::VDD_02, 12::VDD_02)	0.00684024 (Ohm)
Z1[13,13] - (13::VDD_03, 13::VDD_03)	0.00644002 (Ohm)



PI – Thermal Co-Simulations

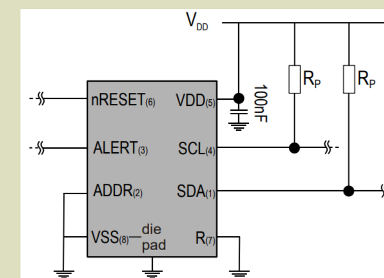


- Available with most PI – Thermal sim suites
- Thermal PI Co-Simulations considers the heat generated due to the current flowing through the metal structures on the board from the VRM to the DC sinks (DUT or other current sink devices)
- Predicts the temperature rise with flowing electrical current considering combined currents of different supply rails on the return path
  - Important consideration: Which supplies activates at the same time?
- Useful for especially very high-power designs to identify any thermal concerns and high temperature spots which can damage board hardware
- Flooding GND copper on outer layers with thermal vias acts as heat sink
  - Additional heatsink structures can be placed on the outer layers to dissipate heat
- Frames and stiffeners also acts as heat sinks and can dissipate heat energy
  - Purge air solution and cold air can be used to dissipate heat as well

PI – Thermal Co-Simulations

Thermal concerns can be alleviated by adding heat sensor circuits on the PCB Board

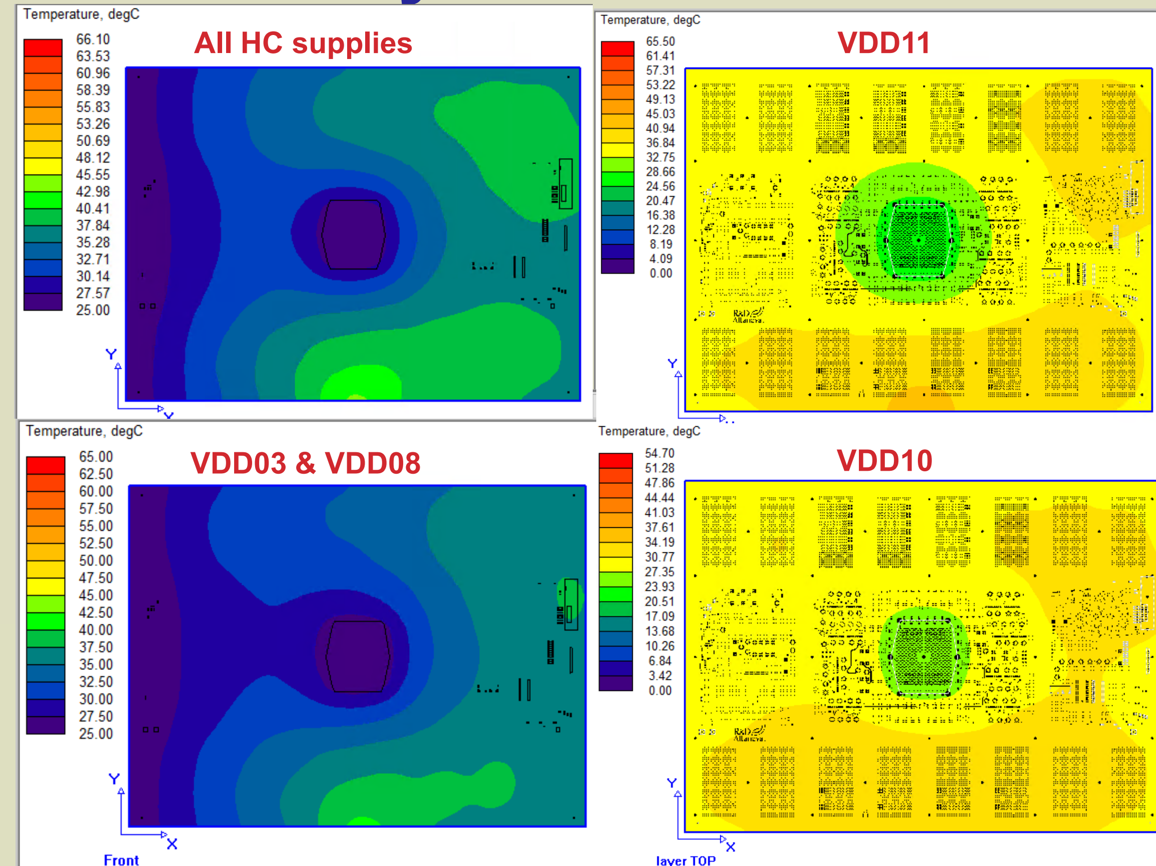
- Multiple sensor can be placed on Top/bottom side at different location to sense temperature2
- Sensors can be programmed using serial I2C interface. Sensor alerts the tester via alert pin when certain temperature threshold is reached.
- Alert pins connects with a pin electronics channel to read Alert condition
- Example sensors:
  - Senserion SHT35
  - Texas Instruments TMP1075



Example Circuit

Thermal Analysis

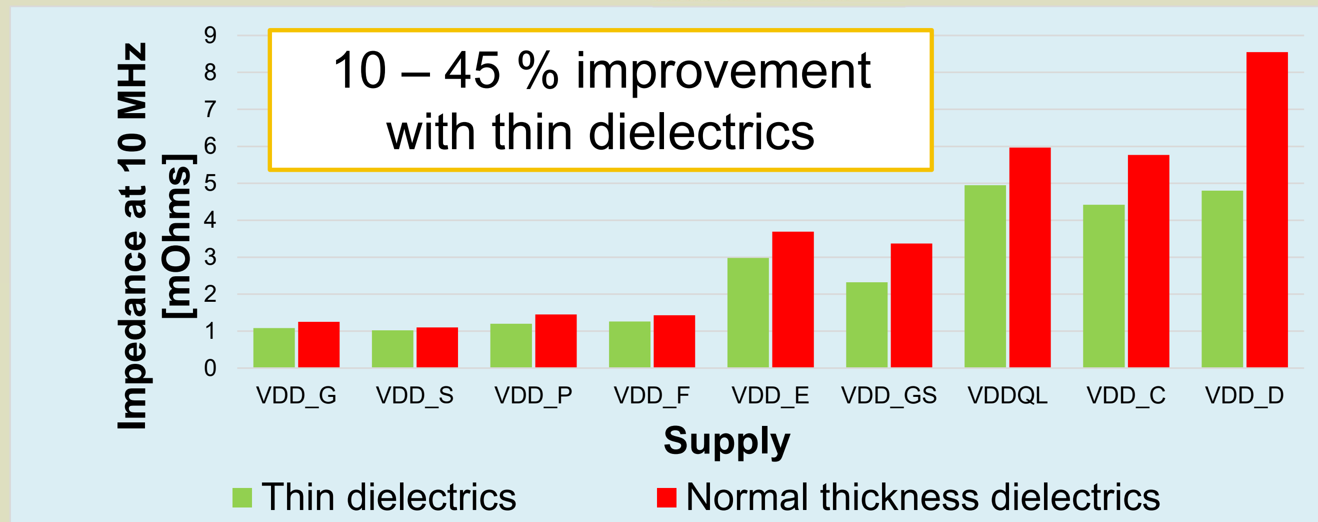
- Thermal Simulations confirms satisfactory board temperature due to supply currents
- Supplies were run individually as well as multiple supplies activated with a common return path
- Doesn't consider for heat generated due to components or DUT itself

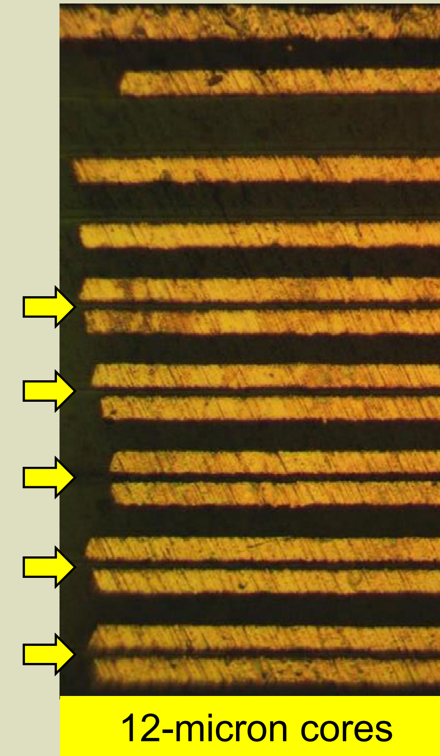


Useful Tools: Thin Core Dielectrics

12um cores for regular PCBs & MLOs
PWR / GND structures only
Higher layer density
Lower plane inductances

- Cost
- Handling risk
- Availability





12-micron cores

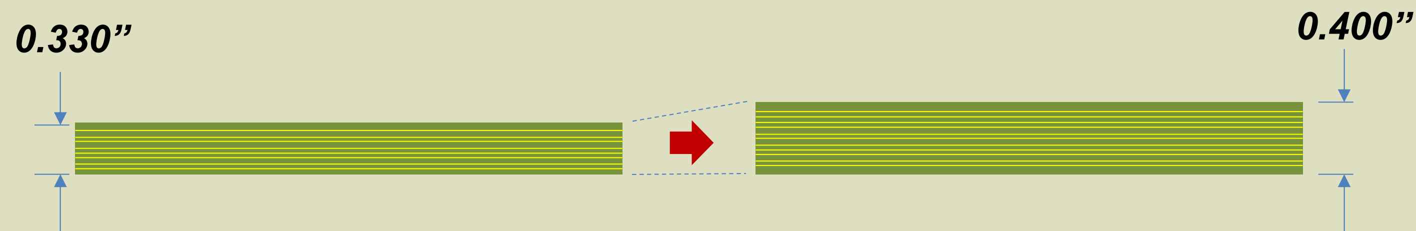
Useful Tools: Thicker Stacks

Existing ATE FABs offer board thickness up to 0.330” with Single Lamination

- More Layer for Power planes – Higher density stacks
- CPU / GPU and AI accelerator ATE boards
- Memory probe and other probe testing
- Increased number of layers with 2Oz copper cores can help design a better PDN

Advanced FABs can create boards up to 0.400” thickness

- Increases the layer density of the stacking by 21% from 0.330” thick boards
- Only usable from 0.65mm and higher due to Aspect ratio limitations
- Production ready at R&D Altanova in Q2’23



Conclusion

- Analysis using simulations tool is the key to success!
- Design optimization greatly helps achieve critical targets
- Understanding of key practices and PI performance parameters are essential to achieve better PDN results
- Thermal concerns are real with ever increasing device power consumptions and needs a careful review