Drive More Than Two Pin Levels With DPU-16

Evan Chen & Kristine Chen
Teradyne SEG, China ADC

TestConX中国 China

Virtual ▪ November 1-4, 2022

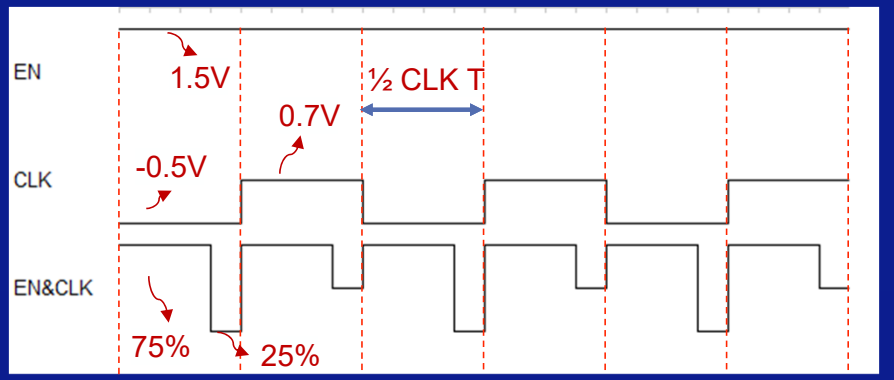
TERADYNE

Contents

- Background and Requirements
- ETS-88 and DPU-16
- Two Methods to Drive 3 Pin Levels
- Drive More Than 3 Levels
- Q&A

Background and Requirements

- With the fast development of semiconductor technology in the world, there's a tendency to reduce the device size and redundant pin count.
- A device pin combines EN pin and CLK pin to limit the pin count in scan chain structure.
- The combined signal drives three levels in total, normally we use DPU to drive high/low, that is 2 levels
- 0-75% of each period is EN signal, 75%-100% is CLK signal



TestConX中国 China

Drive More Than Two Pin Levels With DPU-16

2022

3

Introduction of ETS-88

- ETS-88 is a mixed signal automated testing environment, testing a wide variety of devices including: simple analog, high precision, high voltage, high current / power, automotive etc.
- Eagle test system offers high throughput, low cost for Single site, Multi-site and Index Parallel Applications

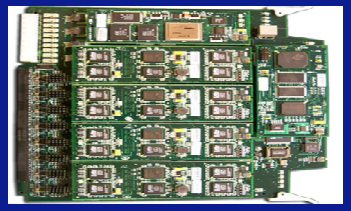
TestConX中国 China

Drive More Than Two Pin Levels With DPU-16

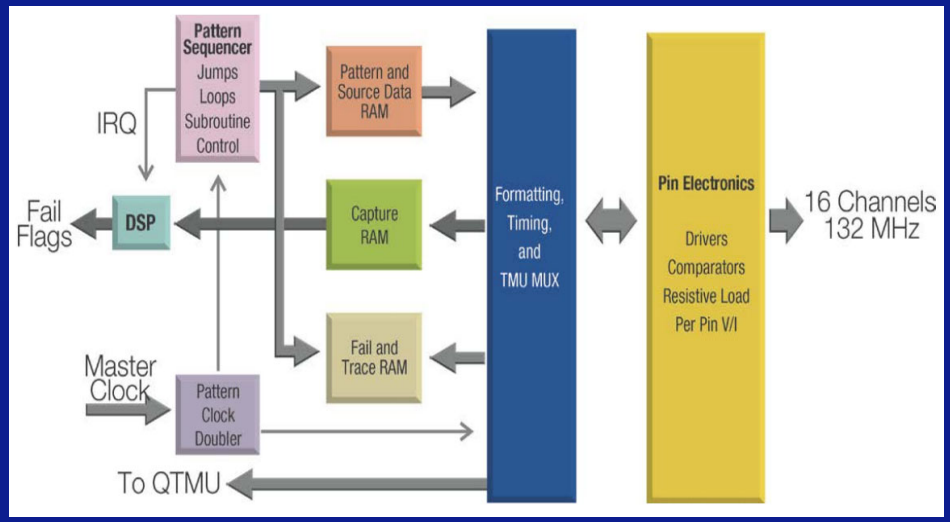
2022

4

Introduction of DPU-16 board



- DPU-16 is a commonly used instrument for digital tests
- It provides 16 full-featured digital I/O channels
- Supporting vector rates up to 132 MHz(DDR mode)



DPU-16 Block Diagram

TestConX中国 China

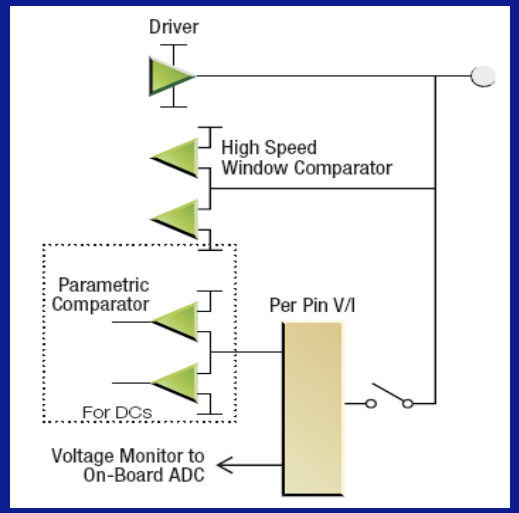
Drive More Than Two Pin Levels With DPU-16

2022

5

Pin Electronics

- Independent programmable drive and receive levels per pin
- Drive pin state: 0, 1, T, Z
- Receive pin state: H, L, X, V, M



Pin Electronics Diagram

TestConX中国 China

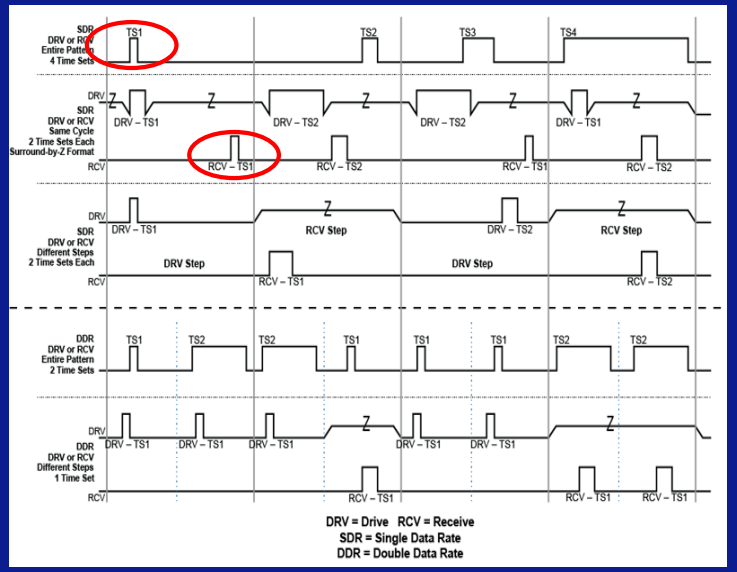
Drive More Than Two Pin Levels With DPU-16

2022

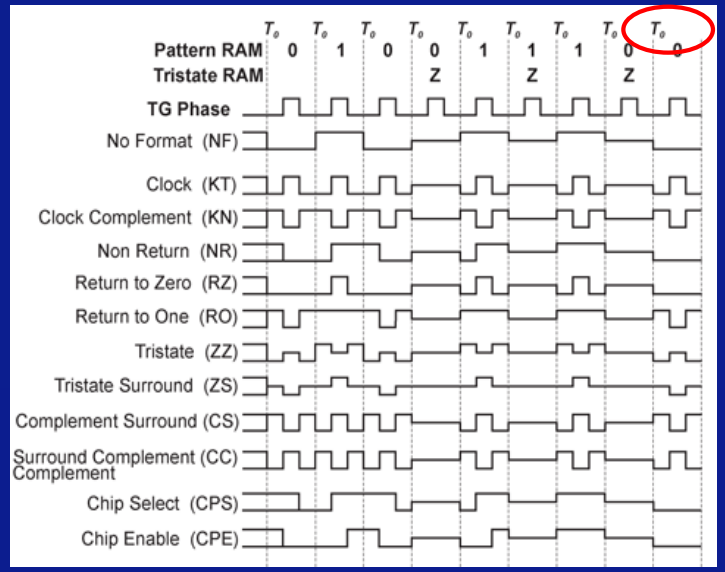
6

Data Format and Edge setting

- Data format: specify the level change within a period
- Edge set : specify when to have the level change



Timeset Application for DPU-16 Pin Modes



DPU-16 Digital Data Formats

T0:Period Clock, generate the timing reference

TestConX中国 China

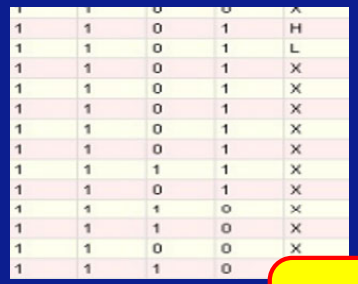
Drive More Than Two Pin Levels With DPU-16

2022

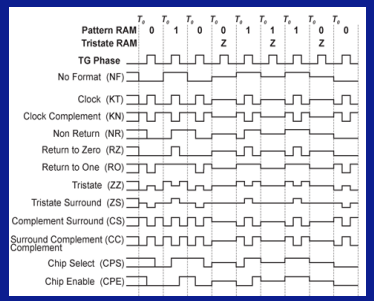
7

Drive the Waveform

- With PE, combine the settings to get the actual drive waveform we need.

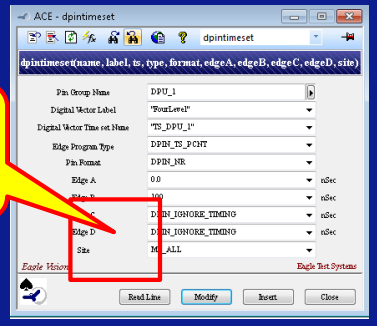


Pattern Dat

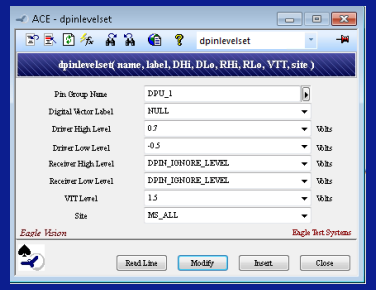


Format Setting

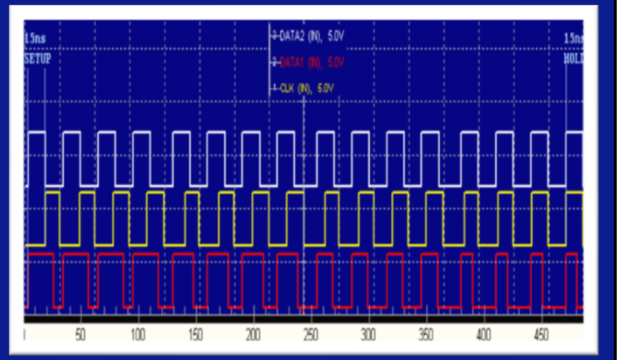
Edge setting for Leading and Trailing



Edge Setting



Level Setting



The ideal drive waveform

TestConX中国 China

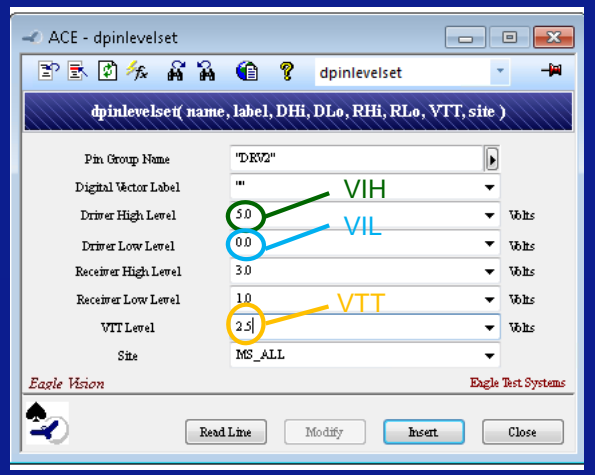
Drive More Than Two Pin Levels With DPU-16

2022

8

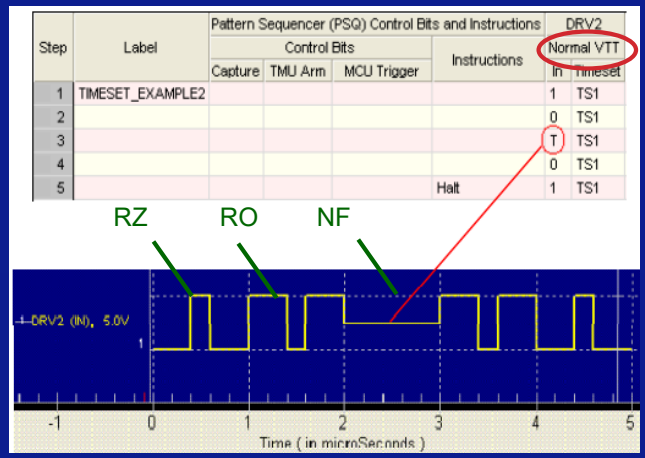
VTT Drive Mode(the 3rd Level)

- Three drive levels: drive high, drive low, VTT level
- VTT level is 50 Ω output impedance, -1.0 to +7.0 V
- **Restrict**: format is not available on VTT level



Level Setting

Define Pin as VTT type



VTT Mode Setting in Pattern

TestConX中国 China

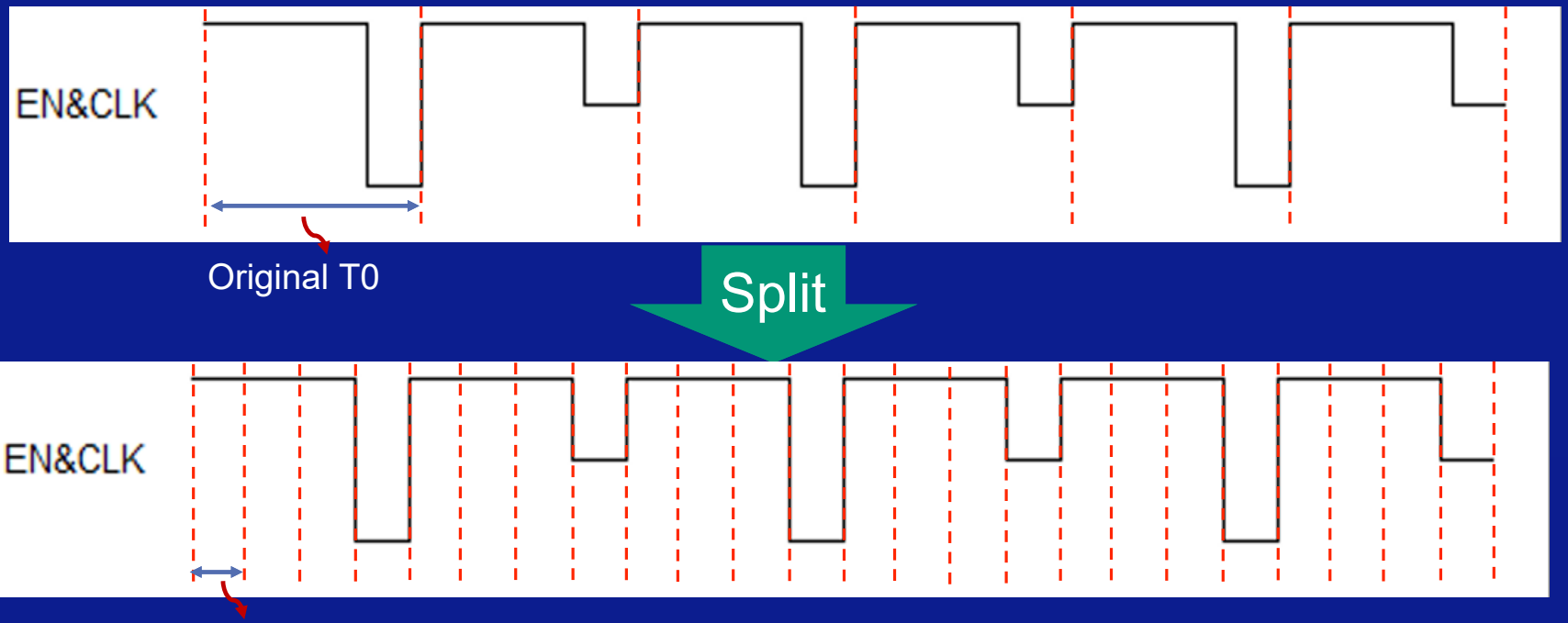
Drive More Than Two Pin Levels With DPU-16

2022

9

Method 1: Split Period

- T0: split x4



TestConX中国 China

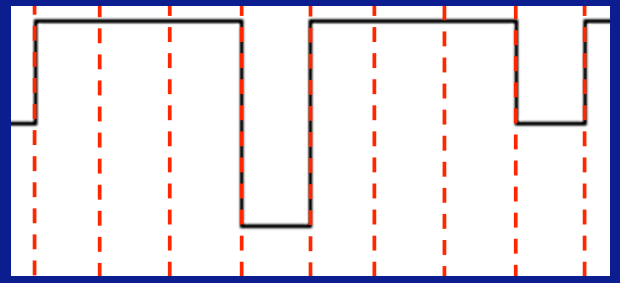
Drive More Than Two Pin Levels With DPU-16

2022

10

Method 1: Split Period

- Pattern to describe the waveform



Step	Label	Pattern Sequencer (PSQ) Control Bits and Instructions				DPU_1	Comments
		Control Bits			Instructions	Normal VTT	
		Capture	TMU Arm	MCU Trigger		InOut	
1	Three levels_div4					T	
2						T	
3						T	
4						0	
5						T	
6						T	
7						T	
8						1	
9						T	
10						T	
11						T	
12						0	
13						T	
14						T	
15						T	
16						1	
17						T	
18						T	
19						T	
20						0	

- Restrict: Need more store memory. Need to translate the pattern data.

Is it possible to drive the levels with original T0? Yes!

TestConX中国 China

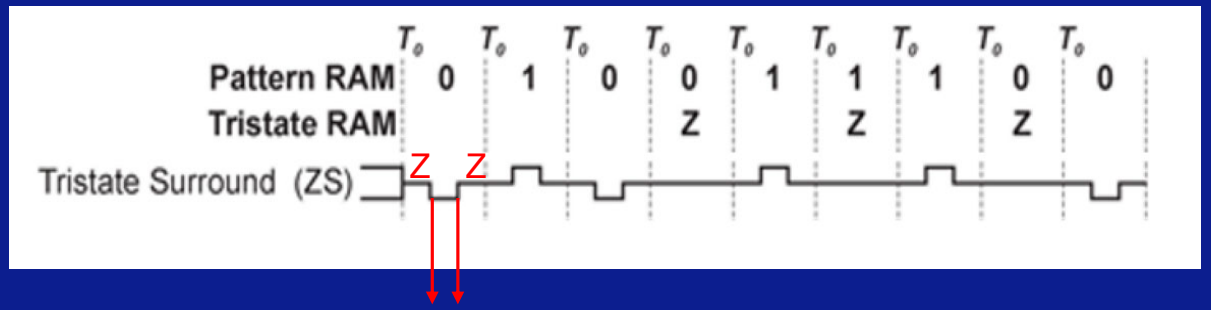
Drive More Than Two Pin Levels With DPU-16

2022

11

Method 2: With Format Tristate Surround(ZS)

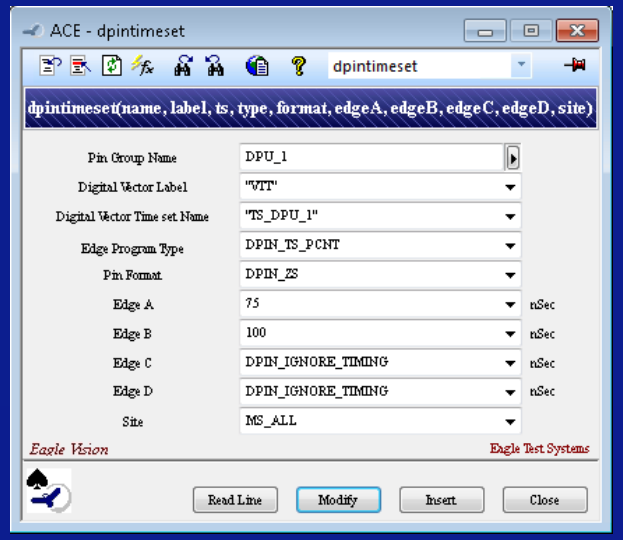
- The format *Tristate Surround* means the level before edge A and after edge B is set to Z(VTT level) .



- In our case, we can set the edge A to 75% of the whole period, edge B as the end of a period.

Method 2: With Format Tristate Surround(ZS)

- No need to split T0, save store memory.
- No need to translate the data, easy to create the pattern data.

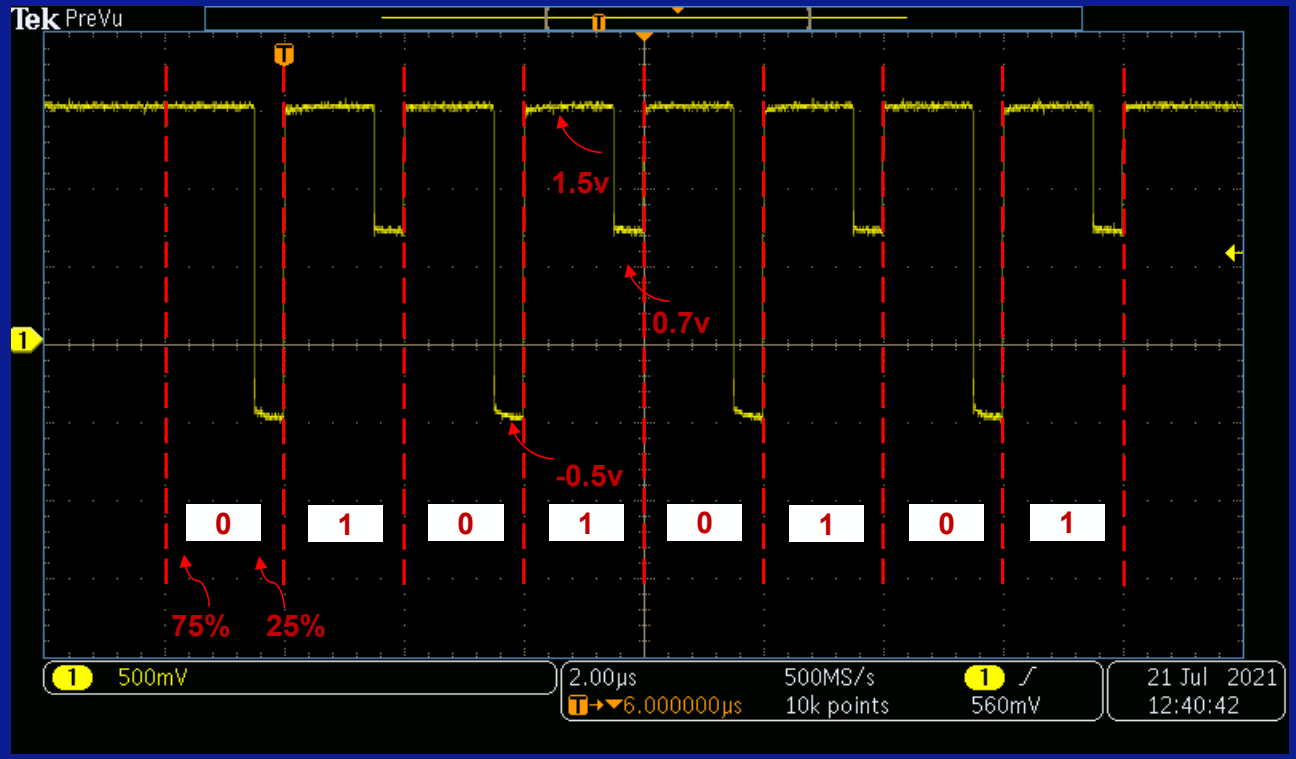


Format and Edge Setting

Step	Label	Pattern Sequencer (PSQ) Control Bits and Instructions				DPU_1	Comments
		Control Bits			Instructions	Normal VTT	
		Capture	TMU Arm	MCU Trigger		InOut	
1	VTT					0	
2						1	
3						0	
4						1	
5						0	
6						1	
7						0	
8					Halt	1	

Pattern Data

Actual waveform



TestConX中国 China

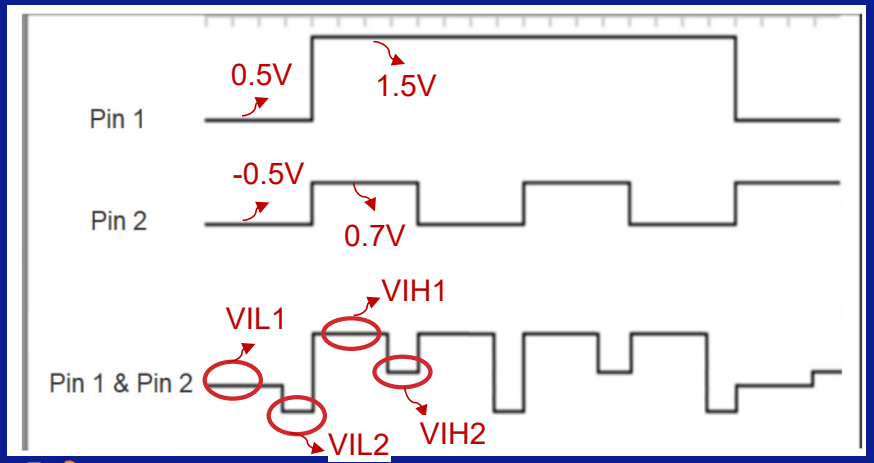
Drive More Than Two Pin Levels With DPU-16

2022

14

Drive More than 3 Levels

- One more complexed case:
  - One device pin combines pin1 and pin2
  - VIL1 and VIH1 on pin1, VIL2 and VIH2 on pin2
  - the combined signal drives four levels in total
  - One DPU channel can't achieve, take into two DPU channels



TestConX中国 China

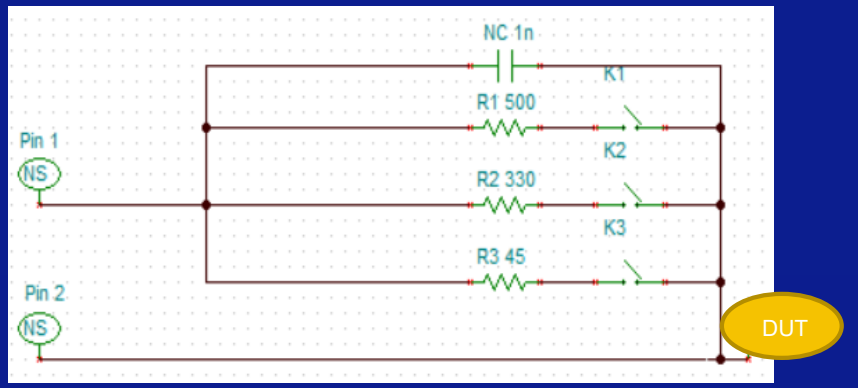
Drive More Than Two Pin Levels With DPU-16

2022

15

Block Diagram

- Pin1 and Pin2 connect R to device pin
- Pin1 drive VIL1, VIH1 while Pin2 drive Hiz
- Pin2 drive VIL2, VIH2 while Pin1 drive Hiz



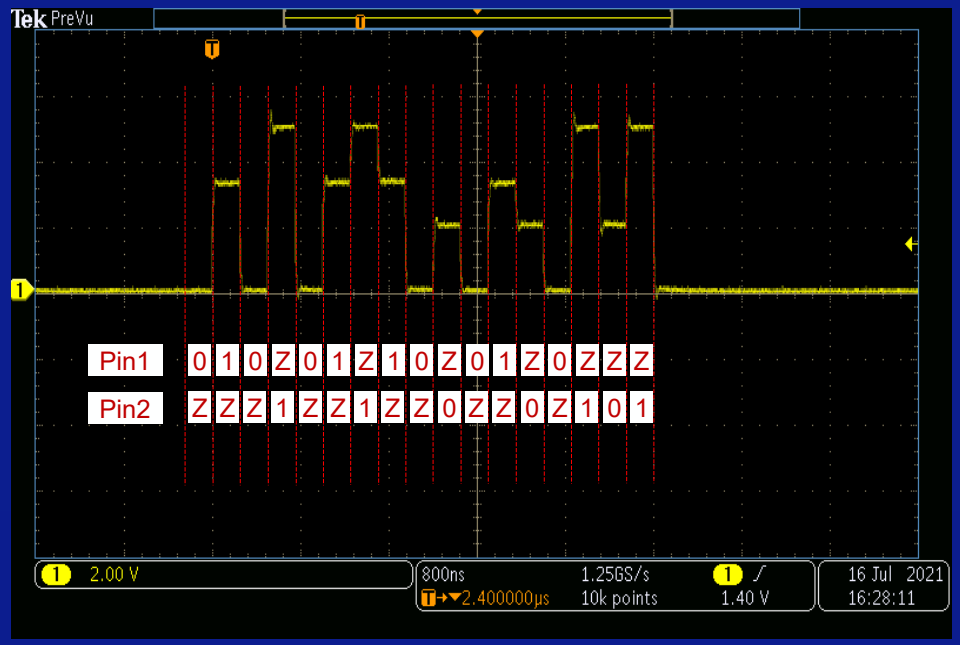
Block Diagram

Pattern and Waveform

- One more complex vector data needed

Step	Label	Pattern Sequencer (PSQ) Control Bits and Instructions				Pin1		Pin2		Comments
		Control Bits			Instructions	Normal		Normal		
		Capture	TMU Arm	MCU Trigger		InOut	Timeset	In	Timeset	
1	FourLevel					0	TS_Pin1	Z	TS_Pin2	V1
2						1	TS_Pin1	Z	TS_Pin2	V2
3						0	TS_Pin1	Z	TS_Pin2	V1
4						Z	TS_Pin1	1	TS_Pin2	V4
5						0	TS_Pin1	Z	TS_Pin2	V1
6						1	TS_Pin1	Z	TS_Pin2	V2
7						Z	TS_Pin1	1	TS_Pin2	V4
8						1	TS_Pin1	Z	TS_Pin2	V2
9						0	TS_Pin1	Z	TS_Pin2	V1
10						Z	TS_Pin1	0	TS_Pin2	V3
11						0	TS_Pin1	Z	TS_Pin2	V1
12						1	TS_Pin1	Z	TS_Pin2	V2
13						Z	TS_Pin1	0	TS_Pin2	V3
14						0	TS_Pin1	Z	TS_Pin2	V1
15						Z	TS_Pin1	1	TS_Pin2	V4
16						Z	TS_Pin1	0	TS_Pin2	V3
17						Z	TS_Pin1	1	TS_Pin2	V4
18					Halt	0	TS_Pin1	0	TS_Pin2	V1

Pattern to Drive Four Levels



Actual Waveform

TestConX中国 China

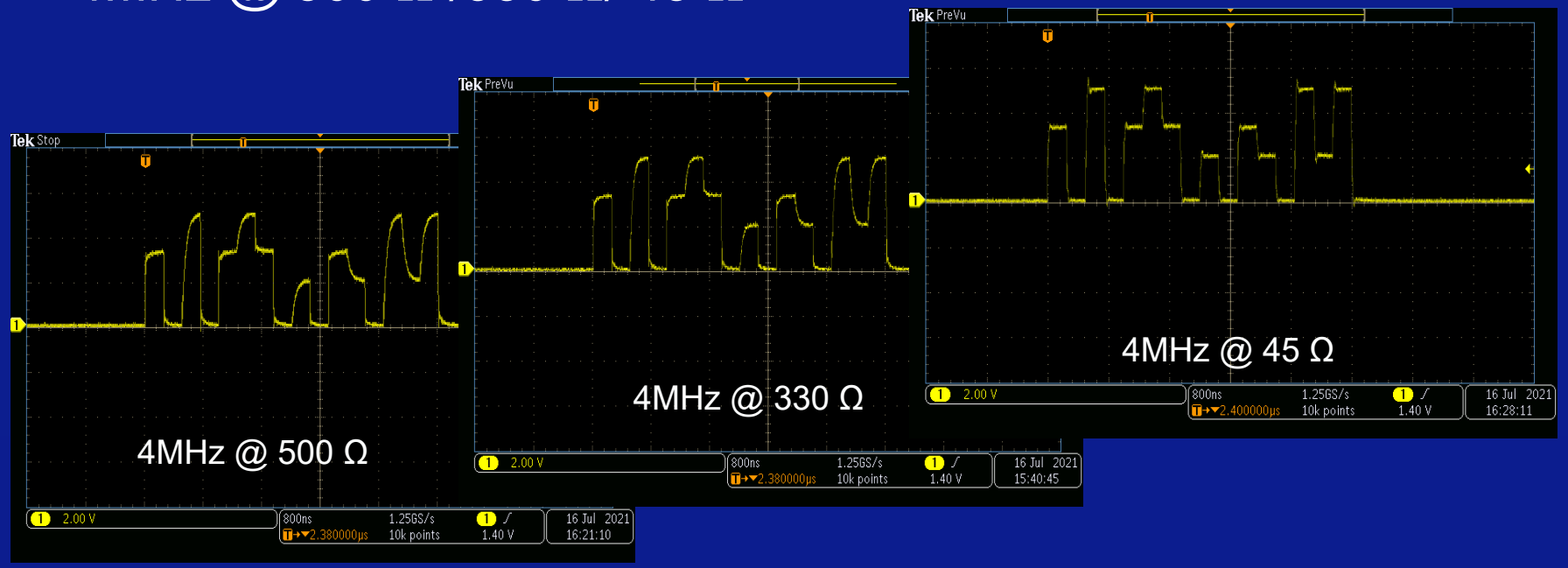
Drive More Than Two Pin Levels With DPU-16

2022

17

Actual Waveform

- 4MHz @ 500 Ω /330 Ω/ 45 Ω



TestConX中国 China

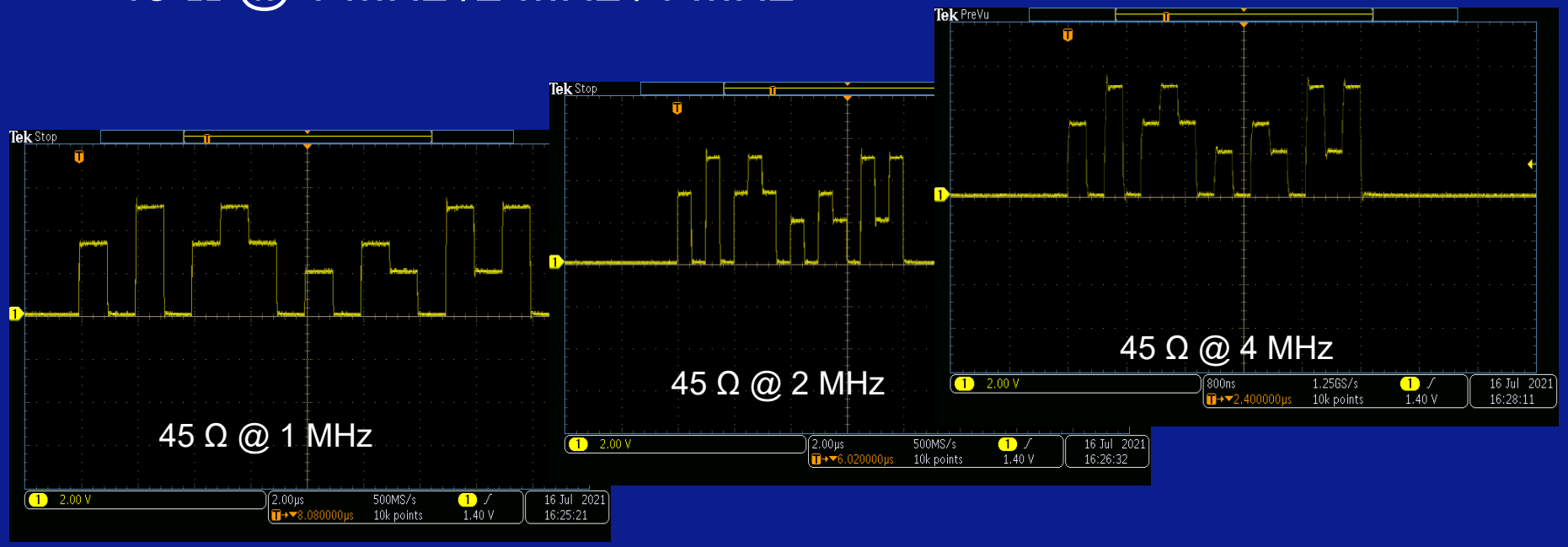
Drive More Than Two Pin Levels With DPU-16

2022

18

Actual Waveform

- 45 Ω @ 1 MHz /2 MHz /4 MHz



TestConX中国 China

Drive More Than Two Pin Levels With DPU-16

2022

19

Something Need to Add

- The higher the resistance is, the slower the signal rises/falls
- Resistor select suitable value to fit impedance matching
- Resistor connects to device as close as possible to reduce spikes when high speed signal

With Thanks to Our Sponsors!

Honored

JCT TECHNOLOGY 金东唐科技

Distinguished

smiths interconnect

TERADYNE

FELDMAN ENGINEERING


金东唐科技
TECHNOLOGY
5G
自动化&智能化的综合方案供应商
Automation & intelligent integrated solution supplier
jdt-precision.com


TestConX中国™
China
is sponsored by
smiths interconnect
Your Global Partner for Innovative
Semiconductor Test Solutions

Enabling the Next Generation of Technology
Through Advanced Test Solutions

TERADYNE.COM

COPYRIGHT NOTICE