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## Virtual Event

## November 1 – 4, 2022
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# Challenging solution design and application for automotive electronic testing on the Advantest V93000 tester

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ADVANTEST

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- Automotive electronic classification and testing challenges
- Floating resources using
- Low and high instrument connection, protection circuit and possible connections
- Systematic utility solution, utility control bit extension and power analysis
- Quality and safety software check tool application

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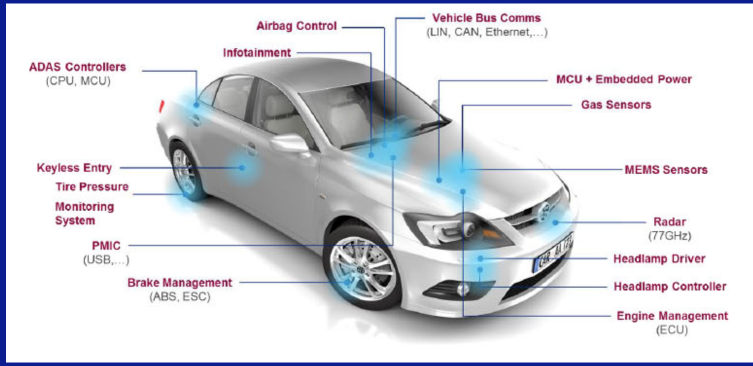
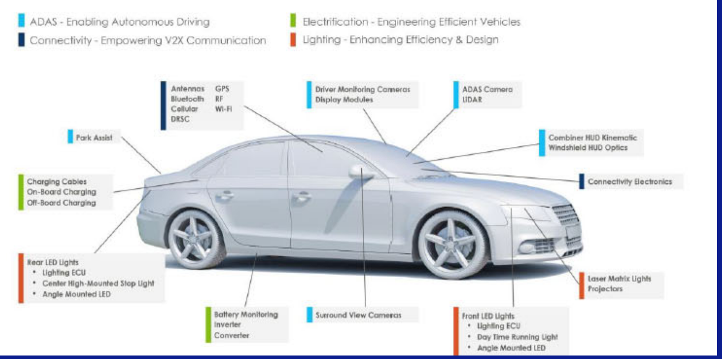
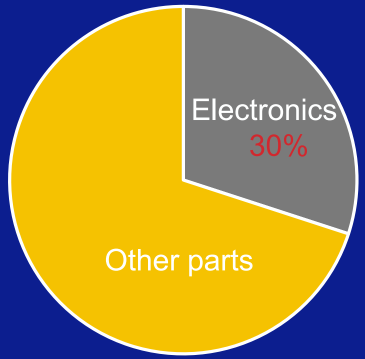
## Automotive Electronic Classification



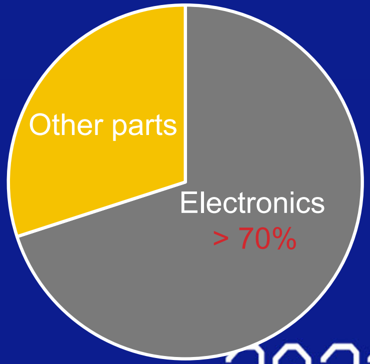

Traditional Automotive




***Traditional Automotive*:**
- Safety and Chassis
  - ABS, ESC, Airbag…
- Power Train
  - Engine Management, injection, transmission…
- Body comfort electronic
  - Door/window/seat controls, LED lighting, wiper…)
- Infotainment
  - Audio, GPS…
- Sensors Control
- Acceleration, gyro, pressure…
- Car Radar

***New Generation Automotive*:**
- Hybrid & Electric Vehicles (EV)
  - Battery monitor, Battery Charger, balancing,
  - Motor Driver/controller
  - Switches (HS/LS, H-Bridges…)
- ADAS system extends
  - Lidar
  - Digital Lighting
  - Camera and Sensors
- V2X (vehicle to everything)
  - 5G, Cellular, Wi-Fi, BT, IoT,…

Electronic Automotive

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## Automotive Electronic Testing Challenges

- Different Level VI cards combination
- Increasing components because of high parallelism
- Lots of resource sharing
- Test costs control
- High voltage and current requirements and high accuracy measurement
- High test program quality

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## V93000 Expansion into Power / Analog / Control

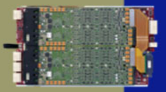
### High Density & Universal Instruments

**PS1600 Universal Pin**
DC.. 1600Mbps
Digital, TMU, VI/PPMU, DPS
**128 channels per card**

**DPS128 HC/HV**
-2.5V…7V, 1A max (-6V…+15V HV)
Precision DC, DPS, VI
**128 channels per card**

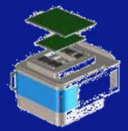
**FVI16**
-60V…+120V, 3A DC / 10A pulsed
VI, DPS, TMU, AWG/DGT
**16 floating channels per card**

**AVI64**
**Universal Analog Pin**
-40..+80V, 100uV accuracy, ±4A pulsed
Precision DC, TMU, AWG/DGT, Digital_IO
**64 channels per card**

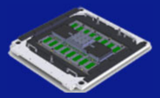



### Scalable Platform

**DUT Scale**
- Same DUT I/F on all TH classes

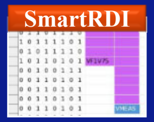


**Direct Probe**
- No need for a probe tower
- High parallel test of WLCSP
- Same Loadboard for wafer/final test



**Power MUX**
- Integrated Power MUX module
- 100V, 1A/5A continuos/pulsed
- **12 x 1:4 Kelvin MUX per module**

**High-Throughput Pattern Based Testing**

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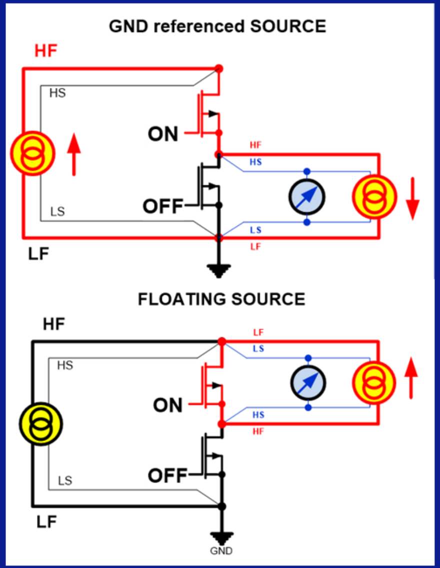
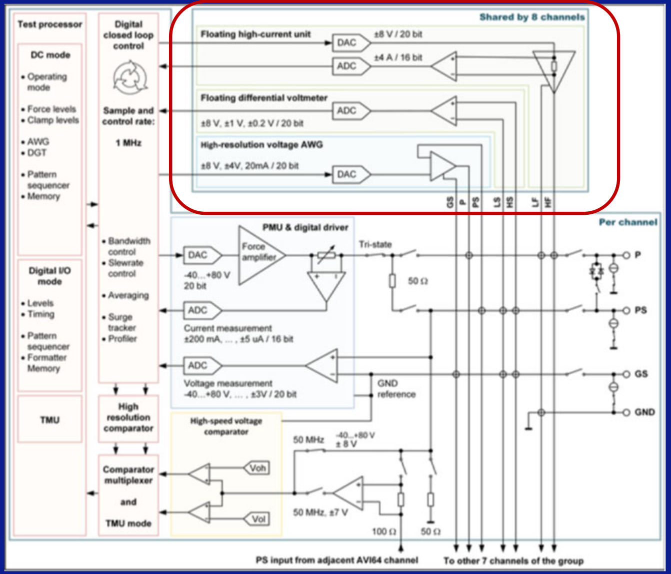
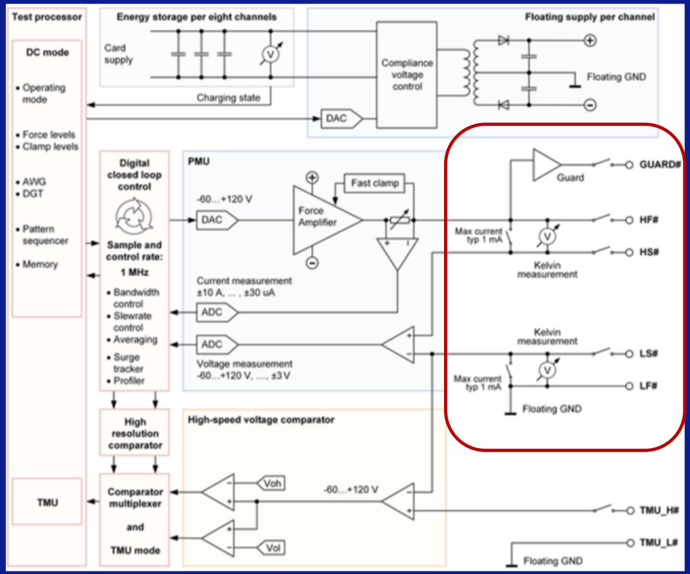
# Concept of Floating and Resources

- For 93K tester, there are two floating resources, AVI64 and FVI16. AVI64 floating resource is shared by one group/8 channels. FVI16 has floating resource per channel.




AVI64 Block diagram




FVI16 Block diagram

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## Floating Resources Using(AVI64 DiffVM)

| Floating differential voltmeter / digitizer | |
|---|---|
| Voltage ranges | ±200 mV, ±1 V, ±8 V |
| Common mode range[1)] | -40 V ... +80 V |
| Input current (maximum) | ± (1 nA + 1 nA / V * $\lvert V_{act} \rvert$)[2)] |
| Input capacitance (typical) | 530 pF (differential), 750 pF (single ended to GND) |

| Voltage measurement | Range | Resolution | Accuracy[3)] |
|---|---|---|---|
| | ±200 mV | 0.4 µV | ± (10 µV + 0.003 % of relative reading)[4)5)] |
| | | | ± (60 µV + 0.003 % of reading)[4)] |
| | | | ± (200 µV + 0.05 % of reading) |
| | ±1 V | 2 µV | ± (15 µV + 0.003 % of relative reading)[4)5)] |
| | | | ± (100 µV + 0.003 % of reading)[4)] |
| | | | ± (300 µV + 0.01 % of reading) |
| | ±8 V | 20 µV | ± (50 µV + 0.003 % of relative reading)[4)5)] |
| | | | ± (300 µV + 0.003 % of reading)[4)] |
| | | | ± (1.0 mV + 0.01 % of reading) |

| Floating differential digitizer | ± 200 mV range | ± 1 V range | ± 8 V range |
|---|---|---|---|
| Resolution | 20 bit (0.4 µV) | 20 bit (2 µV) | 20 bit (20 µV) |
| DC Accuracy[6)] | ±(0.2 mV + 500 ppm of reading) | ±(0.3 mV + 100 ppm of reading) | ±(1 mV + 100 ppm of reading) |
| INL (typical) | ± 3 µV (± 7 ppm FSR) | ± 6 µV (± 3 ppm FSR) | ± 40 µV (± 3 ppm FSR) |
| DNL (typical) | ± 1 ppm FSR | | |
| Sampling rate | 0 ... 1 Msps (million samples per second) | | |


**AVI64Ch1 and AVI64Ch2 should be placed in one group of 8 channels when do the test solution design.**

```
rdi.dc().pin("PinS").vForce(7.8 V).vForceRange(10 V).vMeasRange(8 V).refPin("PinO")
        .pin("PinO").iForce(0 mA).iForceRange(200 mA).vClamp(-10 V,10 V).vForceRange(10 V).execute();
RDI_BEGIN((TA::USER_RUN_MODE) rdiRunMode);
    rdi.dc().pin("PinO").iForce(-150 mA).execute();
    rdi.dc("id_v_dropout").pin("PinS").vMeas().average(128).measWait(2 ms).execute();
RDI_END();
```

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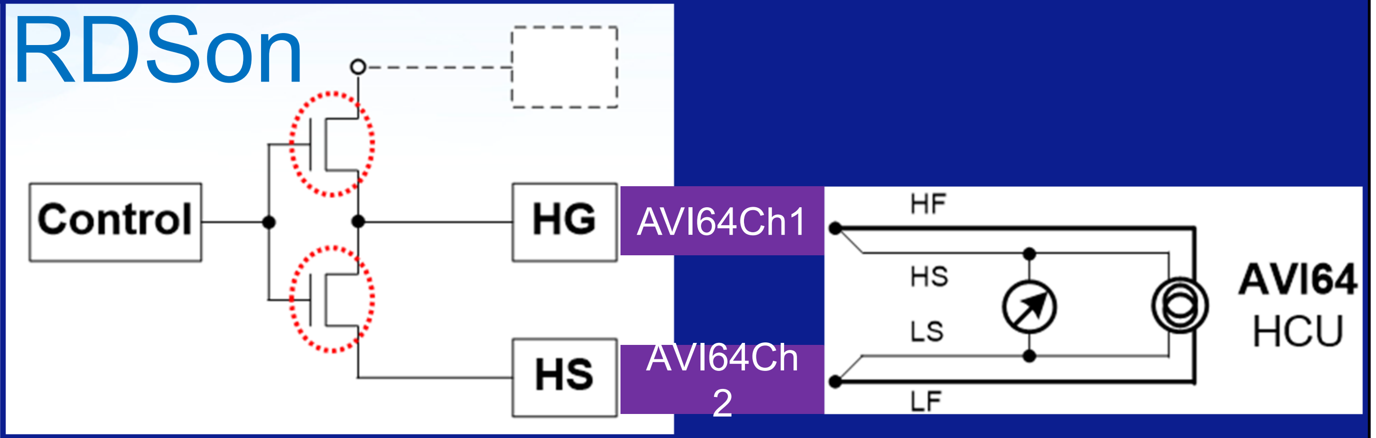
## Floating Resources Using(AVI64 HCU)

| Floating high-current unit (pulsed operation) | |
|---|---|
| Voltage range | ±8 V |
| Voltage measure resolution | 20 µV |
| Voltage measure accuracy | ± (1 mV + 0.01 % of reading) [1] |
| Voltage force resolution | 300 µV |
| Voltage force accuracy | ± (3.5 mV + 0.03 % of setting) |
| Voltage clamp accuracy | ± (10 mV + 0.1 % of setting) |
| Floating range | -30 V ... +80 V [2] |
| Current range | ±4 A (pulsed operation) |
| Current measure resolution | 140 µA |
| Current measure accuracy | ± (2 mA + 0.1 % of reading) [1)3)] |
| Current force resolution | 200 µA |
| Current force accuracy | ± (2 mA + 0.1 % of setting) [3] |
| Current clamp accuracy | ± (4 mA + 0.5 % of setting) |
| Minimum pulse width | 100 µs |
| Maximum pulse width | See diagrams below |




**AVI64Ch1 and AVI64Ch2 should be placed in one group of 8 channels when do the test solution design.**

```
rdi.dc().pin("HG").mode(TA::HiCurrent).iForce(-1 mA).iForceRange(4 A).vClamp(-0.5 V,0.5 V).preCharge(TA::SAFE_CON).refPin("HS").execute();
rdi.dc().pin("HS").connectState(TA::HIZ).vMeasRange(8 V).execute();

RDI_BEGIN((TA::USER_RUN_MODE) rdiRunMode);

rdi.dc("v_rdson").pin("HG").iPulse(1.5 A,-1 mA,250 us).vMeas().average(16).measWait(200 us).execute();

RDI_END();

rdi.dc().pin("HG,HS").disconnect().execute();
```

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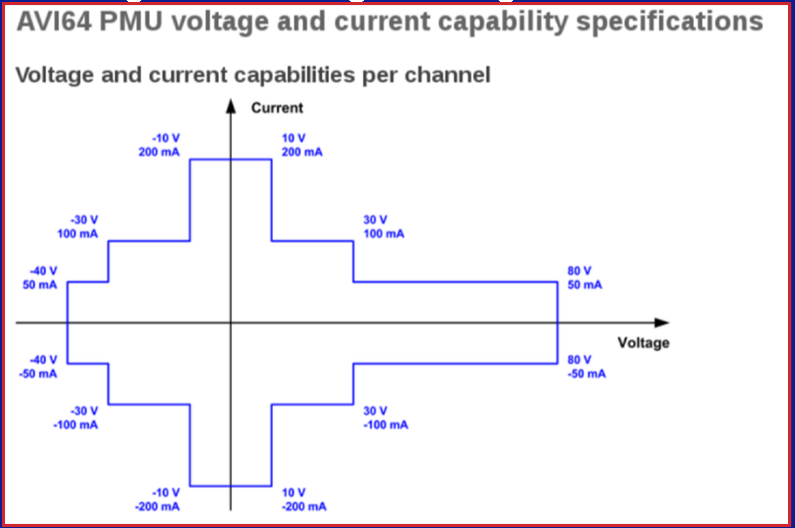
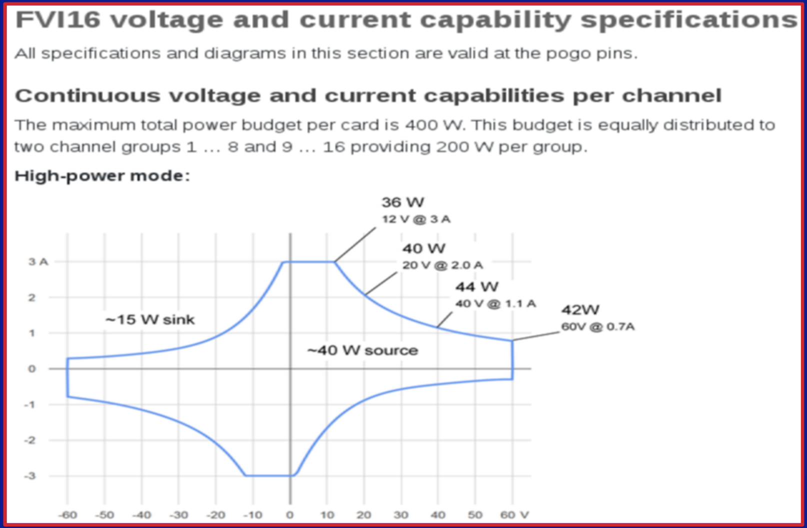
# Floating Resources Using(FVI16)

- **Floating FVI16 Innovative Using**
  - ➢ Background using floating FVI16

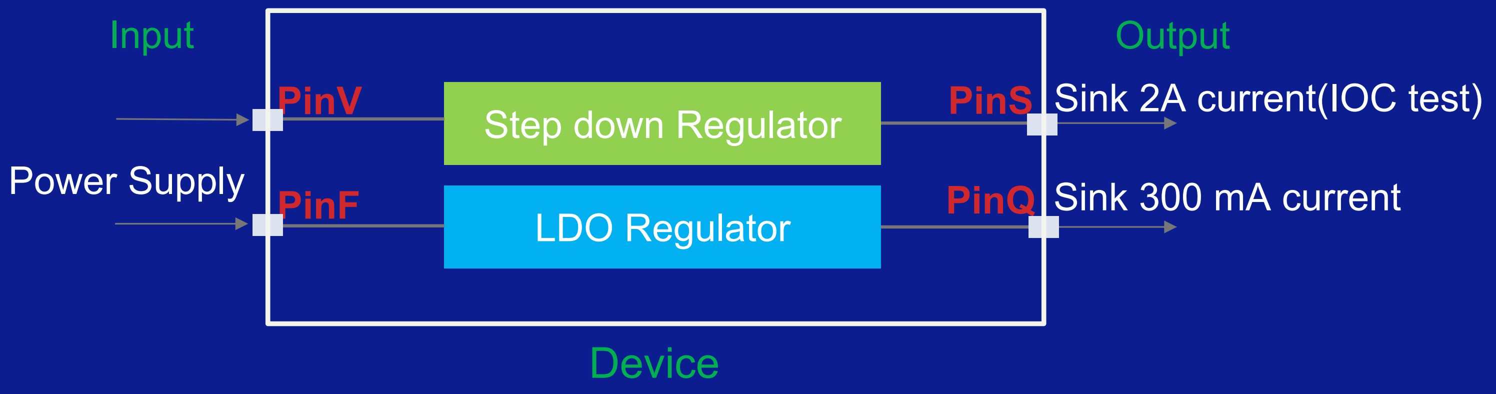



Considering current value is more than 200 mA, we can only use FVI16 channel for PinV, PinS, PinF and PinQ. From the test plan, we should assign 2 FVI16 channels at least on the condition that step down regulator share resources with LDO regulator.

# Floating Resources Using(FVI16)

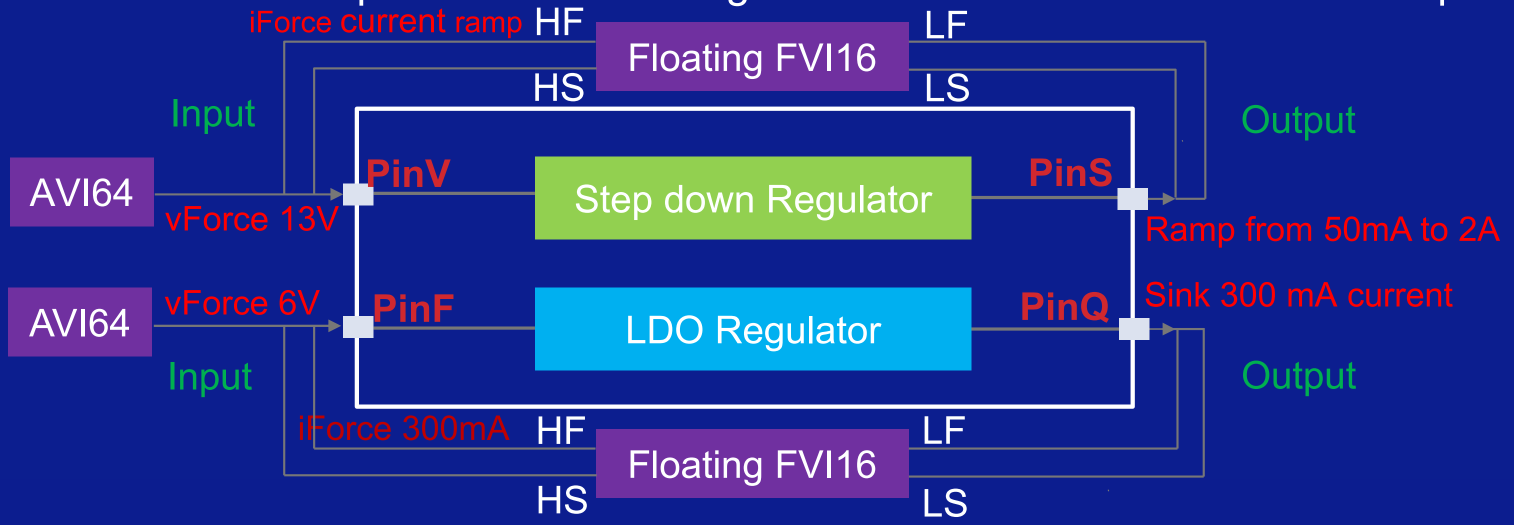
- **Floating FVI16 Innovative Using**
  - ➢ Background using floating FVI16




Configuration customer provided is 2* FVI16 + 4*AVI64 + 4*PS1600 cards for 32 sites, which means we can only assign one FVI16 channel per site.

# Floating Resources Using

- **Floating FVI16 Innovative Using**
  - Solutions---Also Step down and LDO regulator can share one FVI16 channel per site.

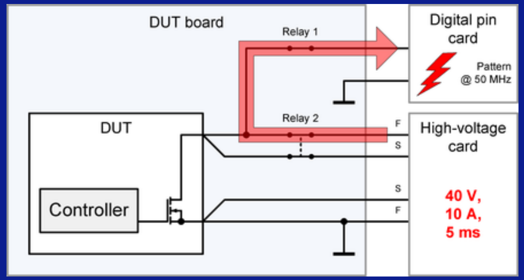



```
anaWaveform IBckOCRamp("IBckOCRamp");
IBckOCRamp.definition(TM::RAMP).direction(TM::POS).samples(200).max(2000 mA).min(0 mA); //10mA steps, ramp 0mA to 2A
rdi.dc().pin("PinV_FVI").iForce(0 mA).vForceRange(10 V).preCharge(TA::SAFE_CON).vClamp(-1 V, 10 V).iForceRange(2000 mA).execute();
rdi.dc().pin("PinV_AVI").vForce(13 V).vForceRange(30 V).preCharge(TA::SAFE_CON).iClamp(-10 mA, 100 mA).iForceRange(100 mA).execute();
RDI_BEGIN();
  rdi.dc().pin("PinV_FVI") .iForce(0.0 mA).iForceRange(2000 mA).vClamp(-1 V, 10 V).execute();
  rdi.dc().pin("PinV_FVI").iForce().waveform(IBckOCRamp).FS(100 KHz).execute();
RDI_END();
```

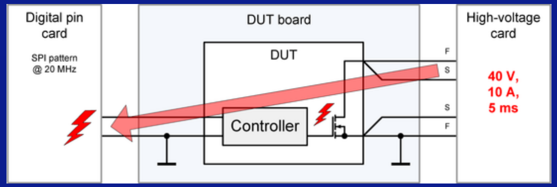
# Connection and Damaged Situations

- ATE low-voltage test head cards can be damaged by high voltage card.
- This will be caused by two situations.

- Wrong relay closed connections
  High voltage from a HV card can be connected to a LV card by mistake when debugging, relay overlapped switching or sticking

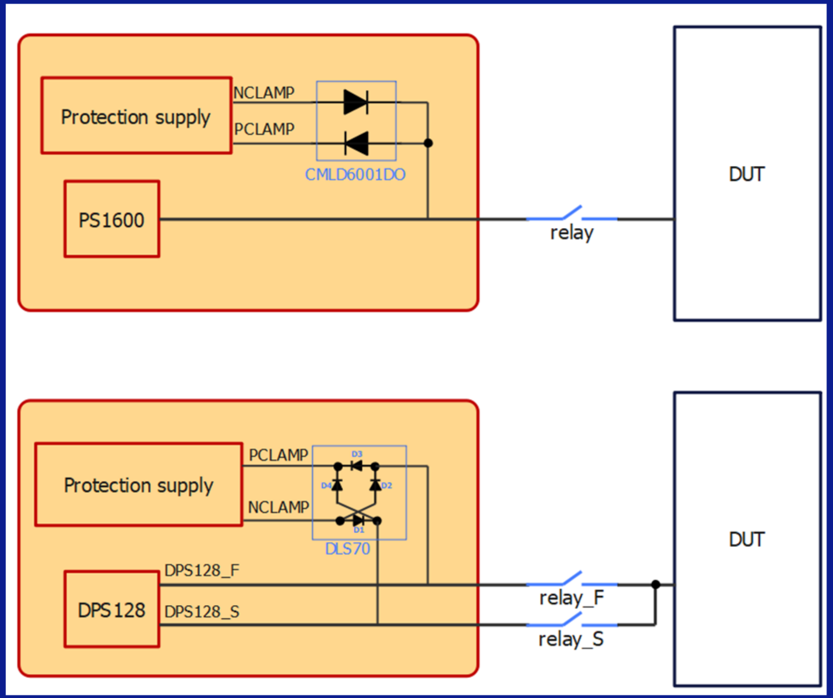



- Defective DUTs
  High voltage from a HV card can be short connected to the low voltage pin connected to LV card even if the DUT already has passed low voltage isolation tests



# Typical Protection Circuit Introduction

- Digital card or other LV cards protection diagram
- **Protection circuity:**
- Protection supply
  - DC supply
  - Positive and negative regulators
- Clamp diodes
  - Generate the positive and negative clamp voltage to the protect lines
- Protection location
  - Place the protection circuit to the tester-end not the DUT-end



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## Possible Connections

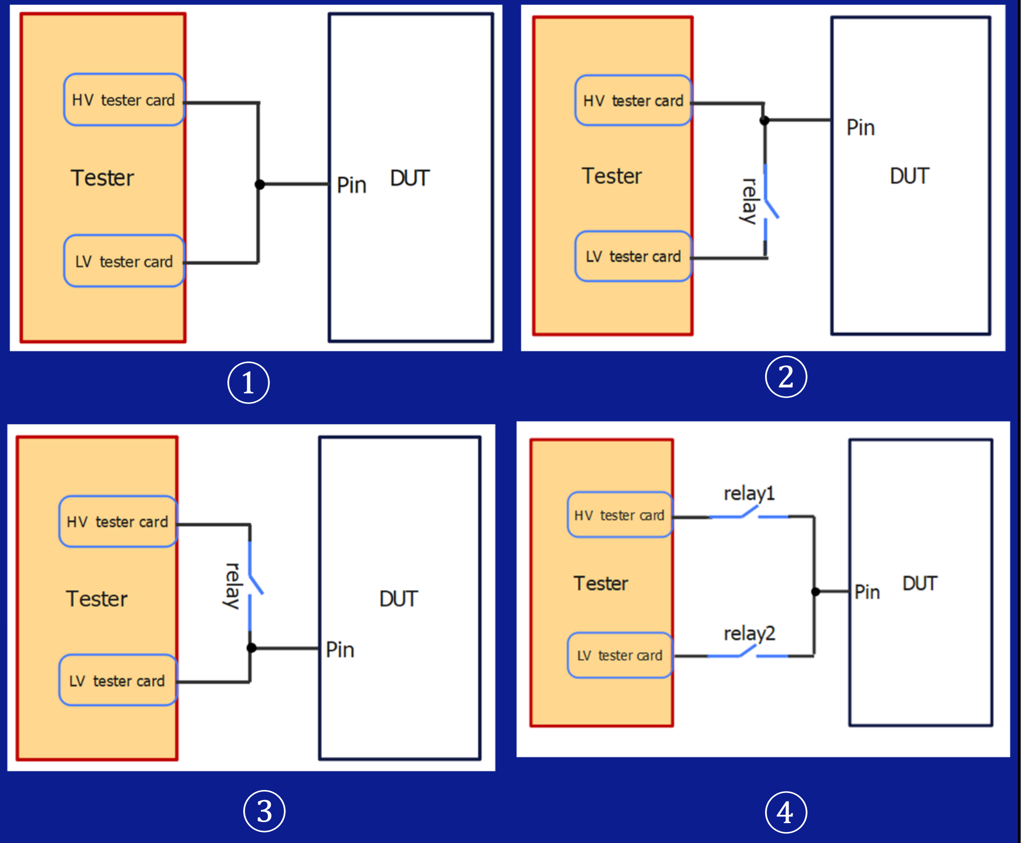
- **4 situations ：**

❑ HV and LV card connect to pin directly
- HV card forced voltage may be clamped to LV card protection voltage
- Test solution failed
- HV and LV resources can not be shared

❑ Only LV card route to pin with relay
- HV card can force the voltage exceed LV card protection voltage when relay is off.
- HV resources may not be shared.

❑ Only HV card route to pin with relay
- When relay is on, the status like the situation 1
- LV resources may not be shared

❑ HV and LV card connect to pin with relay
- HV and LV card can force the required voltage flexibly
- HV and LV resources can be shared




Default: LV card with protection circuit

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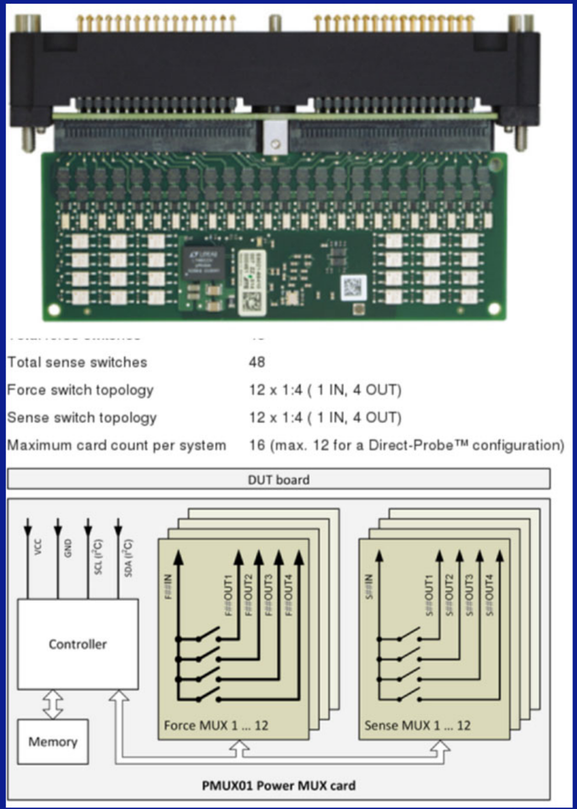
# PMUX

Power mux is a solid-state multiplexer card featuring twelve 1:4 Kelvin multiplexers.

## Key characteristics:

- Multiplexer structure: 1:4 Kelvin (Force + sense)
- Multiplexers per card: 12 high-current (Force) + 12 low-current (Sense)
- Maximum card count per system: 16
- Maximum number of multiplexers per system: 2 * 12 * 16 = 384
  1:4 multiplexers or 1536 switches
- Voltage compliance: 120 V
- Current compliance of high-current multiplexers: 1A DC,5A pulsed,
  (maximum 10 ms,10 % duty cycle)
- Current compliance of low-current multiplexers: 100 mA continuous
- Leakage current: 20nA typical@80 V and ambient temperature



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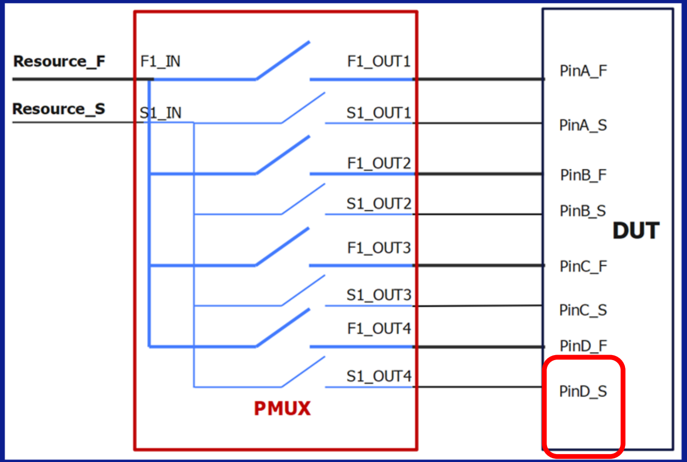
## PMUX

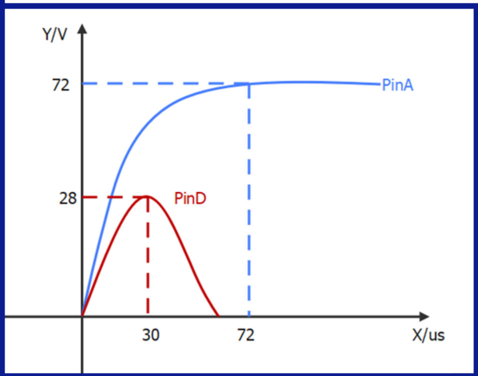
| Pin | Min voltage | Max voltage |
|---|---|---|
| PinA | -10V | 72V |
| PinB | -10V | 72V |
| PinC | -10V | 72V |
| PinD | -2V | 15V |
| PinE | -10V | 72V |




PMUX switches can help achieve the tester resource sharing. When resource card forces 72V to PinA, Spike voltage will appear on the PinD no matter the OUT4 switch is on or off.

Suggestion:

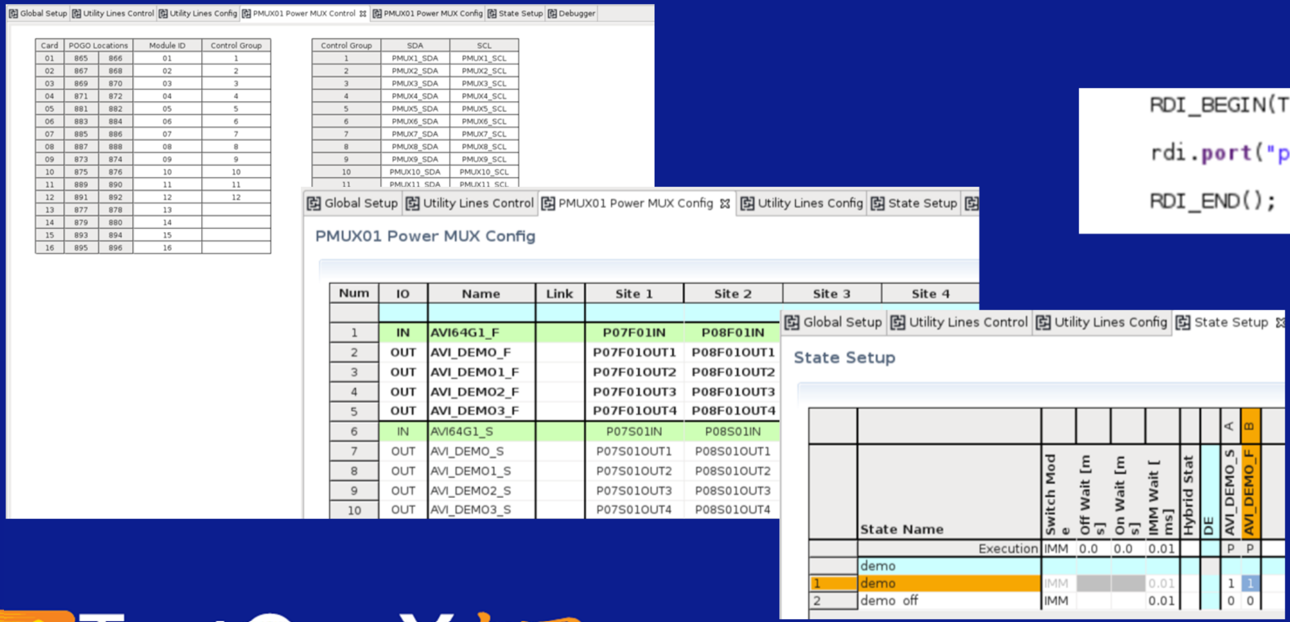
- Arrange the similar pins or same level voltage pins to one multiplexer
- Add the relay isolated with the high voltage pin
- Add the capacitor to make the voltage rise slowly within no other effects to test solution



# PMUX

The Routing Tools feature native multisite handling, user friendly table configuration editors and a unified programming interface for controlling utility lines and MUX card switches.

- Routing Tools editors
- The class rdi.route() of SmartRDI




```
RDI_BEGIN(TA::BURST);

rdi.port("pPMUX").route().applyState("demo").execute();

RDI_END();
```

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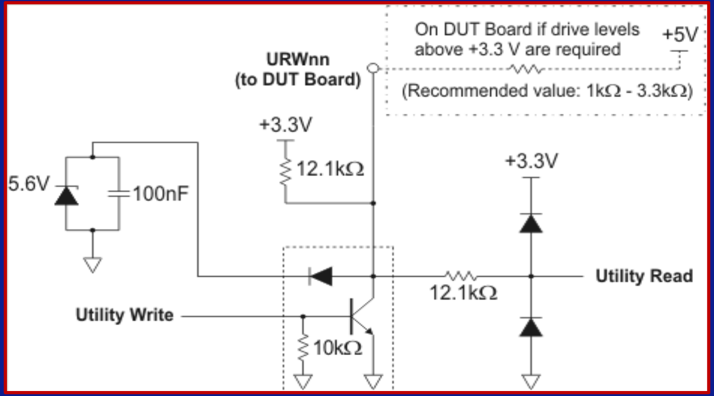
## 93K Utility Resources

For ATE, we use load board or prober card for test. Usually, there are many relays on load board or prober card. How to control relay by 93K utility is a system design.

➢ 93K Utility Resources and Spec




**Utility lines**

Utility lines 129-256 are optional and supported from SmarTest release 7.2.0 on.

| Characteristics | A-test head | | Compact test head | | Small test head | | Large test head |
|---|---|---|---|---|---|---|---|
| | small DUT IF | DUT Scale IF | small DUT IF | DUT Scale IF | small DUT IF | DUT Scale IF | |
| Number of card cages | 1 | 1 | 2 | 2 | 4 | 4 | 8 |
| Number of utility lines | 64 | 256 | 64 | 256 | 64 | 256 | 256 |
| Output type | Open collector | | | | | | |
| Maximum current | 60 mA (each) maximum of 800 mA per utility pogo block (internal utility supply)<br>maximum of 2 A per utility pogo block (external utility supply) | | | | | | |
| Output voltage | | | | | | | |
| Open collector output open, no load applied | The maximum voltage and the impedance depend on the configuration of the system:<br>• An internal pull up resistor is available per utility line.<br>• The pull-up resistor is connected to the internal supply voltage of the utility line.<br>• The resulting output voltage of the open output depends on the configuration of the system and will be in the range from 3.3 V to 5.0 V.<br>We recommend using external pull up resistors for applications with higher requirements.<br>Refer to DUT Board Design Changes for Future Utility Line Compatibility for more information. | | | | | | |
| Open collector output closed | Typically ~0.7 V at low collector currents (<10 mA) or<br>up to 1.0 V at higher collector currents | | | | | | |
| Input type | TTL | | | | | | |
| Input voltage range | 0.0 V ... 5.0 V | | | | | | |
| Input impedance | > 10 kΩ | | | | | | |

- Number of Utility Lines : 128/256
- Sequencer Controlled
- Utility line circuit with internal pull-up resistor to 3.3V

- 60mA is not enough to drive a relay coil
- Not enough utility lines (>256).
- Voltage is too low for a MOSFET gate voltage

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# Utility Bit Extension

Max Number of Utility Lines is 256. Considering the multi-site and high parallelism, we had to extend utility bit to meet challengeable requirements in general. Thus, we need to design systematic relay control by utility solution.

The PCA9698 provides 40-bit parallel input/output (I/O) port expansion for I2C-bus applications organized in 5 banks of 8 I/Os. At 5 V supply voltage, the outputs are capable of sourcing 10 mA and sinking 25 mA with a total package load of 1 A to allow direct driving of 40 LEDs.

- ❑ 1 MHz Fast-mode Plus I2C-bus serial interface
- ❑ Compliant with I2C-bus Fast-mode (400 kHz) and Standard-mode (100 kHz)
- ❑ 2.3 V to 5.5 V operation with 5.5 V tolerant I/Os
- ❑ 40 configurable I/O pins that default to inputs at power-up

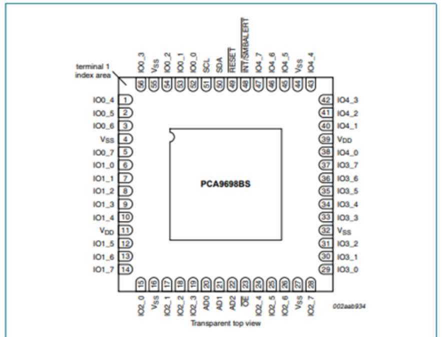


Fig 4. Pin configuration for HVQFN56

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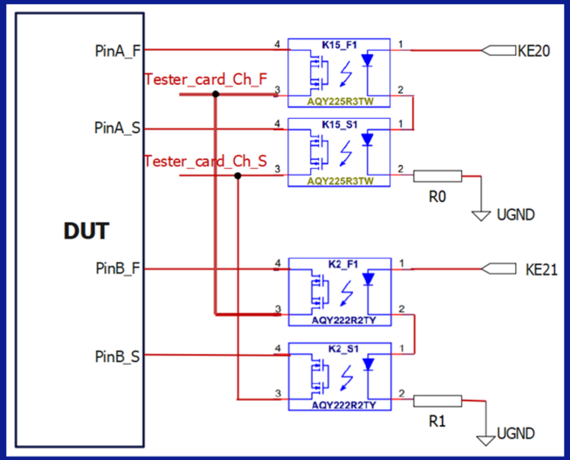
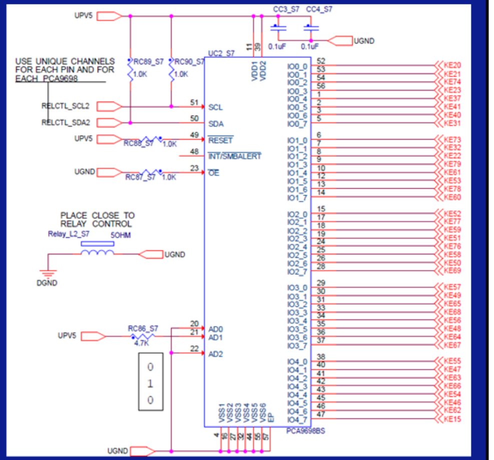
## Utility Bit Extension

Requirement and hardware connection:

- ❑KE20 and KE21 from PCA9698 IO Pins
- ❑KE20 can make the PinA connect to tester channel
- ❑KE21 can make the PinB connect to tester channel
- ❑40 configurable I/O pins
- ❑Configurable address to multiple devices using



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## Utility Bit Extension

### Software control:

- ❑Setup the RelayState file and utility purpose
- ❑Read and analysis the RelayState file
- ❑Subroutine I2C write to control the device
- ❑Using the RDI class smartVec to generate the I2C pattern flexibly
- ❑Using the burst label to decrease the execution time

i2c_RelayStates_demo.csv

| | Relay Channel | 200 | 201 |
|---|---|---|---|
| | | | |
| 1 | I2C Bit | 1_KE20 | 1_KE21 |
| 2 | Relay Number | K15 | K2 |
| 3 | Utility Purpose | PinA connect | PinB connect |
| 4 | all_off | 0 | 0 |
| 5 | i2C_PinA_Connect_demo | 1 | 0 |
| 6 | i2C_PinB_Connect_demo | 0 | 1 |

```
// Read relay settings
readRelayTable("i2c_RelayStates_demo");
void readRelayTable(const string& csvFile) {

    if(relayTableLoaded == false) {

        TestTable* tt = TestTable::createInstance();
        string file = "../testtable/" + csvFile + ".csv";

        if(!tt->readCsvFile(file.c_str())) {
          tminfo3 << "Cannot read " << file << endl;
          return;
        }
```

```
bool rdiWriteRelay(const string& utilPurpose)
{

    map <string, map <int, int> >::iterator it=relayTable.find(utilPurpose);

    if(it == relayTable.end()) {
        tmerr << "Utility_purpose " << utilPurpose << " not found." << endl;
        return false;
    }

    FW_TASK("RLYC AC,OFF,(I2C_SCL,I2C_SDA)");

    // i2c padding solution
        rdi.port("pSCL").func().label("i2c_state_init").execute();

        for(int i = 0; i < 5; i++) {

            adr1 = 0x22;
            reg1 = 0x08 + i;
            I2C_WRITE("pSDA", "I2C_SDA", adr1, reg1, relayTable[it->first][i]);
        }


    return true;
}
```

```
void I2C_WRITE (      const string & PORT,
                      const string & PIN,
                      const int & adr,
                      int reg,
                      int data)
{
    rdi.smartVec().burstLabel("REG_" + rdi.itos_hex(reg)+"__DATA_"+rdi.itos_hex(data)).begin();
    I2C_CALL_SLAVE("w", PORT, PIN, adr);
    I2C_REG(PORT, PIN, reg, rdi.itos_hex(reg));
    I2C_DATA(PORT, PIN, data, rdi.itos_hex(data));
    _Stop(PORT, PIN);
    rdi.smartVec().burstLabel().end();
}
```

# Systematic Relay Solution

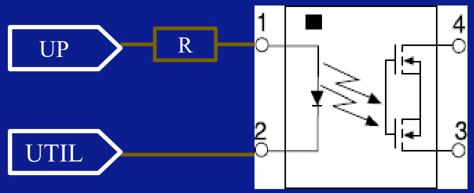
Test Solution :

We used relay photomos G3VM-61GR2 as driver to improve the current capacity to 1.3A. Photomos G3VM-61GR2 Spec. as below.

| | Item | Symbol | Minimum | Typical | Maximum | Unit | Measurement conditions |
|---|---|---|---|---|---|---|---|
| Input | LED forward voltage | $V_F$ | 1.0 | 1.15 | 1.3 | V | $I_F$ = 10 mA |
| | Reverse current | $I_R$ | - | - | 10 | µA | $V_R$ = 5 V |
| | Capacity between terminals | $C_T$ | - | 15 | - | pF | V = 0, f = 1 MHz |
| | Trigger LED forward current | $I_{FT}$ | - | 1.0 | 3 | mA | Io = 100 mA |

| Item | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Load voltage (AC peak/DC) | $V_{DD}$ | - | - | 48 | V |
| Operating LED forward current | $I_F$ | 5 | 10 | 25 | mA |
| Continuous load current (AC peak/DC) | Io | - | - | 1.3 | A |
| Ambient operating temperature | Ta | -20 | - | 65 | °C |

| | Item | Symbol | Rating | Unit | Measurement conditions |
|---|---|---|---|---|---|
| Input | LED forward current | $I_F$ | 30 | mA | |
| | LED forward current reduction rate | $\Delta I_F/°C$ | –0.3 | mA/°C | Ta ≥ 25°C |
| | LED reverse voltage | $V_R$ | 5 | V | |
| | Connection temperature | $T_J$ | 125 | °C | |
| Output | Load voltage (AC peak/DC) | $V_{OFF}$ | 60 | V | |
| | Continuous load current (AC peak/DC) | Io | 1.7 | A | |
| | ON current reduction rate | $\Delta Io/°C$ | –17 | mA/°C | Ta ≥ 25°C |
| | Pulse ON current | Iop | 5 | A | t = 100 ms, Duty = 1/10 |
| | Connection temperature | $T_J$ | 125 | °C | |




For example,

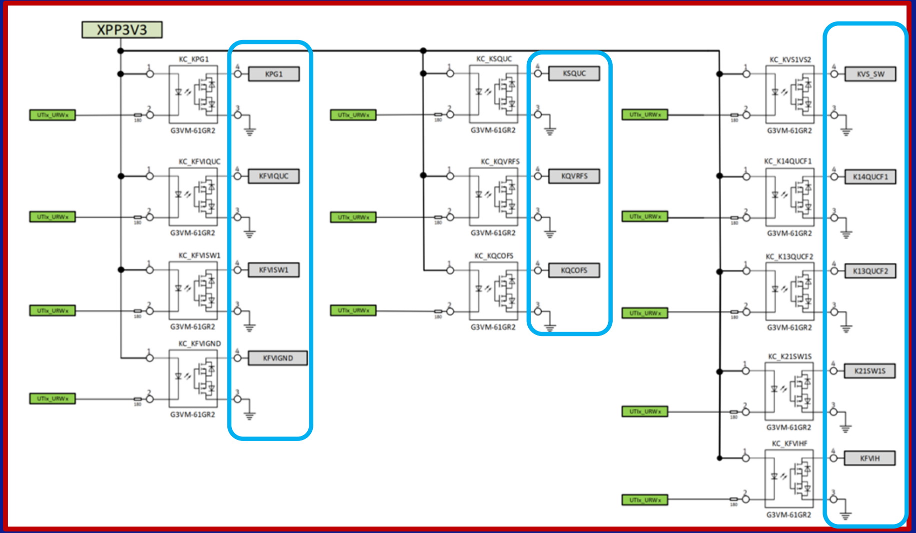
UP is UP5V, R = (UP5V – $V_F$) / $I_F$ = (4.85 – 1.15) V/ 10mA = 370 Ohm

UP is XPP3V3, R = (3.3 – $V_F$) / $I_F$ = (3.3 – 1.15) V / 10mA = 215 Ohm

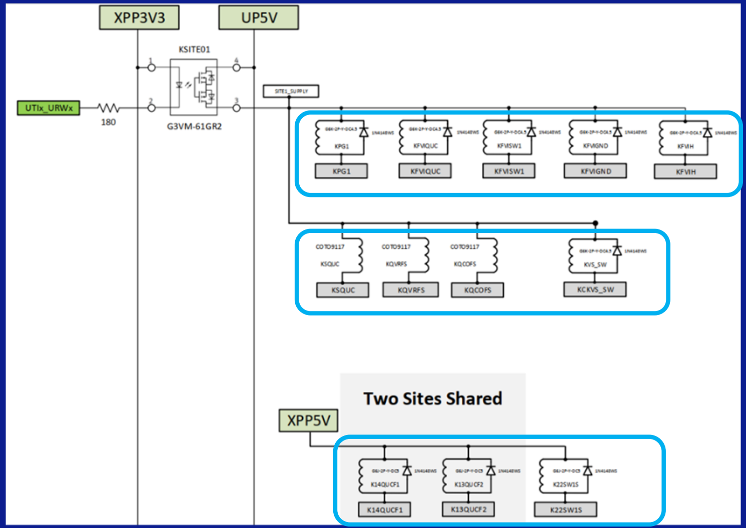
# TestConX China 2022

## Systematic Relay Solution

Relay driver




32 sites control logic

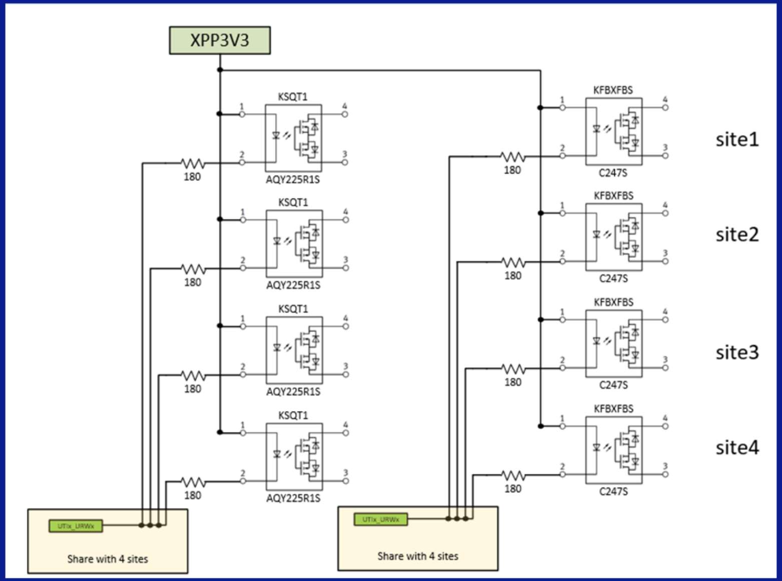


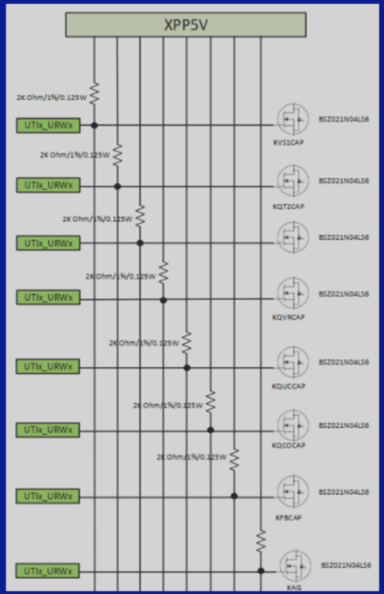

Mechanical Relay Control For All Sites(32 sites)
Utility for Mechanical Relay Control = 12

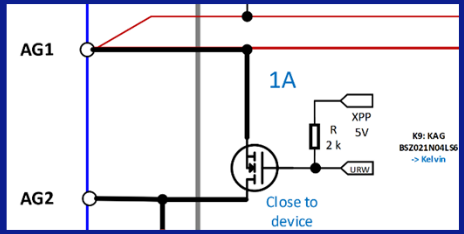
# TestConX China 2022

## Systematic Relay Solution

- For AQY225R1S and C247S, we shared one utility bit for 4 sites
- For BSZ021N04LS6, we use one utility bit for 32 sites. Totally need 8 utility bits.



# Systematic Relay Solution

Overall, for 32 sites, we need 82 utility bits totally.

| Relay Type | SPST | MOSFET | DPDT | DPDT | Photo Mos | Photo Mos | site control/MOS | master relay/MOS | |
|---|---|---|---|---|---|---|---|---|---|
| Model | Coto 9117 | BSZ021N04LS6 | G6K-2P-Y-DC4.5 | G6J-2P-Y-DC5.0 | AQY225R1S | C247S | G3VM-61GR2 | | |
| 5V Domain | | | | | | | | | |
| IF | 12.5 mA | Igs = 0 ? | 23.2 | 28.9 | 3 mA | 3 mA | 10mA | | |
| Specs | 0.5A/0.12Ohm | 147A/2.1mOhm | 2A/100Ohm | 1A / 100 mOhm | 0.35A/1.2Ohm | 1A/0.5 Ohm | 1.7A/.Ohm | | |
| Size(mm) | 9.77x6.85x3.81 | 3.2x3.2x0.9 | 10x6.5x5 | 10.6x5.7x9 | | | 4.4x3.9x2.1 | | |
| Single site | KSQUC | KVS1CAP | KPG1 | KSW1S | KSQT1 (1 util to control 8 sites) | KVST (1 util to control 8 sites) | | | |
| | KQVRFS | KQVRCAP | KFVIQUC | KQUCF1 | KSQT2 (1 util to control 8 sites) | KFBXFBS (1 util to control 8 sites) | | | |
| | KQCOFS | KQUCCAP | KFVISW1 | KQUCF2 | | | | | |
| | | KQCOCAP | KFVIGND | | | | | | |
| | | KFBCAP | KFVI | | | | | | |
| | | KAG | KVS_SW | | | | | | |
| Used Relays | 3 | 6 | 6 | 2 (1 per site, 2 relays shared) | 2 | 2 | | | |
| | | | | | | | KSITE1 | KCKPG1 | |
| | | | | | | | KSITE2 | KCKFVIQUC | |
| | | | | | | | KSITE3 | KCKFVISW1 | |
| | | | | | | | KSITE4 | KCKFVIGND | |
| | | | | | | | KSITE5 | KCKVS_SW | |
| | | | | | | | KSITE6 | KCKQUCF1 | |
| | | | | | | | KSITE7 | KCKQUCF2 | |
| | | | | | | | KSITE8 | KCKSW1S | |
| | | | | | | | KSITE9 | KCKFVIH | |
| | | | | | | | KSITE10 | KCKSQUC | |
| | | | | | | | KSITE11 | KCKQVRFS | |
| | | | | | | | KSITE30 | | |
| | | | | | | | KSITE31 | | |
| | | | | | | | KSITE32 | | |
| Number of Utility(32 sites) | | 6 | 0 | 0 | 16=(32/4)*2 | 16=(32/4)*2 | 32 | 12 | 82 |

9117 and G6K Controlled by Master relay.

| | # of sites-> | 32 | UDPS+5V Output Current: 3A | UP5V Output Current: 6.4 A | XPP5 Output Current: 8A | XPP3V3 Output Current: 6A | |
|---|---|---|---|---|---|---|---|
| Relay Type | mA | Total per site | UDPS+5V Consumption Current (mA) | UP5V Consumption Current (mA) | XPP5 Consumption Current (mA) | XPP3V3 Consumption Current(mA) | G3VM Relay Driver (<1.7A) |
| G3VM (Master Relay) | 7.1 | 45 | | | | 318 | |
| BSZ (1 util for 4 relays) | 2.5 | 6 | | | 480 | | |
| AQY (1 util for 4 relays) | 7.1 | 2 | | | | 455 | |
| 9117 (thru Master Relay) | 12.5 | 3 | | 1200 | | | 400 |
| G6K (thru Master Relay) | 25 | 6 | | 4800 | | | 924.3212016 |
| G6J | 28.9 | 2 | | | 1849 | | |
| C247S | 6.8 | 2 | | | | 437 | |
| PMUX-F | 8 | 48 | | | 1536 | | |
| PMUX-S | 5 | 30 | | | 960 | | |
| PMUX Idle | 100 | 50 | | | 1600 | | |
| Total Current mA (PMUX used) -> | | | 0 | 6000 | 4825 | 1210 | |
| Total Current mA (PMUX unused) -> | | | 0 | 6000 | 3929 | 1210 | |
| Current Usage | | | 0.00% | 93.75% | 60.31% | 20.17% | |

## Utility Power Analysis

| Type | Output | Consumption | Ratio |
|---|---|---|---|
| UP5V | 6.4A | 6A | 93.75% |
| XPP5V | 8A | 4.825A | 60.31% |
| XPP3V | 6A | 1.21A | 20.17% |
| Relay driver | 1.7A | <1.7A | ---------- |

TestConX 中国 China

Challenging solution design and application for automotive electronic testing on the Advantest V93000 tester

2022

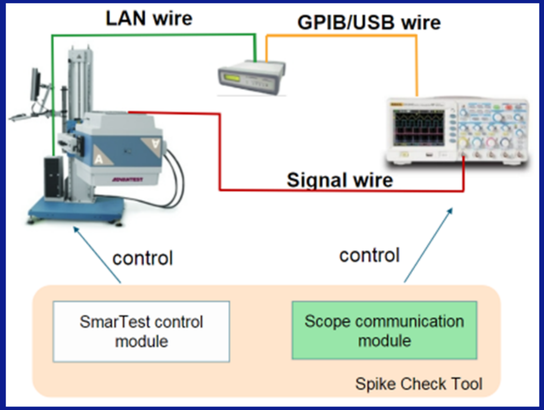
# Quality and safety software check tool application

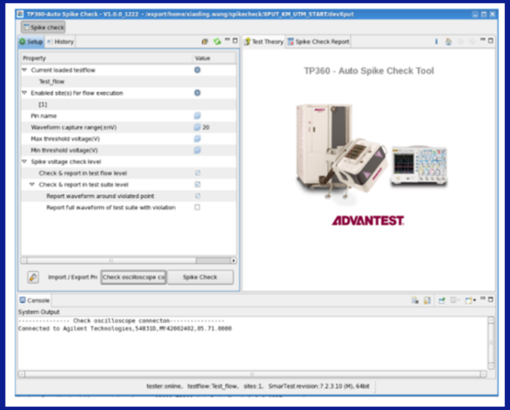
Even though we can do a lot when do the test solution, but still where you can't think about it.
2 tools can help check or avoid the risk:

- ❑ **Spike check tool**
- ❑ Alarm handling

**"Auto spike check" is a GUI software to check spike voltage with external oscilloscope**

- Auto detect the spikes in the test flow with scope
- Auto identify and locate the spike/violation
- Report the detailed spike/violation information



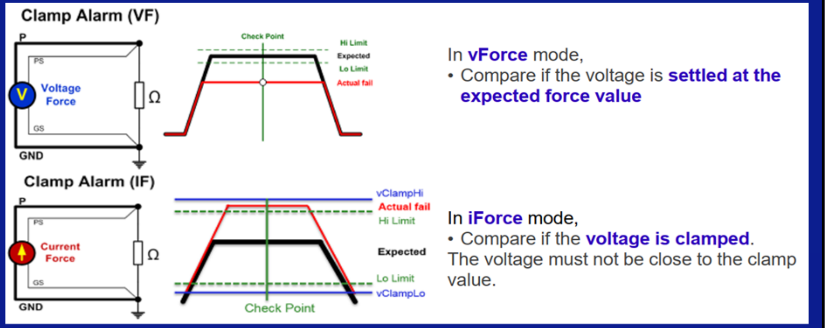
# Quality and safety software check tool application

## ❑ Alarm handling

**Alarm handling is a smartRDI feature by inserting compare events between measurements and judging pass or fail based on alarm limit values set in the alarm setup file.**

Purpose: Detect when a programmed force value is not present at the DUT

- Verify all conditions for test items of automotive applications
- Measure and report the detailed pass or fail information



# Quality and safety software check tool application

## How to apply to tests?

- Activate Alarm handling in the RDI_Configure file, including global parameter and per pin parameter
- SmartRDI inserts alarm check events after measurement without user code change automatically

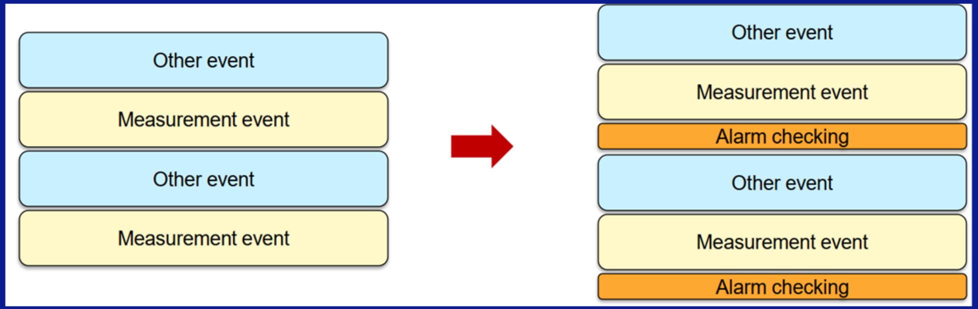
```
# Alarm setup file referenced by testmethod/RDI_configure
# TDC Concept 345140
# enable for debug to get the measurement results in the UI report window
DEBUG_VALUE = FALSE # default is FALSE, when TRUE all results of the vMeas event will be uploaded and shown in the UI Report window

SET DEFAULT  # Applied by default, S1520
GlobalLimitRelForce = 10%
GlobalLimitMinDisForce = 10 mV
GlobalLimitRelClamp = 10 mV
PINS AVI1_AVI AVI2_AVI AVI3_AVI AVI4_AVI AVI5_AVI AVI6_AVI AVI7_AVI AVI8_AVI VS1_FVI

# needs to be pins, it does not resolve groups or ports, no comma(?)
# No local limit value defined means that global values are applied.
##PINS VCC1_AVI,VCC2_AVI,VSSBC_FVI,HSS_DCDC_FVI
##LimitRelForce = 10%
##LimitMinDisForce = 10 mV

##SET Demo_Alarm_SETUP
##PINS VCC1_AVI,VCC2_AVI,VSSBC_FVI,HSS_DCDC_FVI
##LimitRelForce = 10%
##LimitMinDisForce = 100 mV

##PINS CANL_AVI CANH_AVI
##LimitLo = -0.1 V
##LimitHi = 68 V
```



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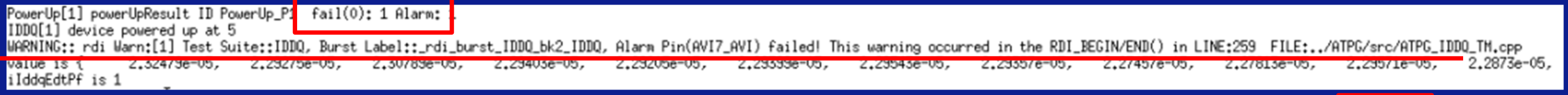
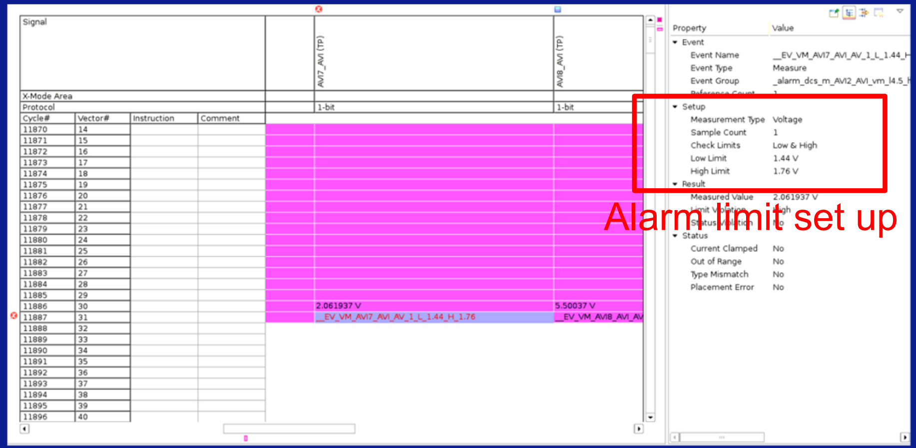
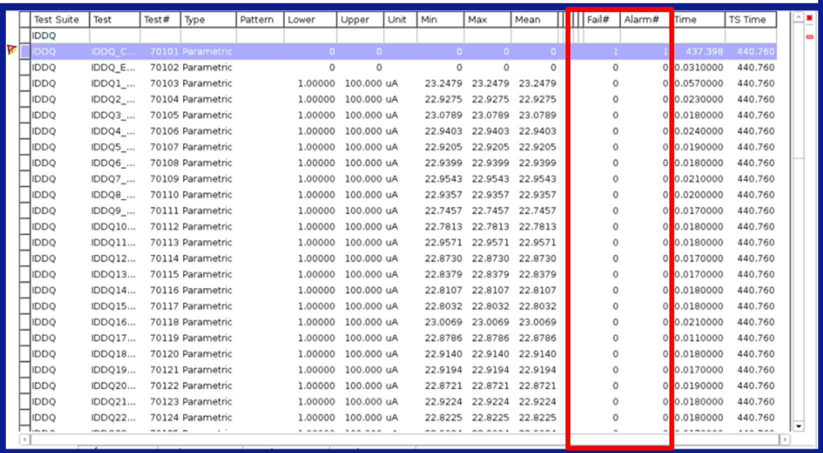
## Quality and safety software check tool application

### How to apply to tests?

- When the alarm failed, we can get the failed information below in pattern, UI report and data log.



If test value is passed, but Alarm failed, The test will be also failed at last.

Benefits:
Alarm handling can improve DC test program quality.

# Summary

- **Floating resources using**
  - AVI64 DiffVM
  - AVI64 HCU
  - FVI16 per pin
- **Different V/I level card connection**
  - Damaged situations
  - Protection circuit
  - Possible connections
- **Relay control**
  - Utility bit expansion
  - Systematic relay solution
- Software check tool
  - Alarm handing
  - Spike check tool

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