Solving Socket Power Integrity; The Last Link in the Chain

Don Thompson – Advantest / R&D Altanova

David Unger – Advantest / R&D Altanova

TestConX™

Mesa, Arizona • May 1-4, 2022

ADVANTEST® R&D Altanova®

Review: What is Power Integrity?

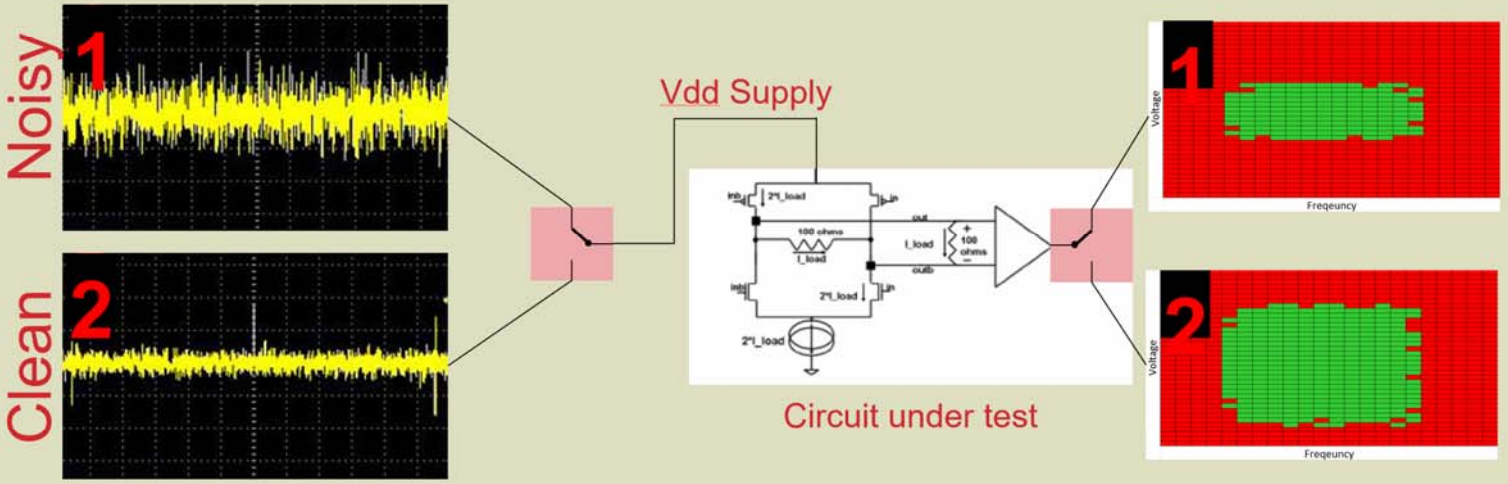
What is Power Integrity?

- Power Integrity is the behavior of your Power Distribution Network (PDN) as it relates to frequency
- Closely related is IR drop analysis, which is the behavior of your device at DC
  - IR drop analysis is relatively intuitive and deals with resistance and thermal concerns with in the board. *This is not addressed in this paper.*
- Power Integrity is typically represented as an Impedance. *(That's another way of saying "resistance as it relates to frequency"!)*

TestConX™ 2 2020

Why Do We Care About Power Integrity?

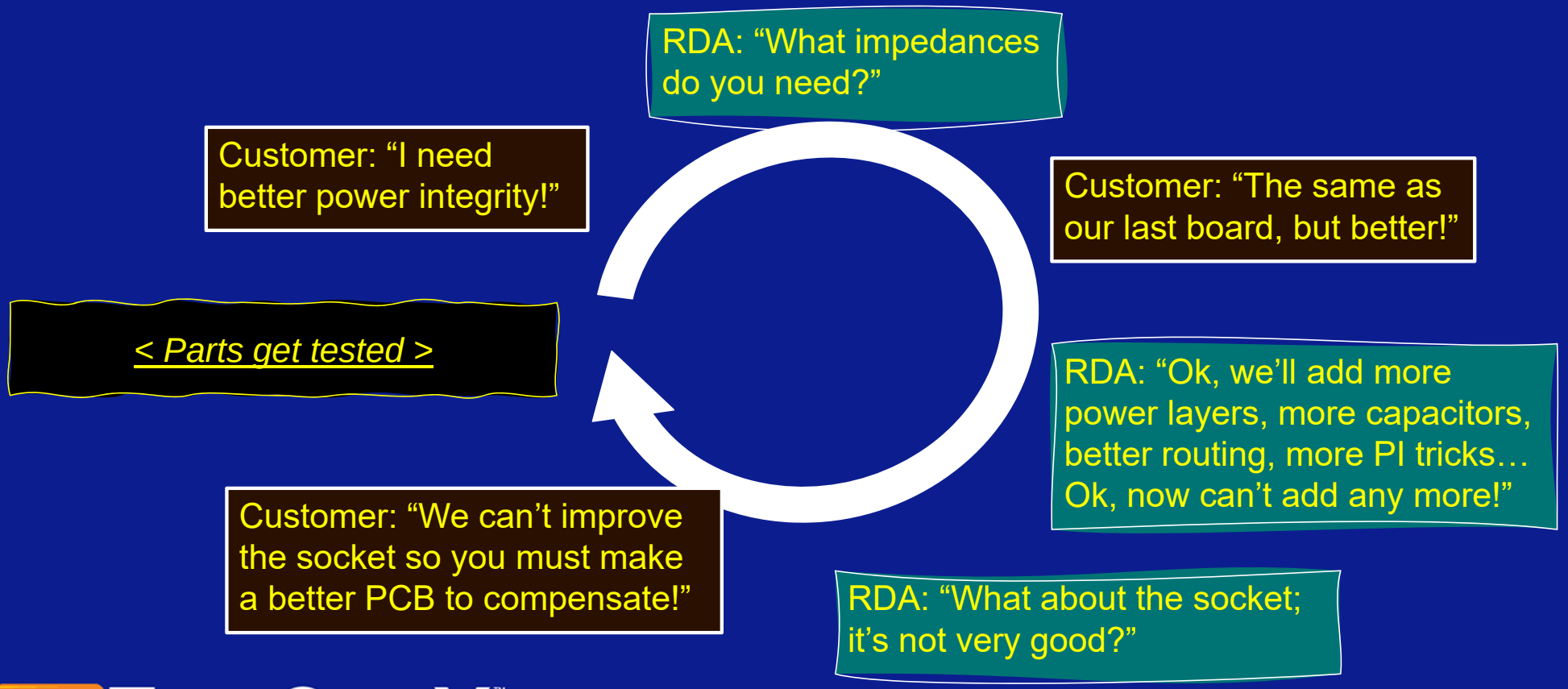
- PI relates to how the power supply ripples under load. (Both Vdd and GND!)
- As your power supply ripples, your ability to test your part will be reduced. Ripple on your supply will lead to a yield hit and you may not even be aware of it!



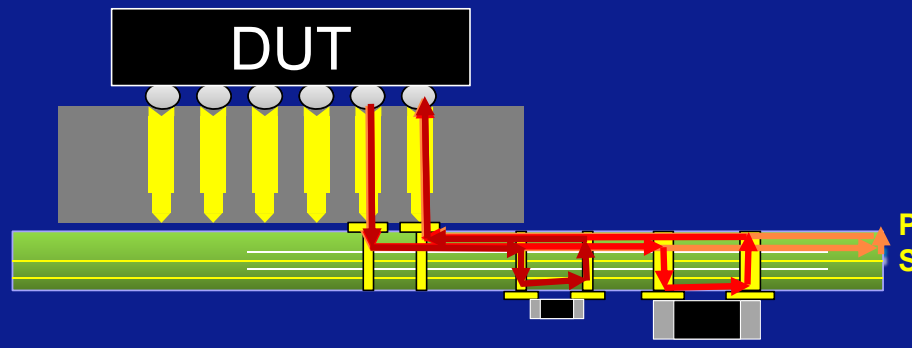
TestConX™

3 2020

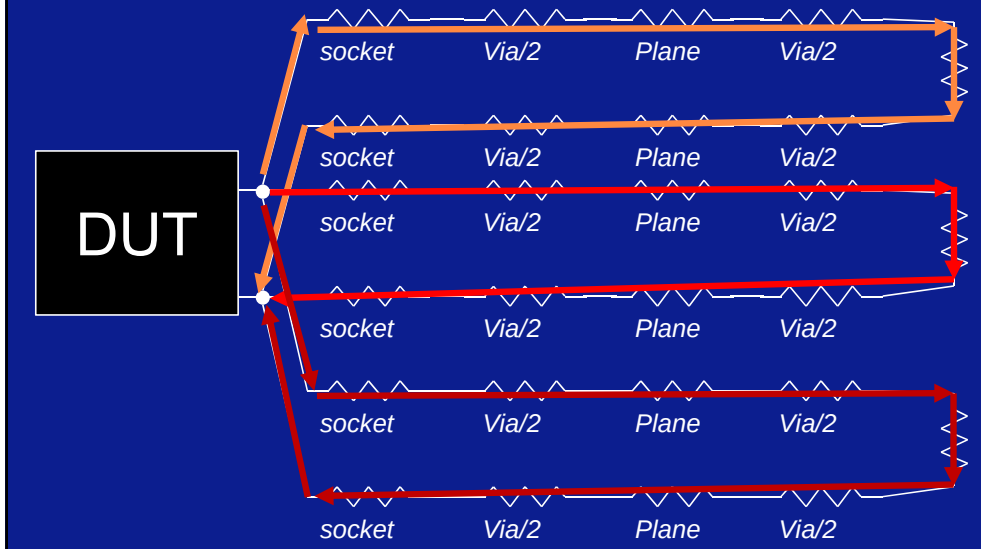
The Typical Model for PCB Power Integrity



Board Impedance from the DUT (Frequency Domain View)



- At DC, path of least resistance is to the power supply
- At medium frequencies, the path of least resistance is to the bulk or mid sized caps
- At High Frequencies, the path of least resistance is to the high speed caps



0 Hz to ~ 10 kHz

~10 kHz to ~ 1 MHz

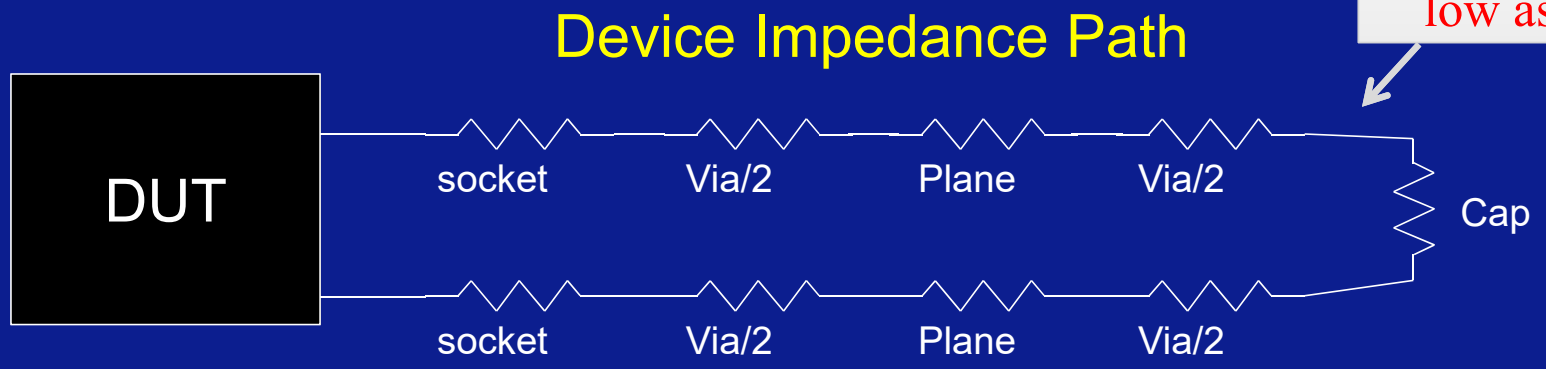
~1 MHz to ~ 50(?) MHz

A Closer Look…

- Path impedance is a measure of how well the by-pass caps can get rid of HF energy
- This determines the capacitor's ability to "help" the DUT with PI

- Inductors and capacitors look like resistance at a fixed frequency (Remember phasors!)
- The higher the path inductance, the higher the resistance at frequency

We want this path resistance to be as low as possible!



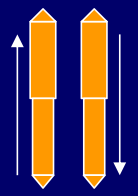
Plane Versus Pin or Via

An ideal low inductance transmission line is a wide conductor, a wide return path, that are very close together. This is your typical power plane, so we expect this to be much lower than spring-pins or vias.

So let's do a comparison:

Inductance of a single pair of power ground spring pins: (vias will be very similar)

Assumed 30 mil dia, 40 mil pitch, 200 long



$$L = \frac{\mu_0 * L}{\pi} cosh^{-1} \frac{S}{D}$$

L = 2.1nH

Inductance of a single power & ground plane:

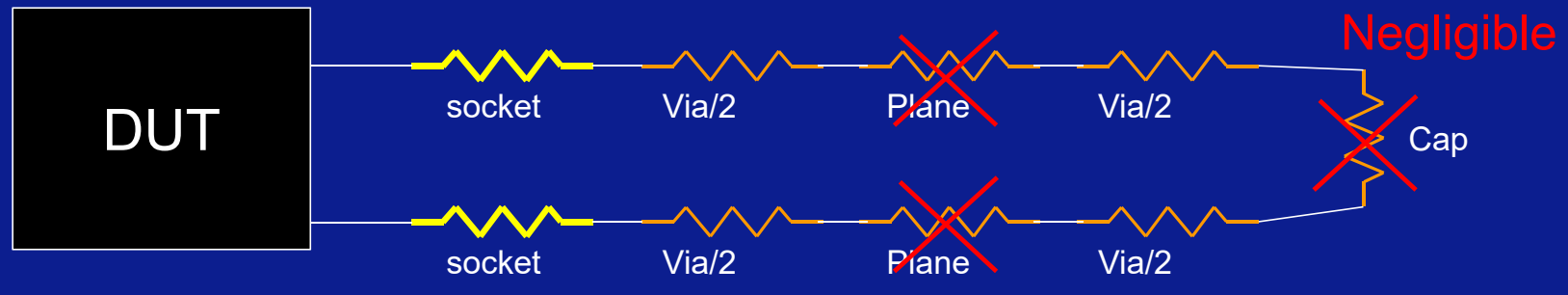
Assumed 1" wide, 1" long, & 15 micron gap

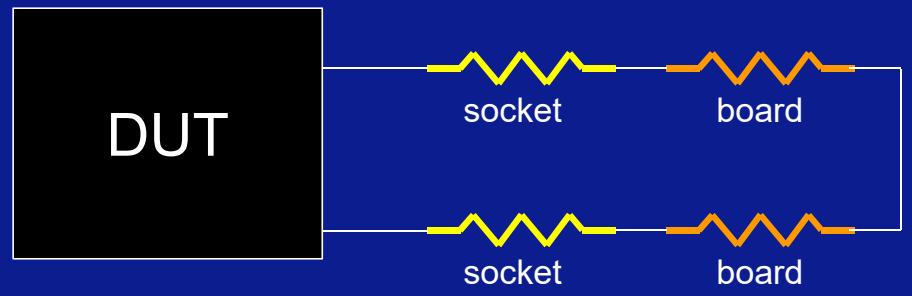
$$L_{planes} = \frac{\mu_{0*S*L}}{W}$$

L = 0.02nH

Inductance of spring pins in this scenario is 100 times more than power planes!

HF DUT Impedance Path Example





- Via and Socket Inductance usually dominate the high frequency response
- Reducing the inductance of these two pieces will dramatically improve high frequency PI performance!
- The DUT socket is also a critical piece of the PI puzzle

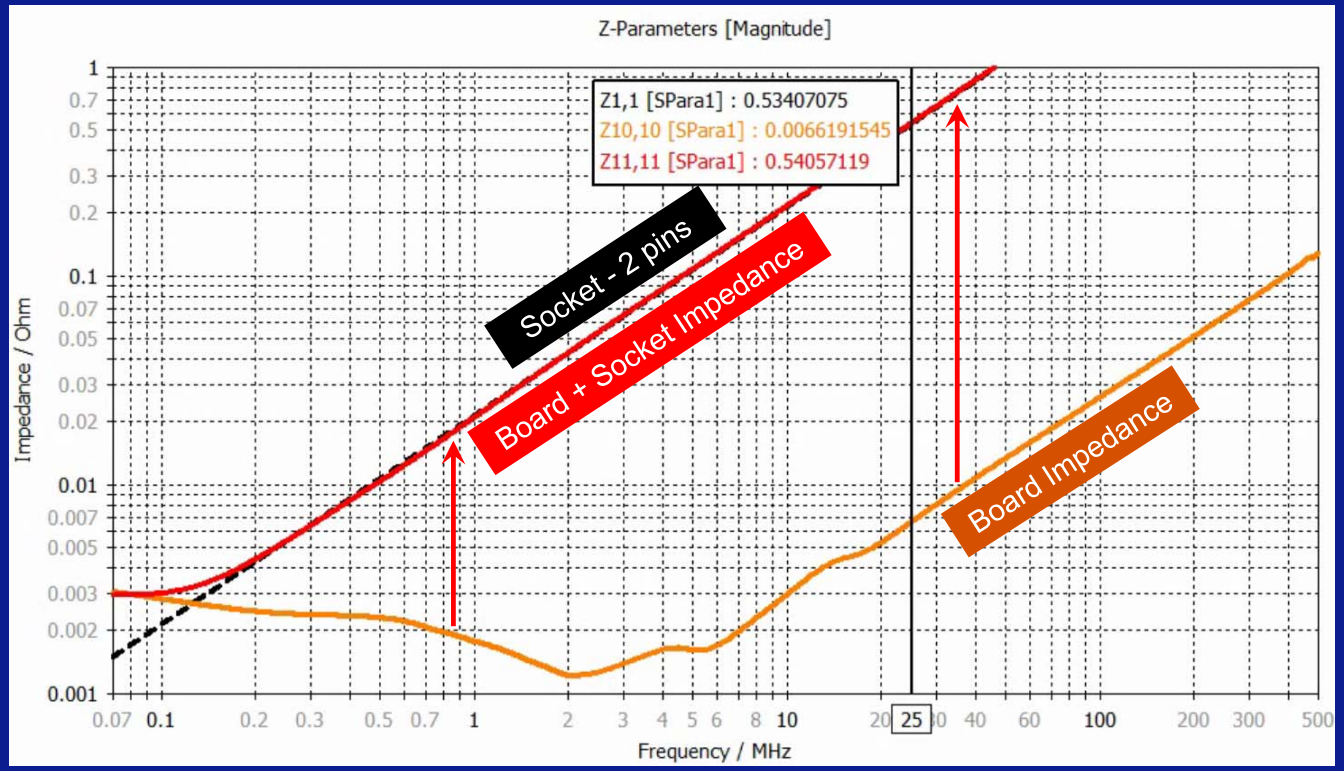
PRACTICAL EXAMPLE: BOARD + SOCKET IMPEDANCE

2 Pin Socket Impedance Impact

Board Impedance = **6.6mΩ**

Socket Impedance = **534mΩ**

Board + Socket = **540mΩ**

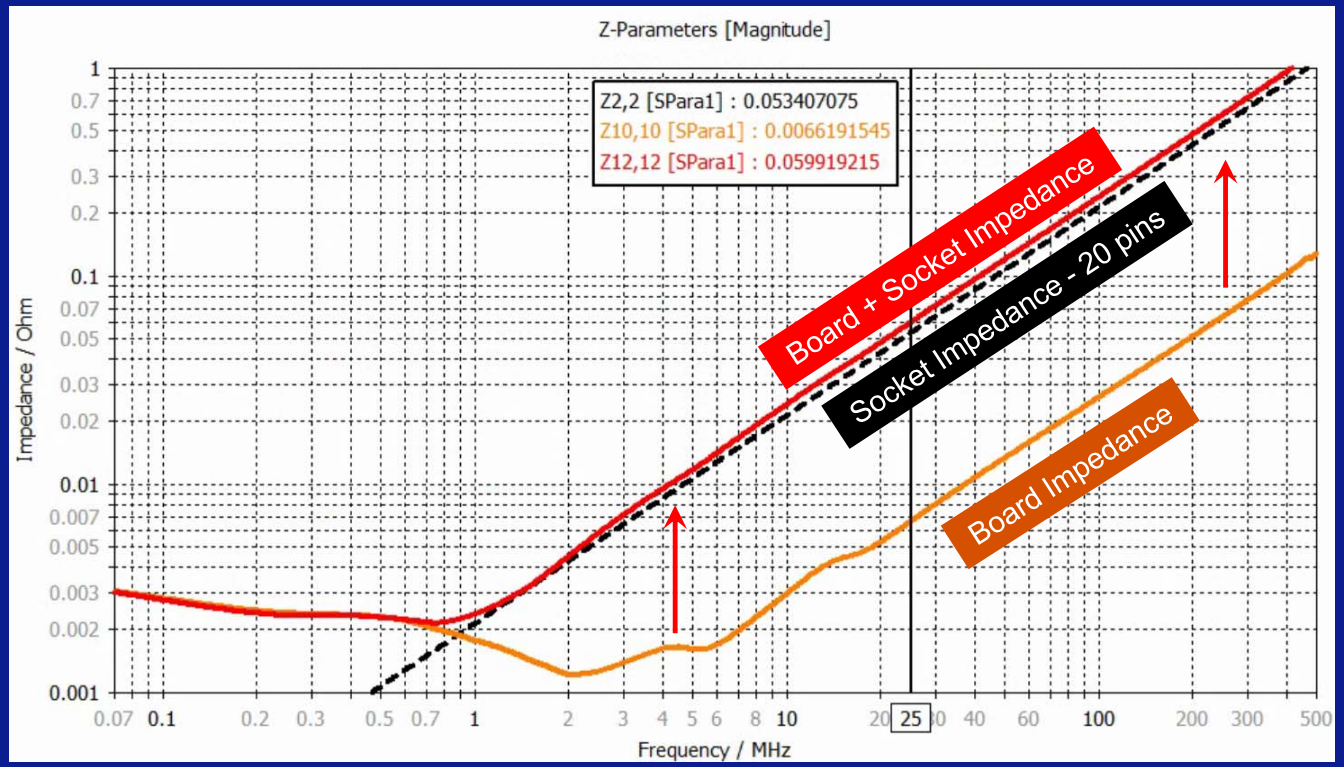


20 Pin Socket Impedance Impact

Board Impedance = **6.6mΩ**

Socket Impedance = **59.9mΩ**

Board + Socket = **66.2mΩ**

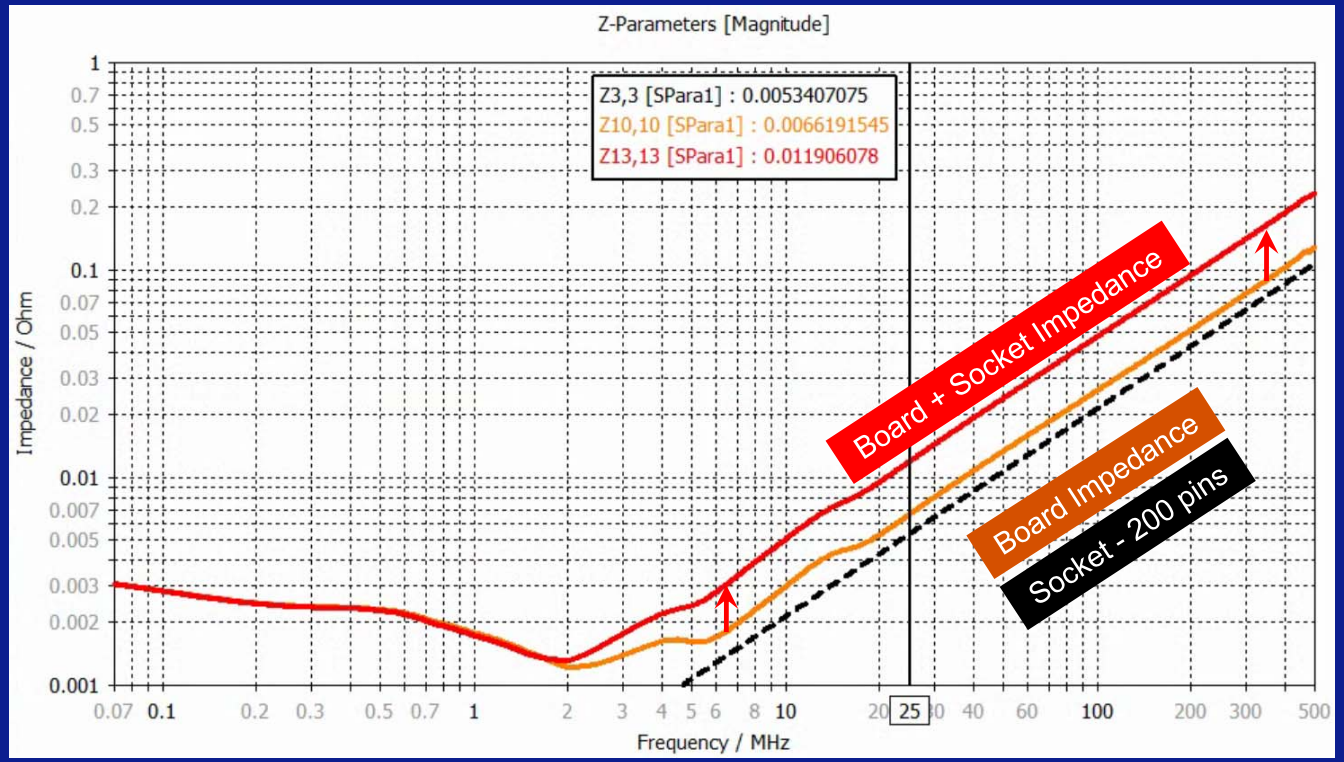


200 Pin Socket Impedance Impact

Board Impedance = **6.6mΩ**

Socket Impedance = **5.3mΩ**

Board + Socket = **11.9mΩ**



Practical Example

Real Example:

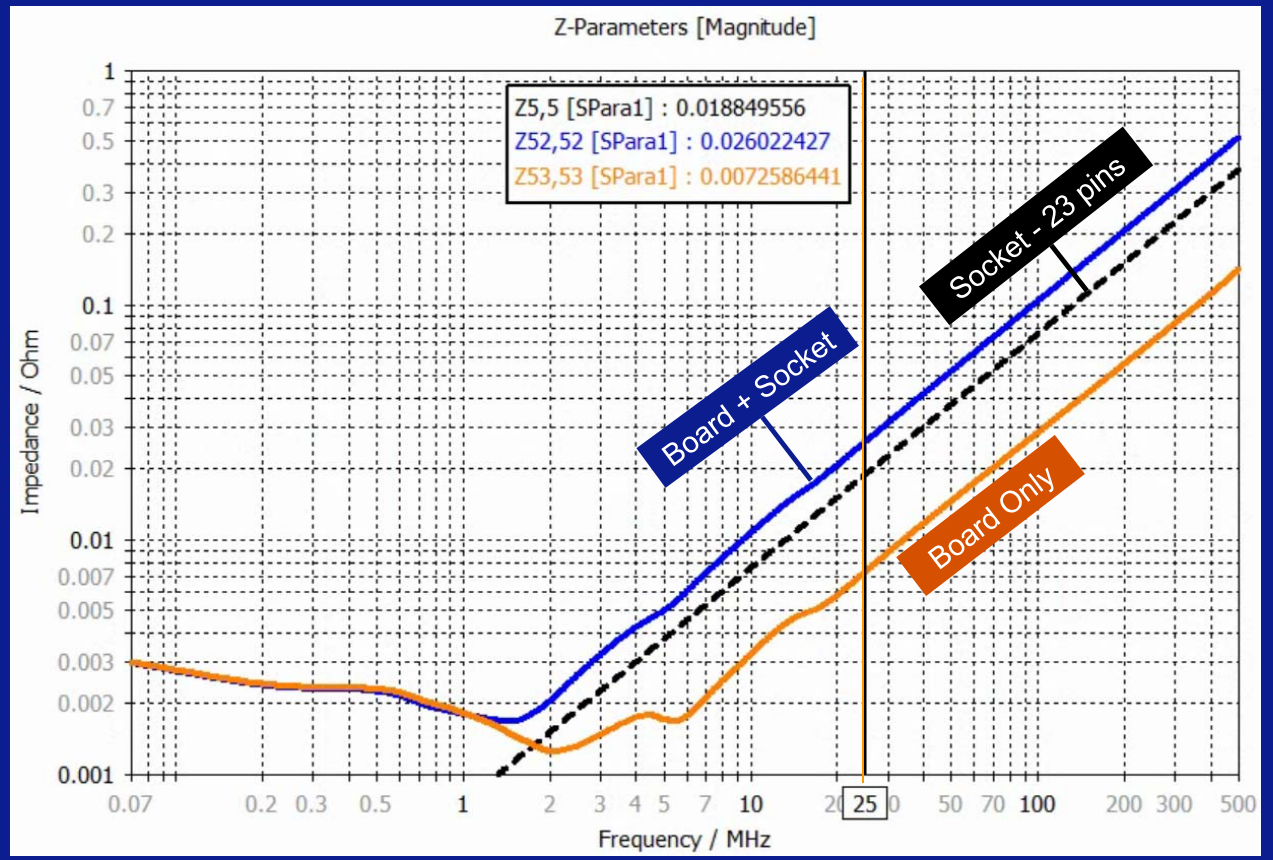
- **Real board simulated in Sigrity, 23 power pin supply**
- **Socket inductance for 23 power / 23 gnd pins**

Board Impedance: 7mΩ

Socket Impedance: 19mΩ

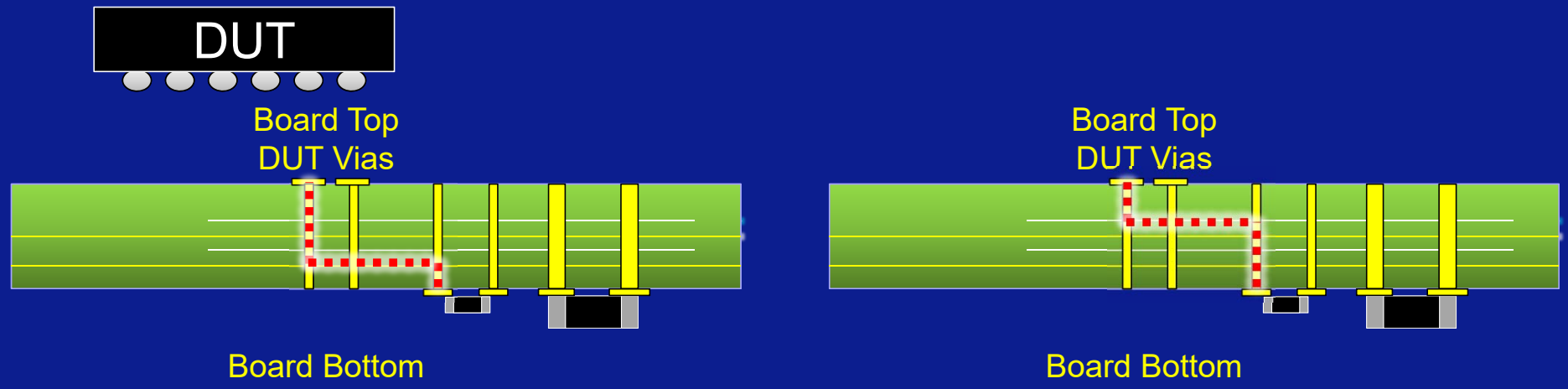
Total Impedance: 26mΩ

In this example, the socket accounts for 75% of total inductance!!



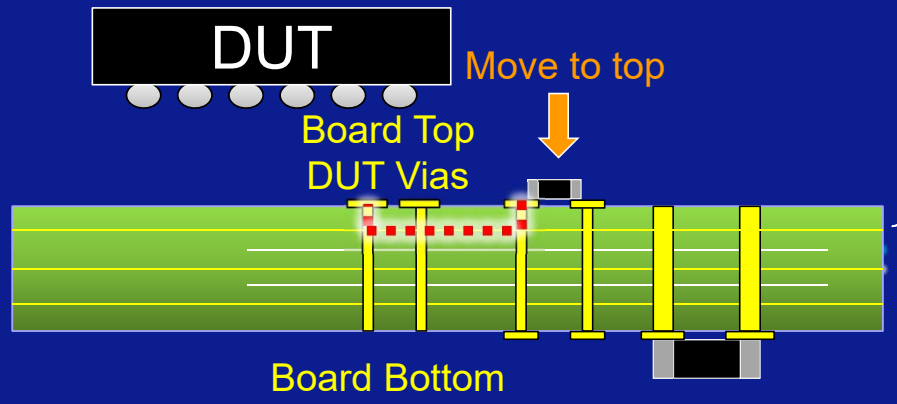
IMPROVING THE BOARD

Via Inductance in a PCB



- If capacitors are on bottom of the board, they will always go through exactly 1 via length of inductance

Via Inductance in a PCB



Critical power nets will have power planes near the top of the board

Remember: (*L* = *Via Length*)

$$Inductance = \frac{\mu_0 * L}{\pi} cosh^{-1} \frac{S}{D}$$

- Via inductance / length can be decreased by putting high-speed caps on top of the board
- The via inductance becomes equal to twice the distance to the power plane
- Via inductance will decrease linearly with a via length reduction

Options for Improving Via Inductance

- Add high-speed caps on top of board
  - Move critical power planes to top of board
- Increase via diameter 

- Add more vias 

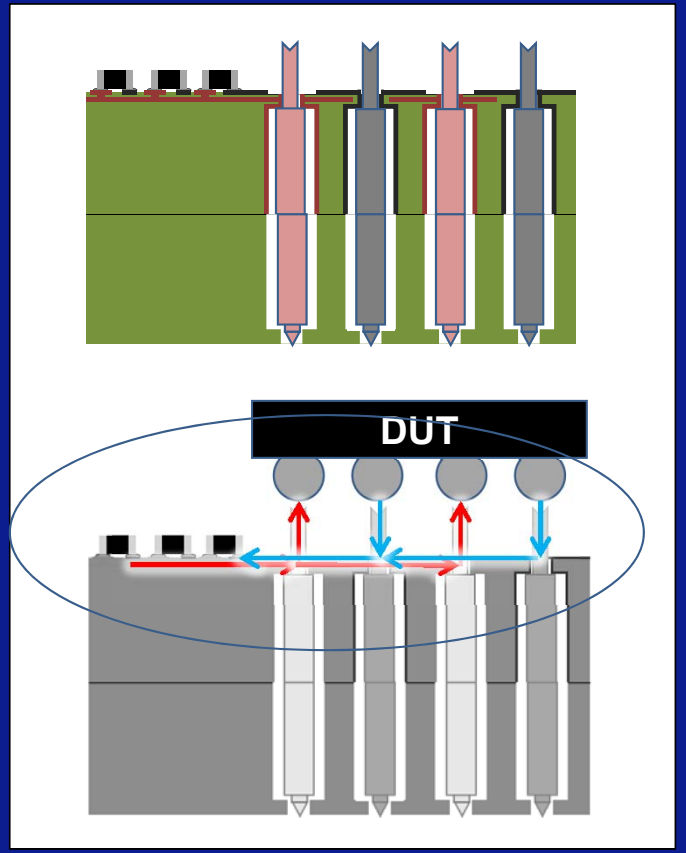
- Improve power plane routing *(a game of trade-offs)*

How To Improve Socket Inductance

…how putting capacitors in the socket?

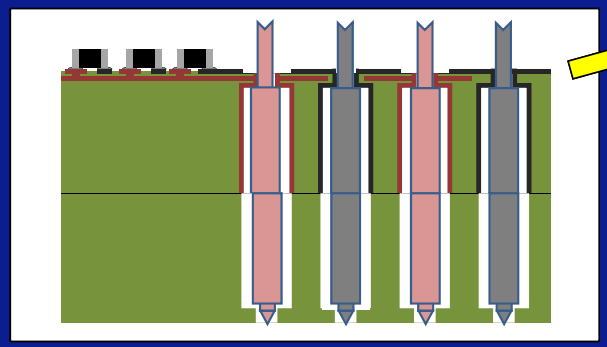
Moving Caps to The Top of the Socket

- Use PCB technology to add capacitors to socket
- Cuts out 90% of spring-pin inductance
- Keep capacitors outside pin array and route them in with low inductance power planes

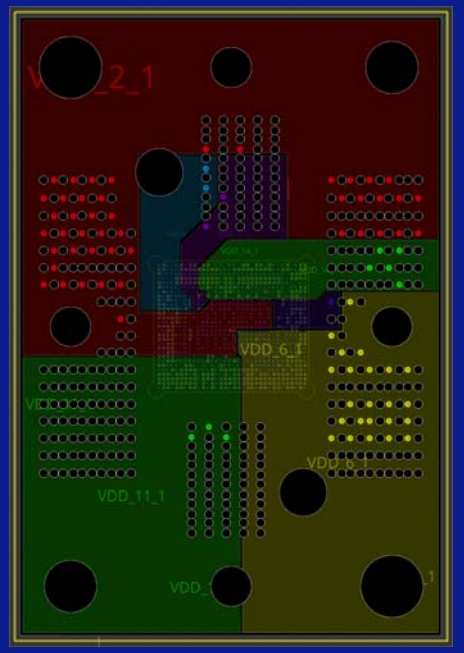


Board Design

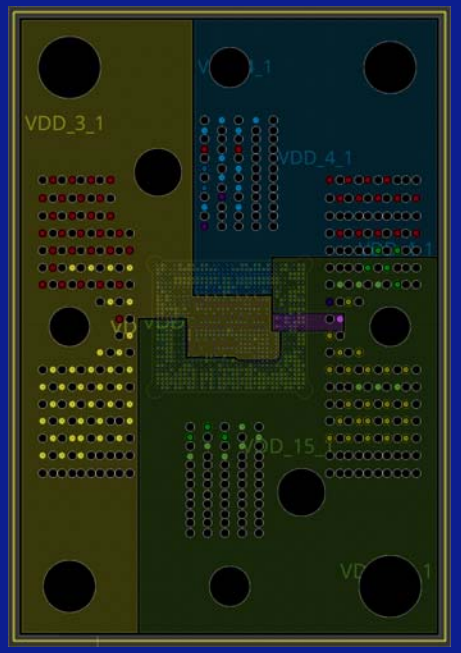
- Multiple power planes can connect even the densest DUT
- Any quantity of capacitors can be added, only limited by size of socket
- Multiple power planes can be added to reduce inductance or improve routing



PWR1

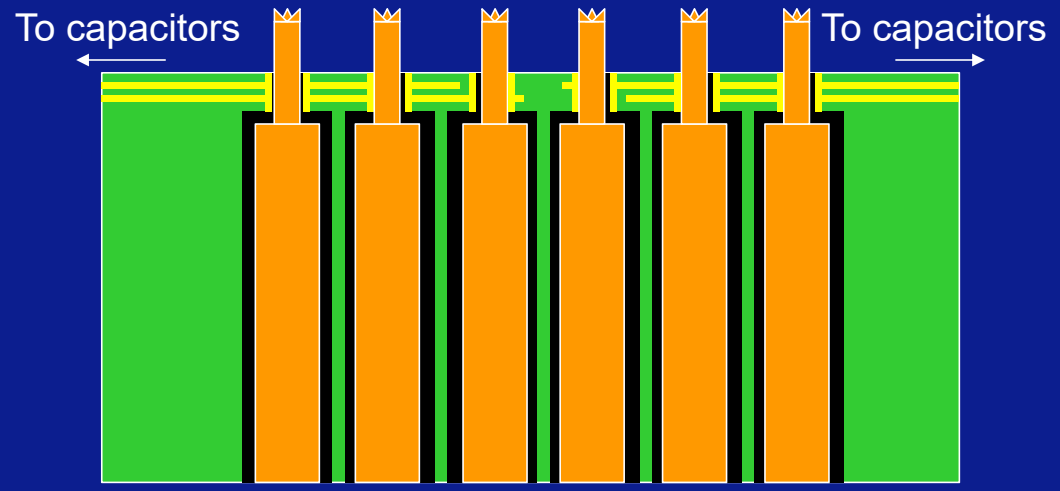


PWR2

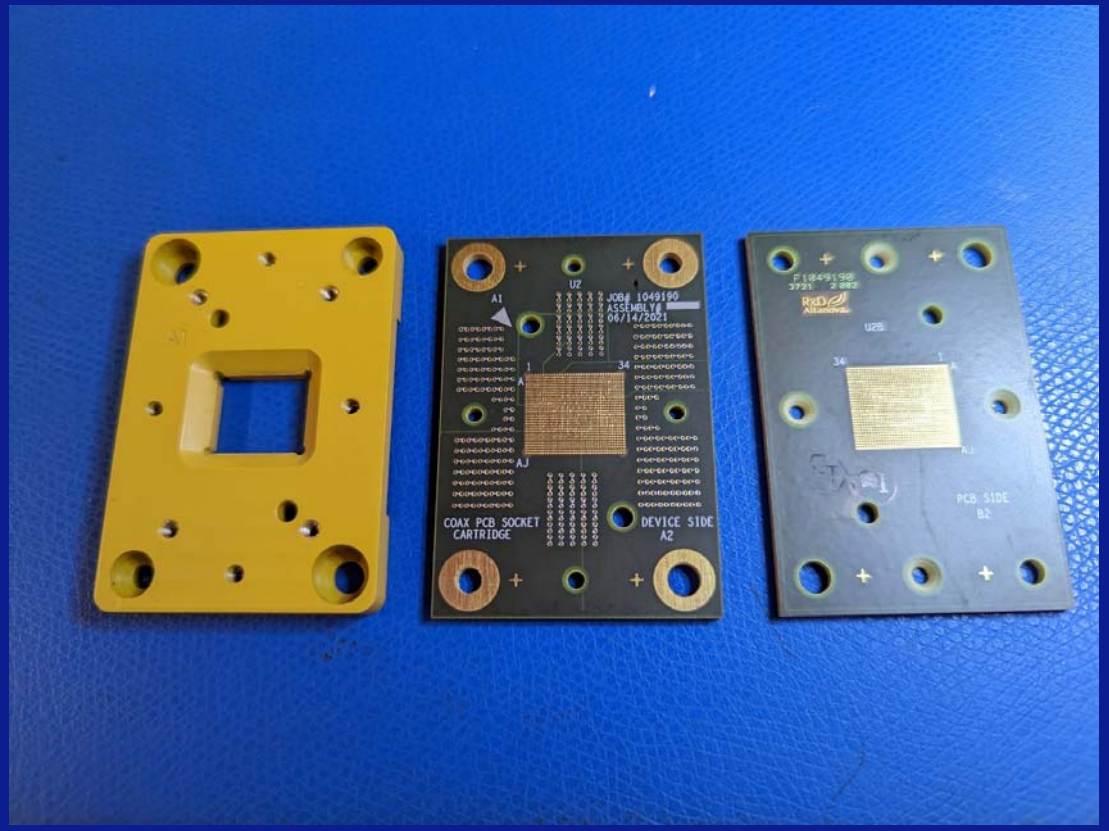


Pin Connection

- Pins are retained in the gold-plated barrel. Any lateral force pushes gold-plated pin against gold-plated barrel making electrical connection.
- While not guaranteeing a connection this has so far been a reliable connection mechanic in prototype testing with > 80% or better connection rate
- This method guarantees normal spring pin behavior with no impact on cycle life or abnormal wear on the pins



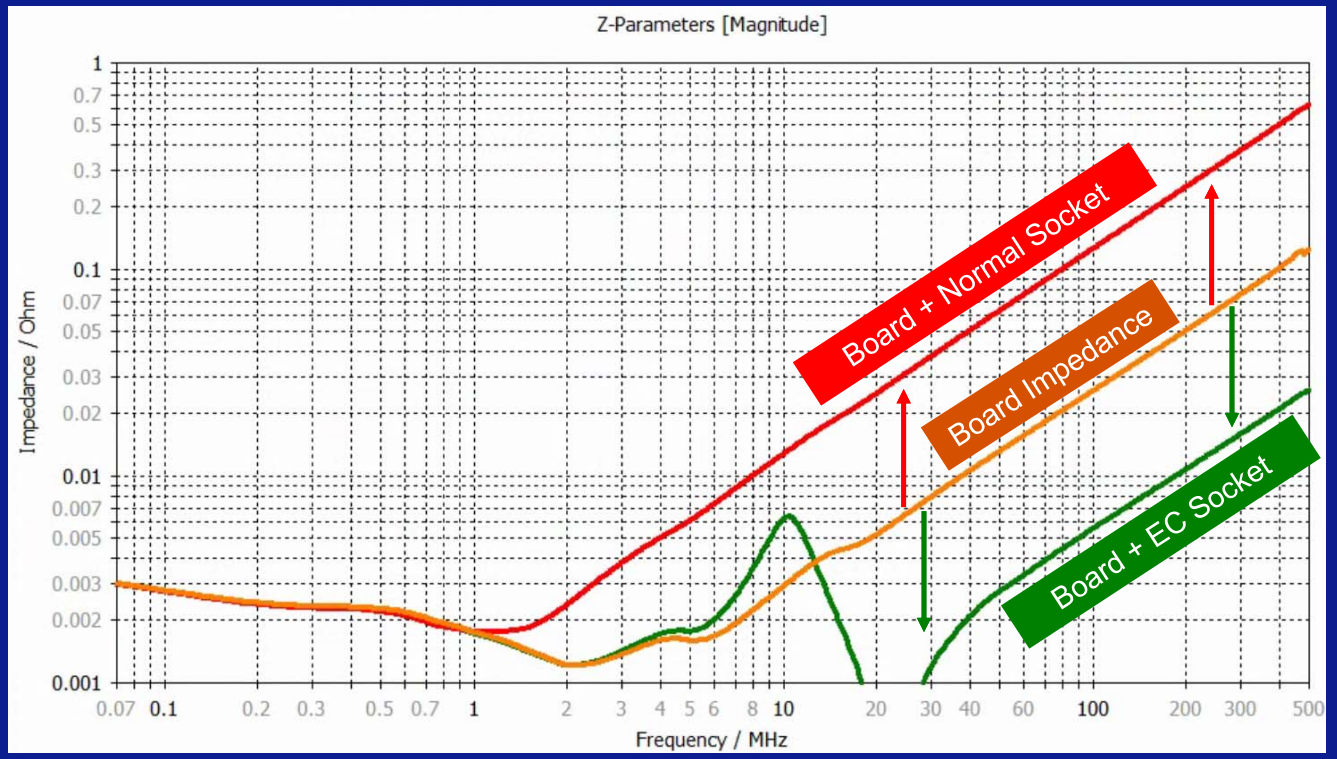
Socket Prototype



EC Socket Improves System Performance

EC Socket improves the power integrity performance!

The EC socket flips the drag to a boost and provides a net benefit at frequencies above 15 MHz



Conclusion

- No matter what you do on the PCB you will never improve on the cutoff frequency imposed by a standard socket's inductance
- A standard socket will always be a drag on PI performance, but by including capacitors in the socket design we can make the socket into a beneficial part of the solution

- R&D Altanova will be bring this to market in partnership with Essai

With Thanks to Our Sponsors!

Premier

Emeritus

Cohu

Johnstech®

Honored

GLOBAL INNOVATION
ISC

WIN SOLUTION

LEENO
Total Interface Solutions

TSE

With Thanks to Our Sponsors!

Distinguished

Industry Partners

With Thanks to Our Sponsors!

Lanyards

Tutorial

Keynote

Keycards

Totebag

Publication Sponsor

COPYRIGHT NOTICE

www.testconx.org