Applications of Advanced Signal Integrity Analysis in DDR5 Memory Validation Platform Design

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Mesa, Arizona • May 1-4, 2022

Agenda

- DDR5 overview
- DDR5 validation platform design challenges
- Advanced signal integrity analysis
- Summary

DDR5 Overview

- High bandwidth with data rate up to 8400 MT/s
- High capacity DIMMs up to 256 GB
- Reduced I/O voltage 1.1 V
- Improved I/O speed by use of DFE and CTLE *
- Better power performance using on-DIMM power management IC modules

* Decision Feedback Equalization and Continuous Time Linear Equalization

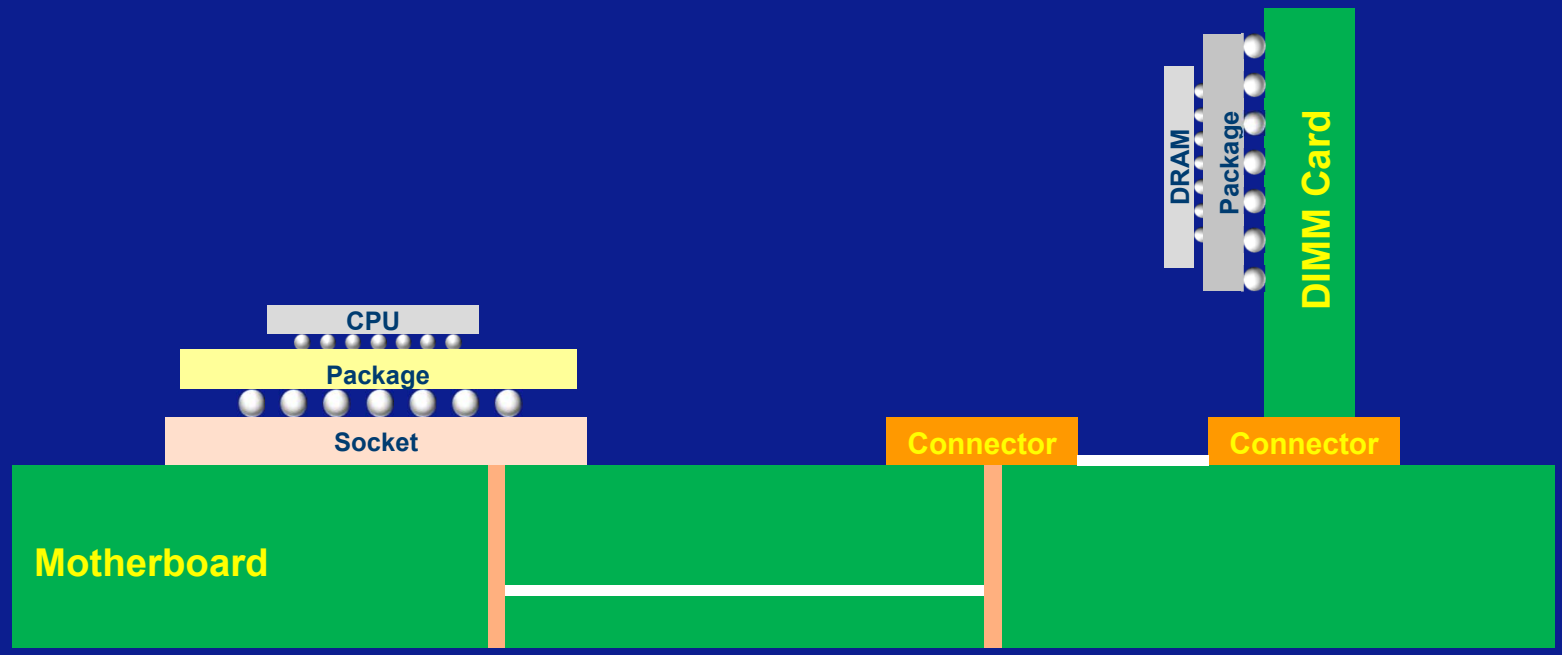
DDR5 Validation Platform Design Challenges

- Accelerated rate of standards evolution
- Shortened design and validation cycles
- Reduced link budget and channel margins
- Tremendous routing constraints on platform design

Advanced Signal Integrity Analysis

- Pre-layout DDR5 channel simulation
- 3D EM (Electromagnetic) model extractions of interconnect
- Post-layout simulation flow
- Tabbed-line design for crosstalk reduction

DDR5 Pre-Layout Simulation Topology



DDR5 one DIMM per channel

Pre-Layout Signal Integrity Analysis

- Coverage of pre-layout DDR5 simulation
  - Define channel topology
  - Evaluate platform enablers such as crosstalk reduction and impedance discontinuity optimization
  - Analyze silicon and interconnect parameters sensitivity
  - Performance optimization
  - Identify end-to-end solution space

Simulation Model Assumptions

- Memory controller buffer models (IBIS-AMI *)
- CPU and DRAM package models
- Socket
- Motherboard trace and vias
- DIMM connector
- DIMM card

* IBIS: Input/output Buffer Information Specification
IBIS-AMI: IBIS Algorithmic Modeling Interface.

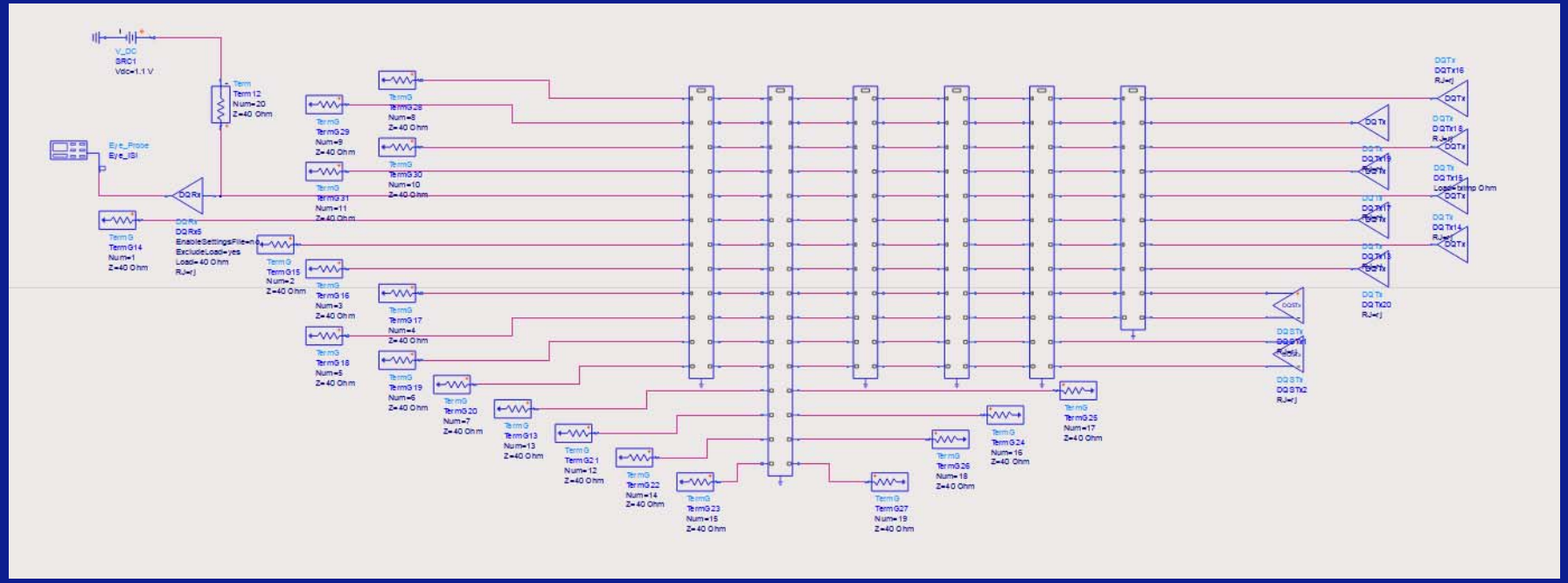
Channel and Silicon Parameter Analysis

- Interconnect impedance mismatch
- Channel insertion loss, routing length
- Crosstalk impact
- CPU and DRAM equalization optimization
  - CTLE (Continuous-Time Linear Equalizer)
  - DFE (Decision Feedback Equalizer)
- Random and deterministic jitter (Rj and Dj)

Channel and Silicon Parameters Optimization

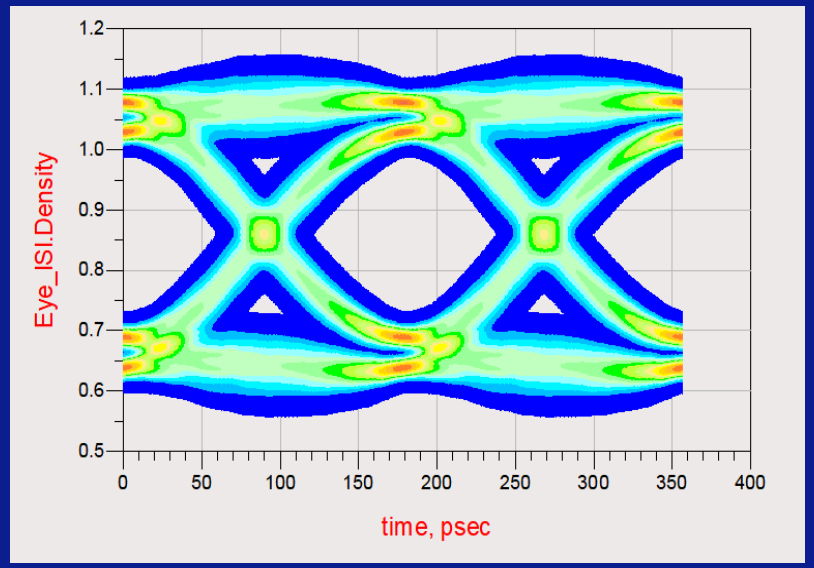
- PCB stackup selection
- Routing layer study
- Channel impedance optimization
- Via type and back drilling
- DDR5 solution space

DDR5 DQ Read Simulation Flow



Simulation flow integrates parameterized interconnect models

DDR5 DQ Read Eye Margins at 5600 MT/s



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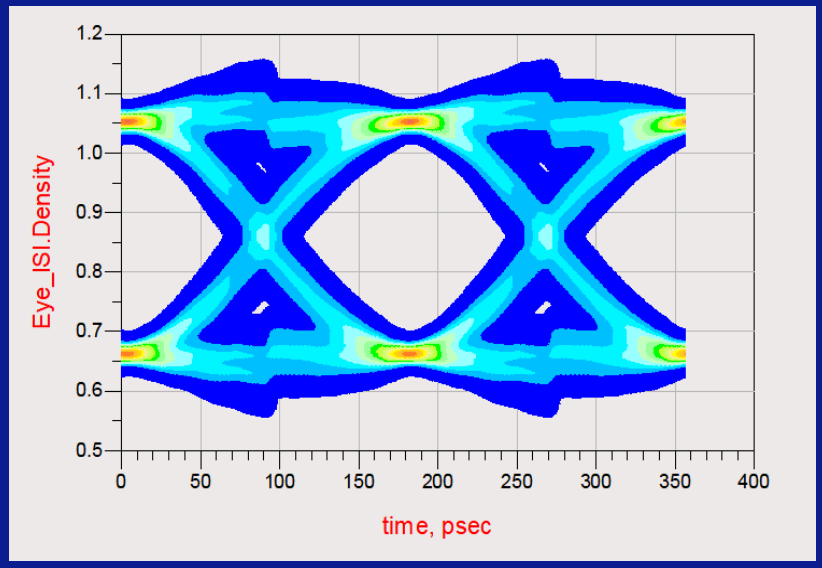
HeightAtBER	0.217

DFE disabled



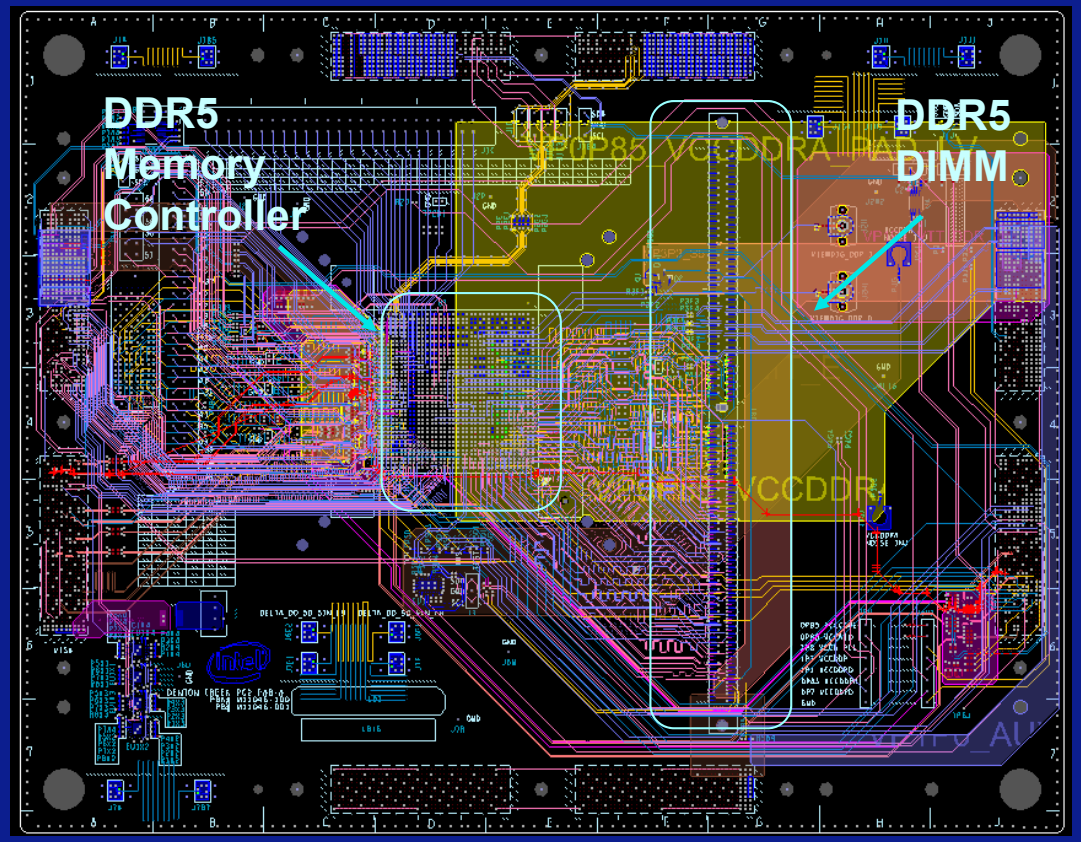
measurement	Summary
WidthAtBER	1.027E-10
HeightAtBER	0.275

DFE enabled

DDR5 Post-Layout Simulation

- PCB stackup and manufacturing technology definition
- Via implementations (through hole, blind, staggered/stacked micro vias) models
- Routing constraints creations
- Component placements, board layout, and routing
- Topology models extraction using 3D EM solvers

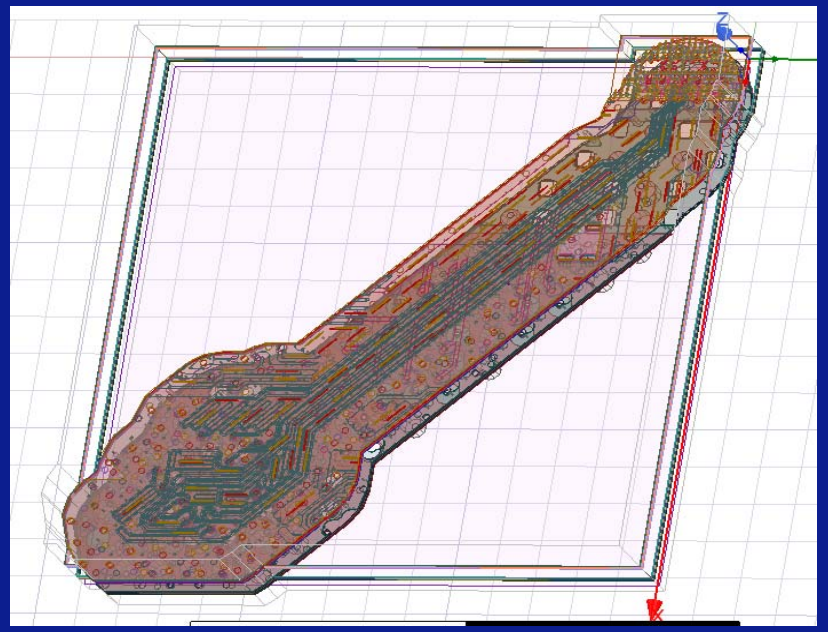
DDR5 IP Validation Platform



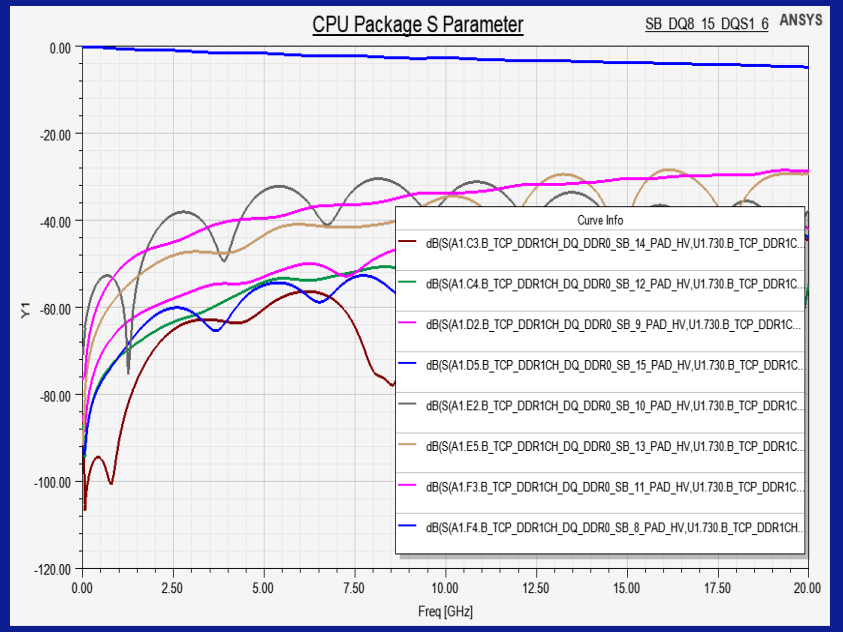
	Surface	
1	TOP Conductor	
	Dielectric	
2	L02_GND Plane	
	Dielectric	
3	L03_SIG Conductor	
	Dielectric	
4	L04_GND Plane	
	Dielectric	
5	L05_SIG Conductor	
	Dielectric	
6	L06_GND Plane	
	Dielectric	
7	L07_SIG Conductor	
	Dielectric	
8	L08_GND Plane	
	Dielectric	
9	L09_SIG Conductor	
	Dielectric	
10	L10_GND Plane	
	Dielectric	
11	L11_PWR Plane	
	Dielectric	
12	L12_PWR Plane	
	Dielectric	
13	L13_PWR Plane	
	Dielectric	
14	L14_PWR Plane	
	Dielectric	
15	L15_GND Plane	
	Dielectric	
16	L16_SIG Conductor	
	Dielectric	
17	L17_GND Plane	
	Dielectric	
18	L18_SIG Conductor	
	Dielectric	
19	L19_GND Plane	
	Dielectric	
20	L20_SIG Conductor	
	Dielectric	
21	L21_GND Plane	
	Dielectric	
22	L22_SIG Conductor	
	Dielectric	
23	L23_GND Plane	
	Dielectric	
24	BOTTOM Conductor	
	Surface	

PCB Board stackup

3D EM Extraction of DDR5 Package

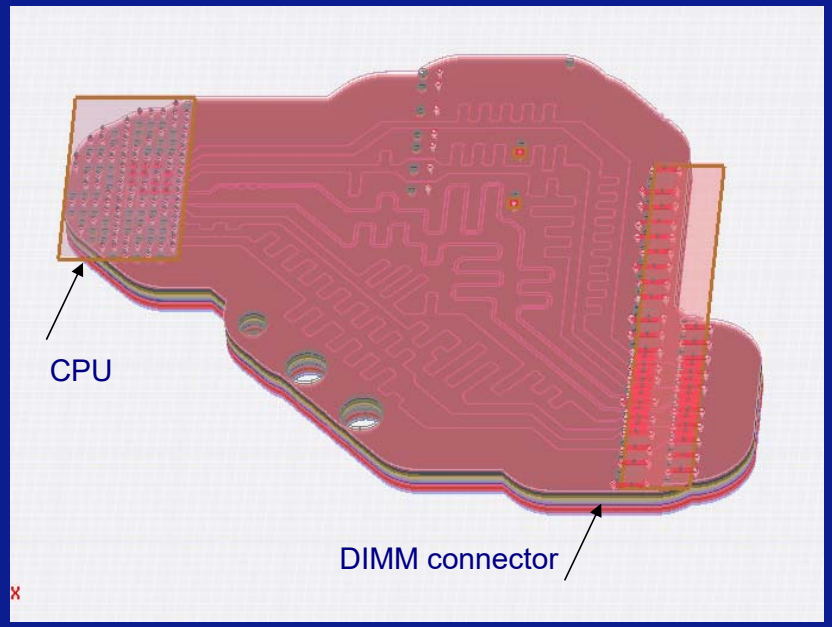


Package 3D model

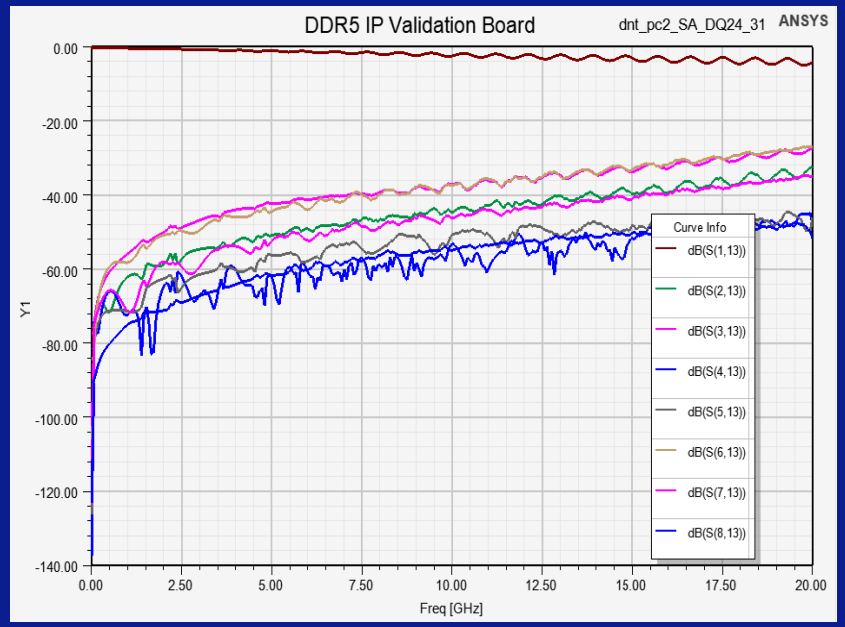


Insertion loss and crosstalk

3D EM Extraction of DDR5 Board

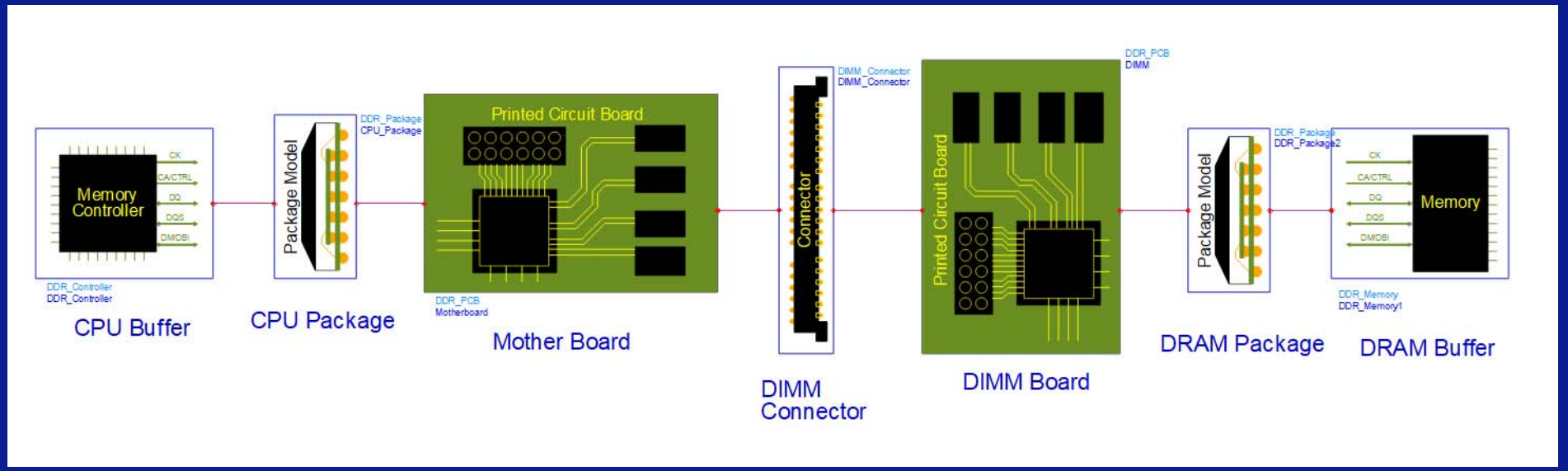


Validation board 3D model



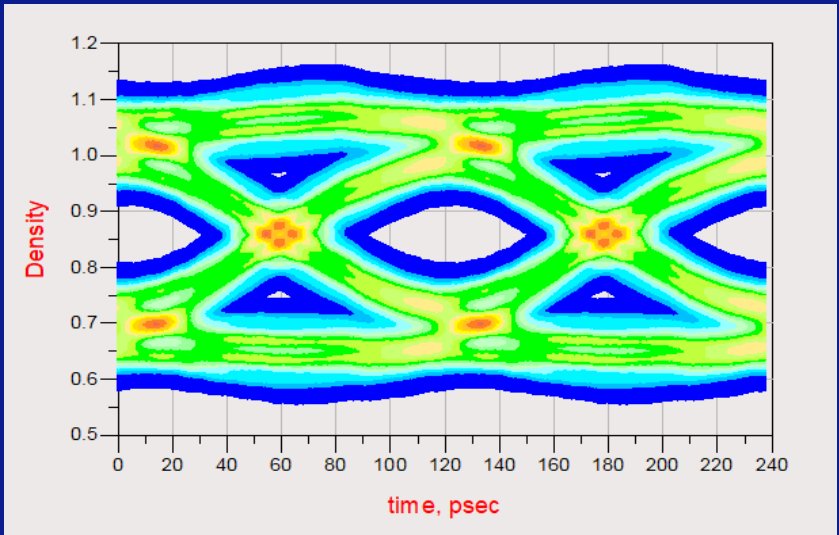
Insertion loss and crosstalk

DDR5 Post Layout Simulation Flow



Simulation flow integrates interconnect 3D EM models

DDR5 DQ Read Eye Margins at 8400 MT/s



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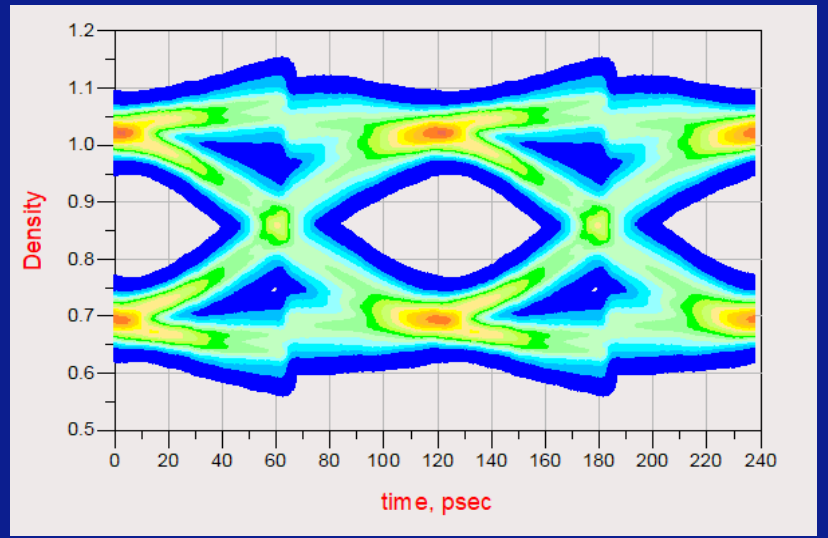
HeightAtBER	0.038

DFE disabled



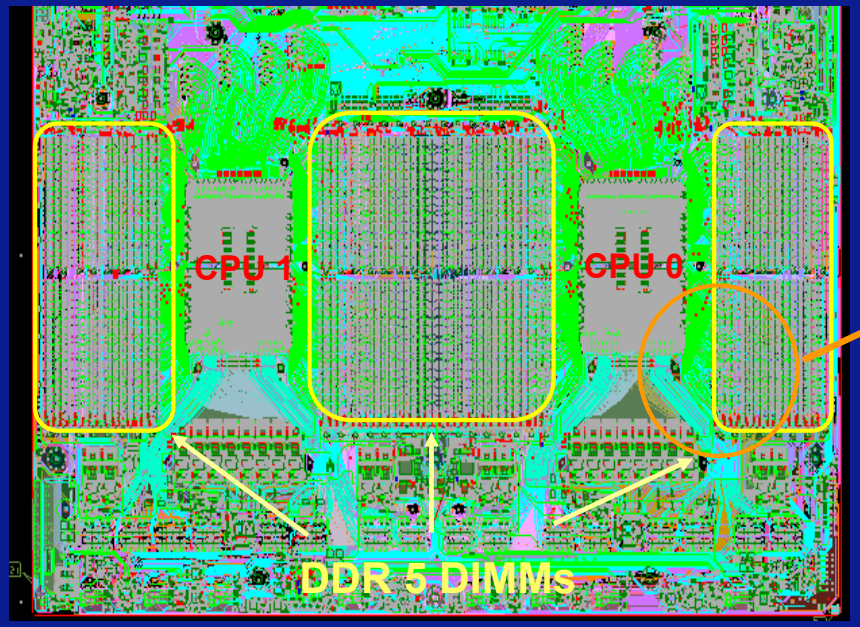
measurement	Summary
WidthAtBER	5.298E-11
HeightAtBER	0.124

DFE enabled

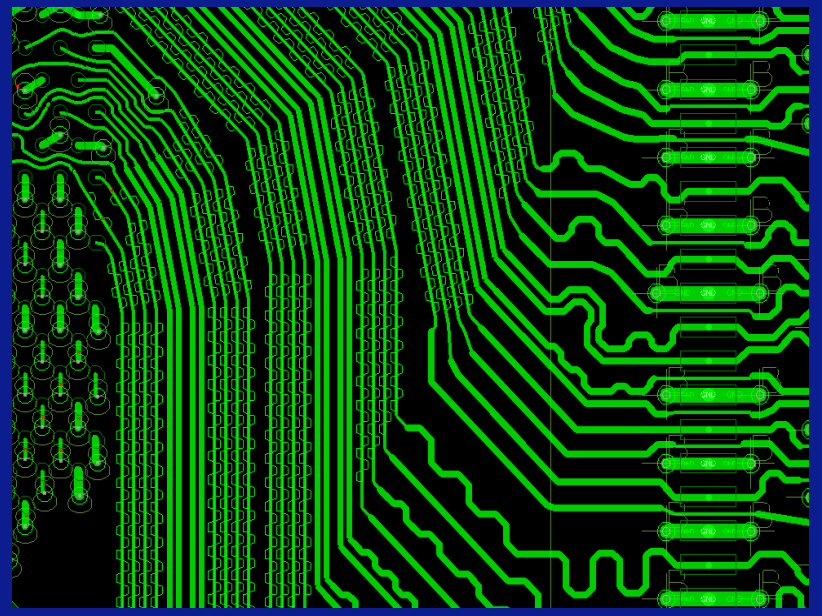
The Need for Crosstalk Reduction

- High capacity DDR5 platforms such as in data center and high-performance computing
- PCB board routing space is very limited and high-density routings are necessary
- Crosstalk is the bottleneck for DDR5
- Tabbed-line design is a promising enabler

DDR5 Reference Validation Platform

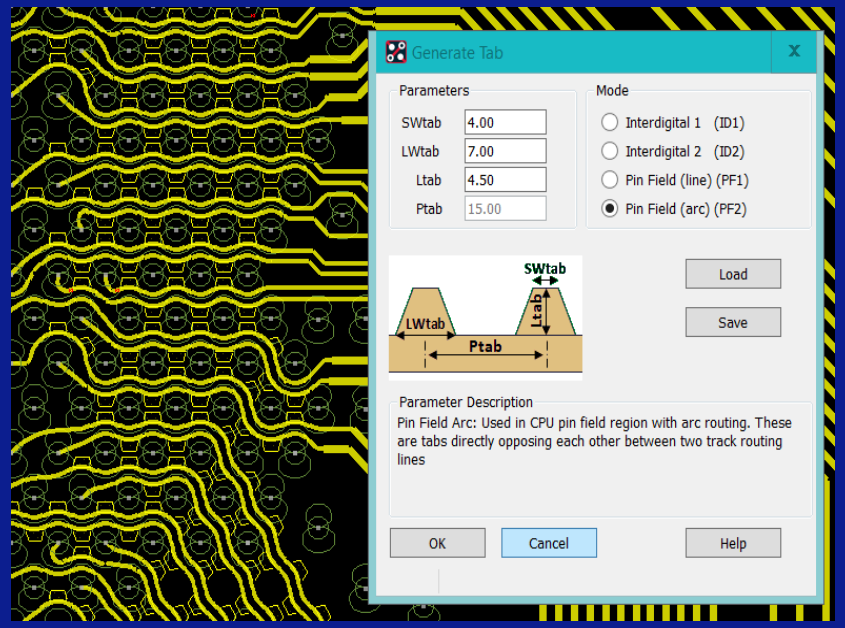


RVP board layout

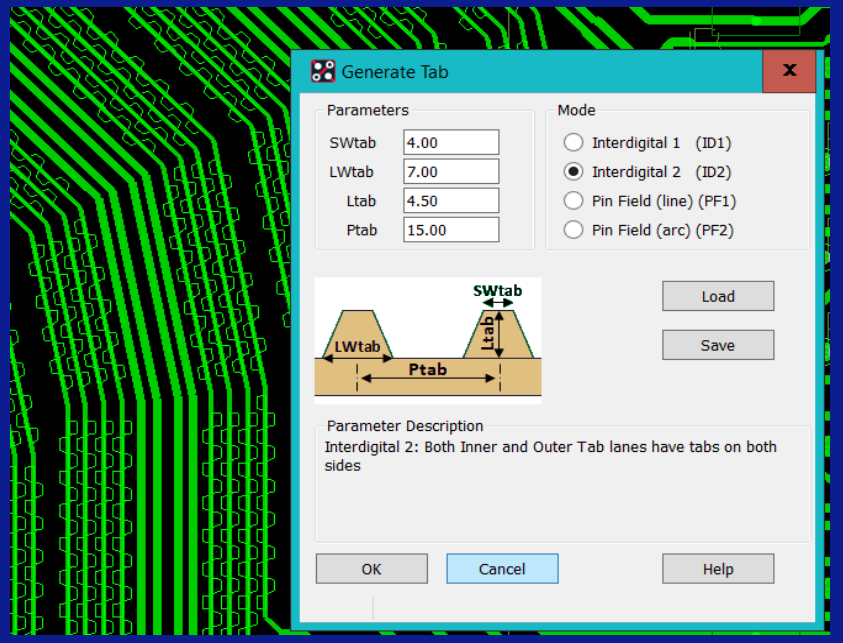


Tabbed lines routings

Tabbed Lines Routings Creation

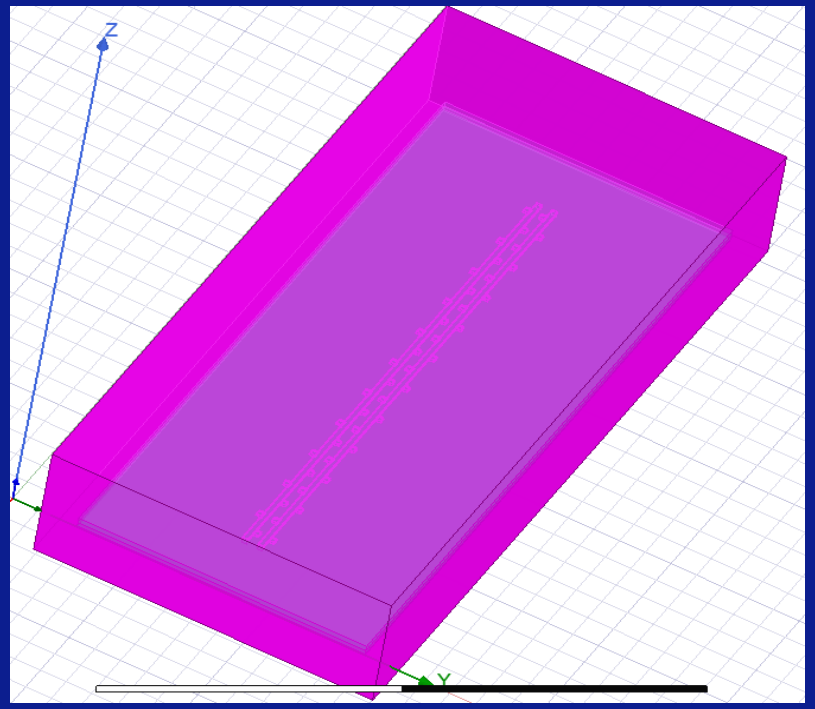


CPU pin field tabbed line routing

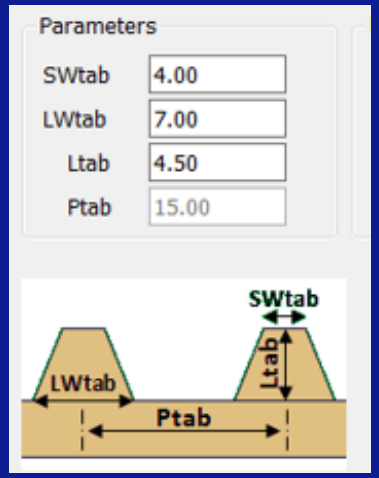


Main region tabbed line routing

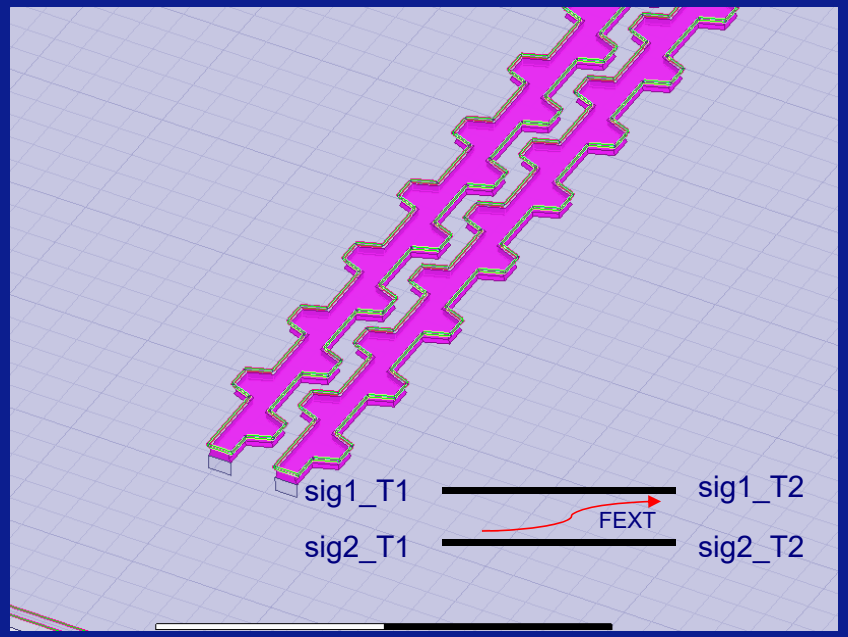
Tabbed Lines Crosstalk Optimization

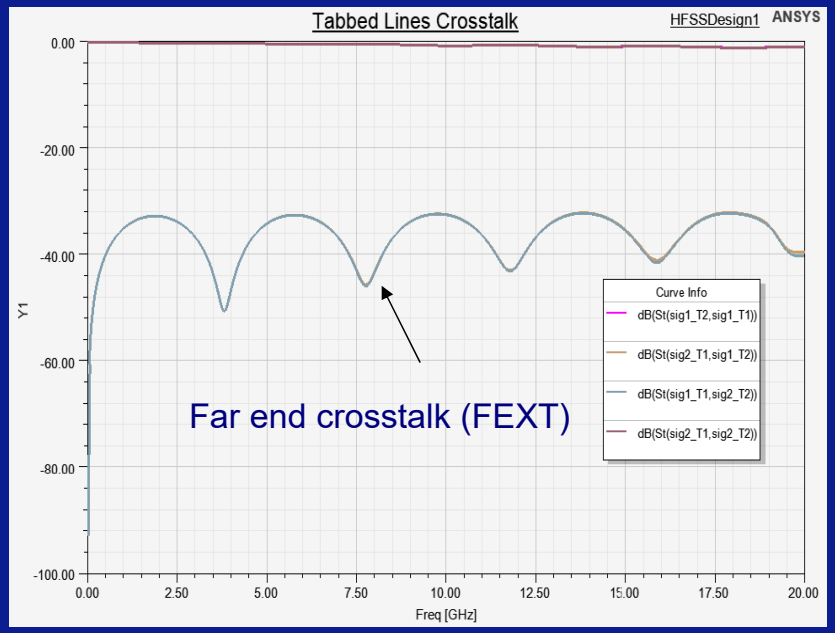


- Create 3D model
- Use 3D EM solver to generate S parameter
- Optimize following parameters to reduce coupling between two lines



Optimized Tabbed Lines Crosstalk Performance





Summary

- Deployment of new DDR5 memory systems requires rigorous and thorough testing
- Design of DDR5 validation platform is complex and challenging
- Advanced SI analyses guarantee platforms performance can meet design target
- Tabbed-line routings can reduce crosstalk and enable DDR5 in high density memory systems

References

[1] R Kunze et al., “Crosstalk Mitigation and Impedance Management Using Tabbed Lines,” Intel white paper, 2015.

Acknowledgments

The author would like to thank Virapandiane Ragavassamy and Kalpit Jha for the discussions

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