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Robust PCIe 5.0 Platform Design, Testing, and Analysis

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Agenda

- PCI Express (PCIe) 5.0 validation challenges
- Modular validation platform architecture
- Platform performance optimization strategies
- Compliance platform design and testing methodology
- Simulation and measurement data
- Summary

PCIe 5.0 Validation Challenges

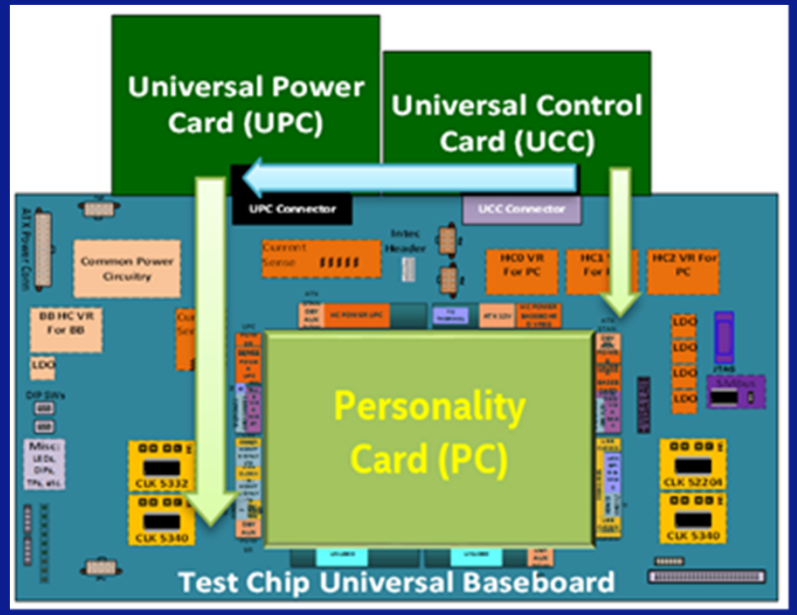
- Accelerated rate of standards development
- Shortened design and validation cycles
- Much higher data transfer rate at 32 GT/s
- Reduced link budget and margins
- Tremendous constraints on platform design

Modular Validation Platform Architecture

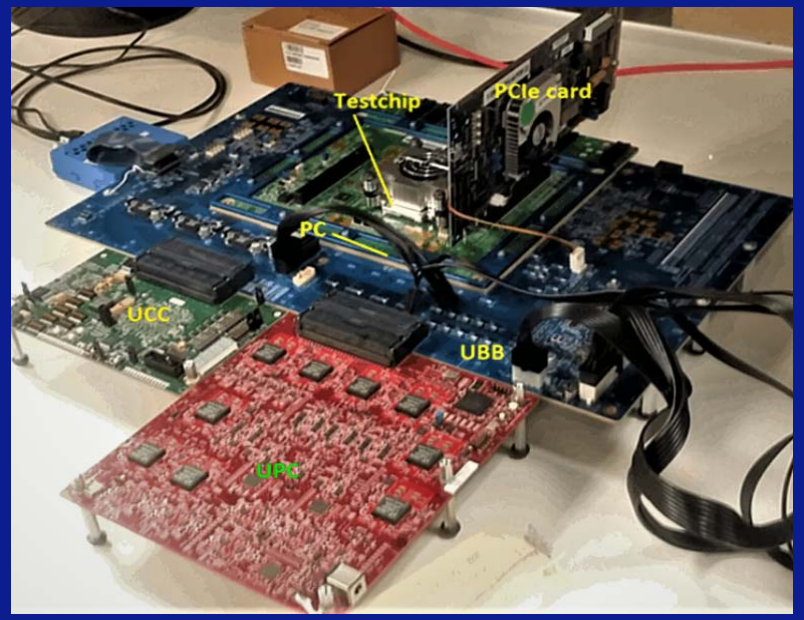
Modular platform components:

- Universal Baseboard (UBB)
- Universal Power Card (UPC)
- Universal Control Card (UCC)
- High Speed I/O Personality Card (PC)

Modular Validation Platform Architecture

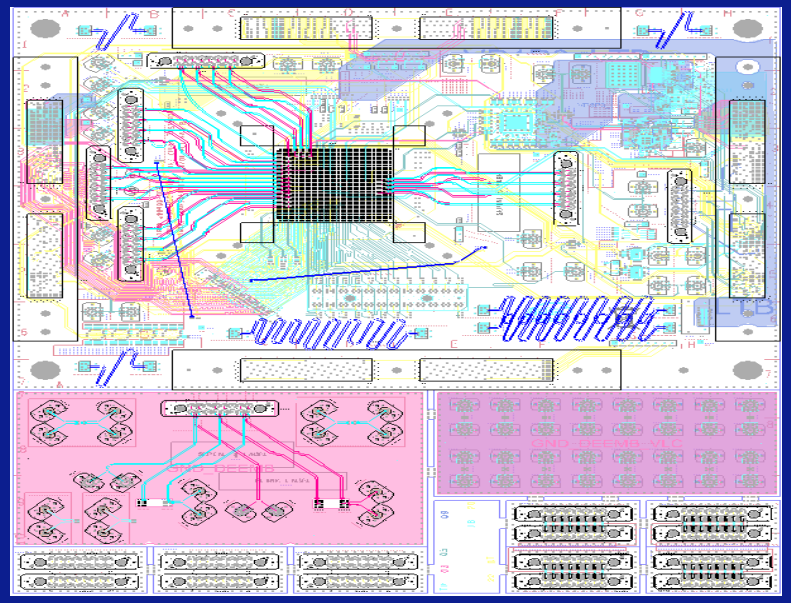


Platform architecture

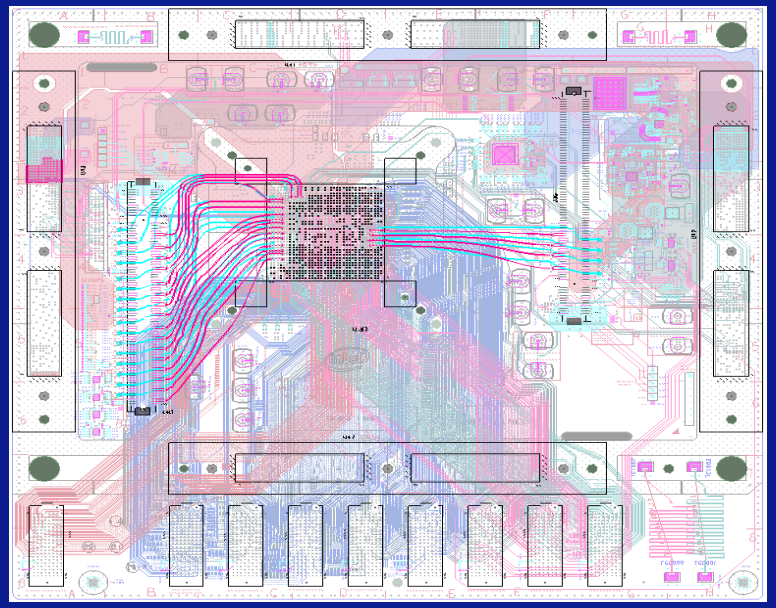


System setup

High Speed I/O Card Architecture

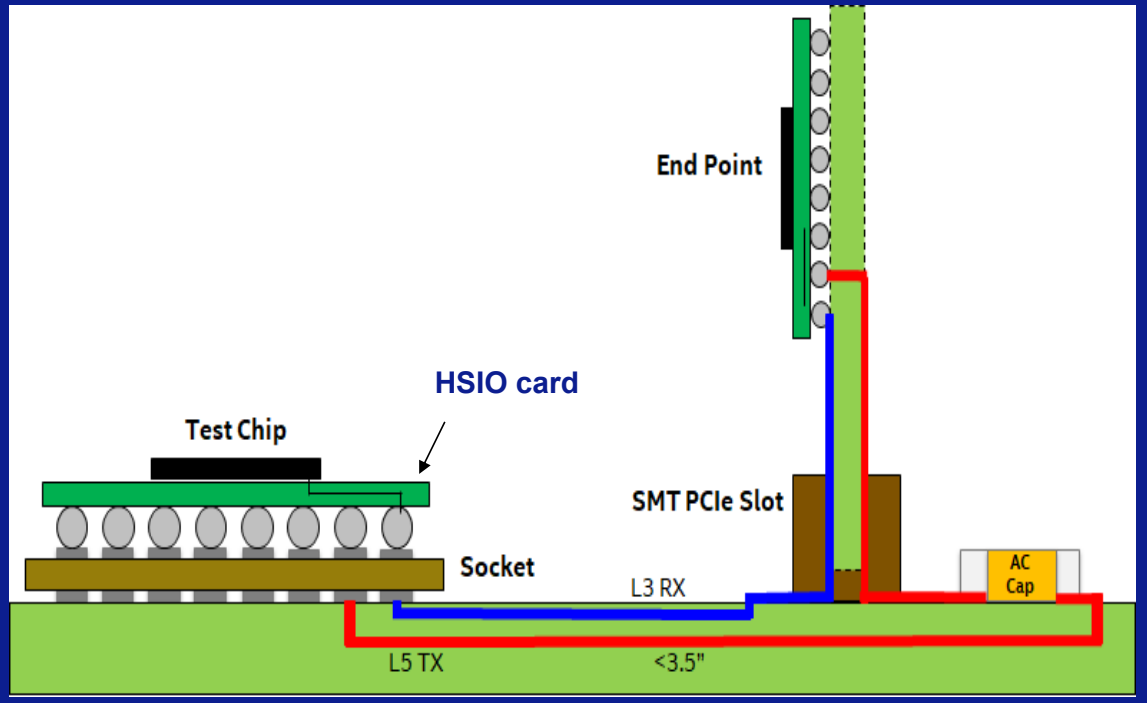


PCIe 5 EV (Electrical Validation) card layout



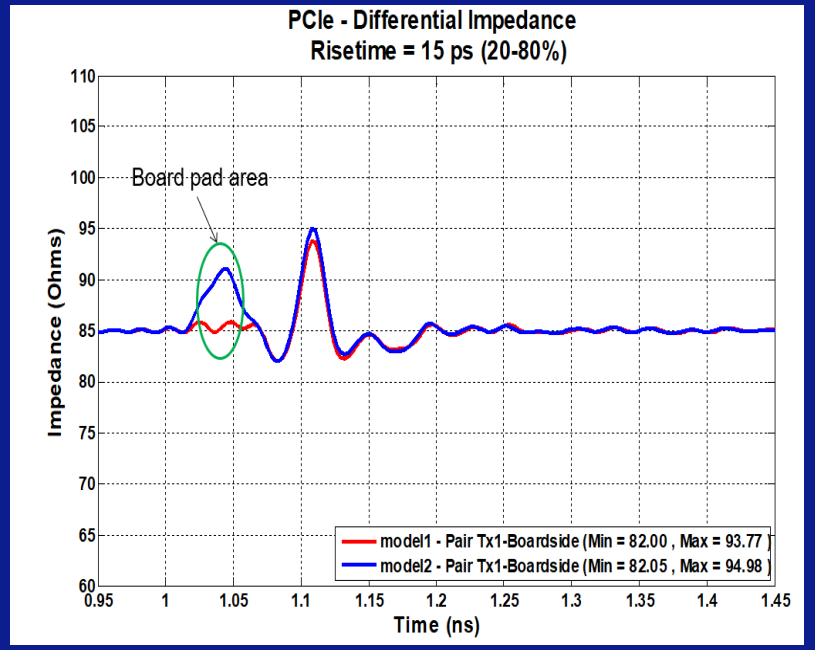
PCIe 5 FV (Functional Validation) card layout

High Speed I/O Card Usage Model

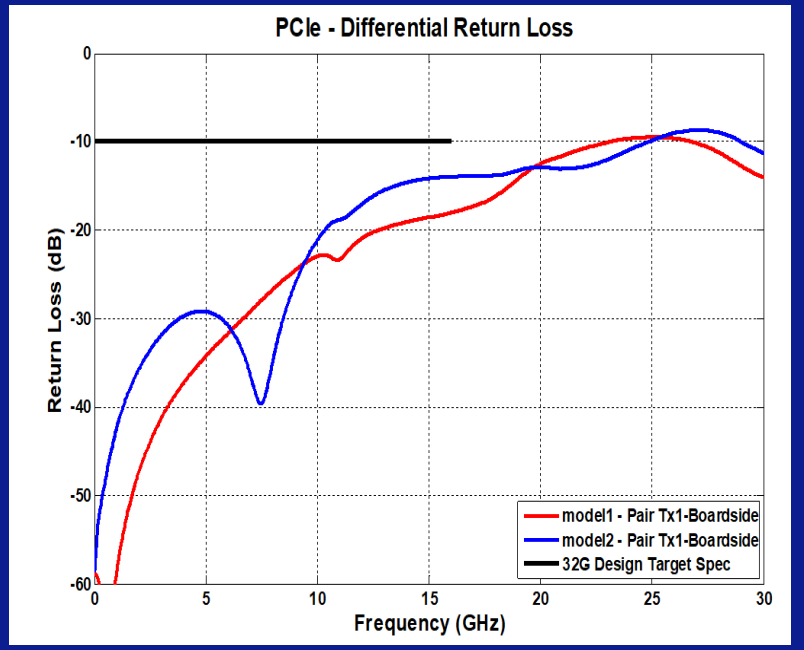


System margin validation using a plug-in card

PCIe 5 Connector Board Pad Stack Optimization

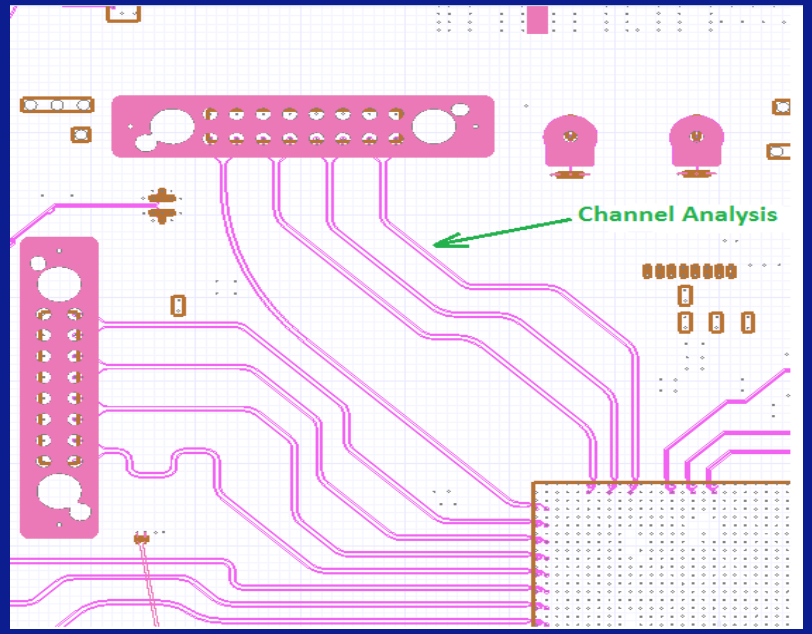


Impedance optimization

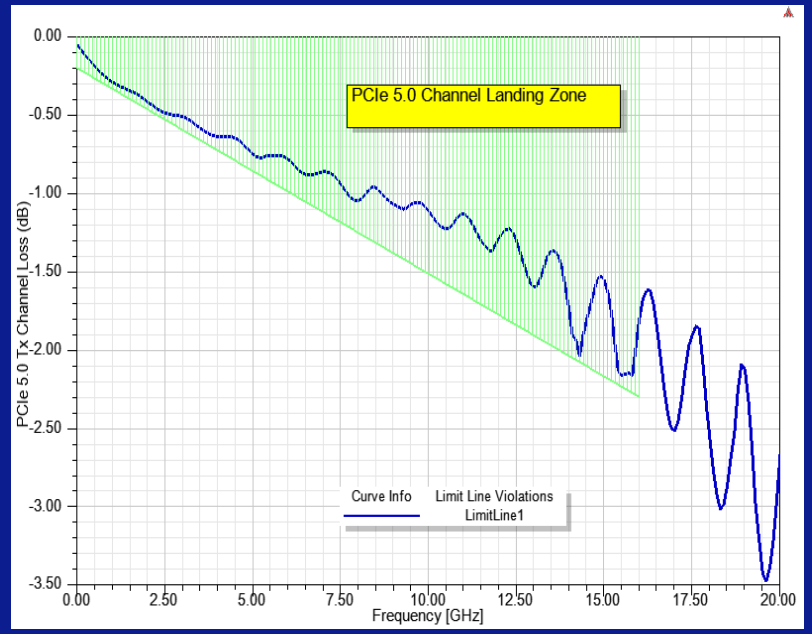


Return loss optimization

High Speed Channel Signal Integrity Analysis

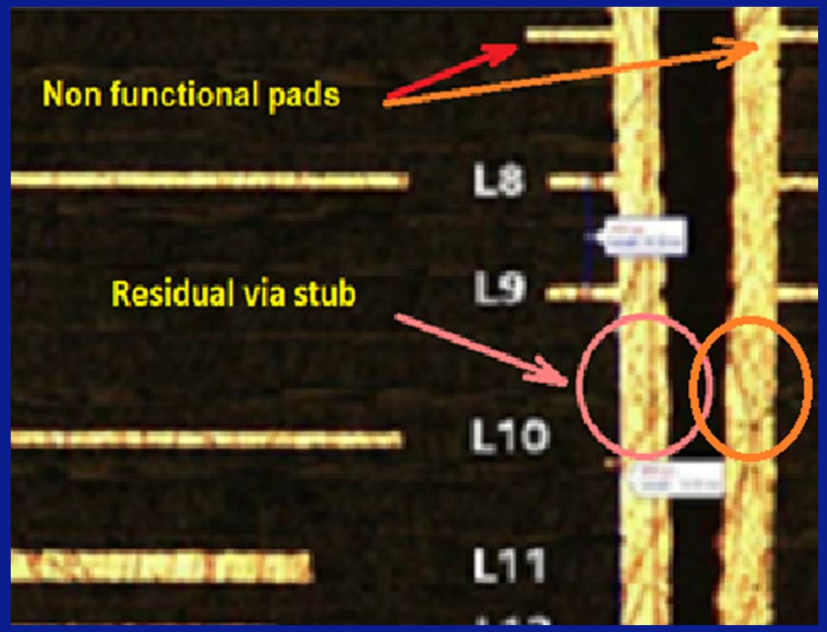


PCIe 5.0 Tx channels

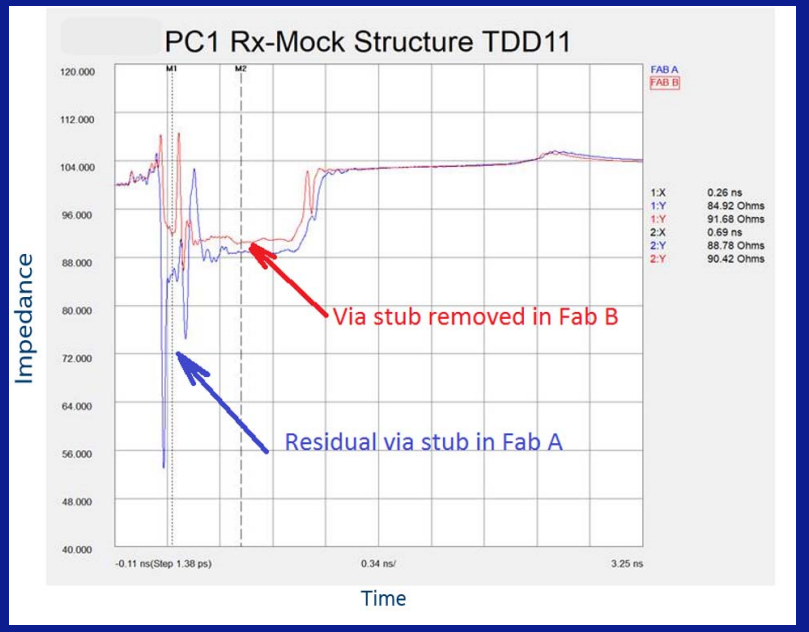


PCIe 5.0 Tx channel loss

Manufacturing Process Quality Control

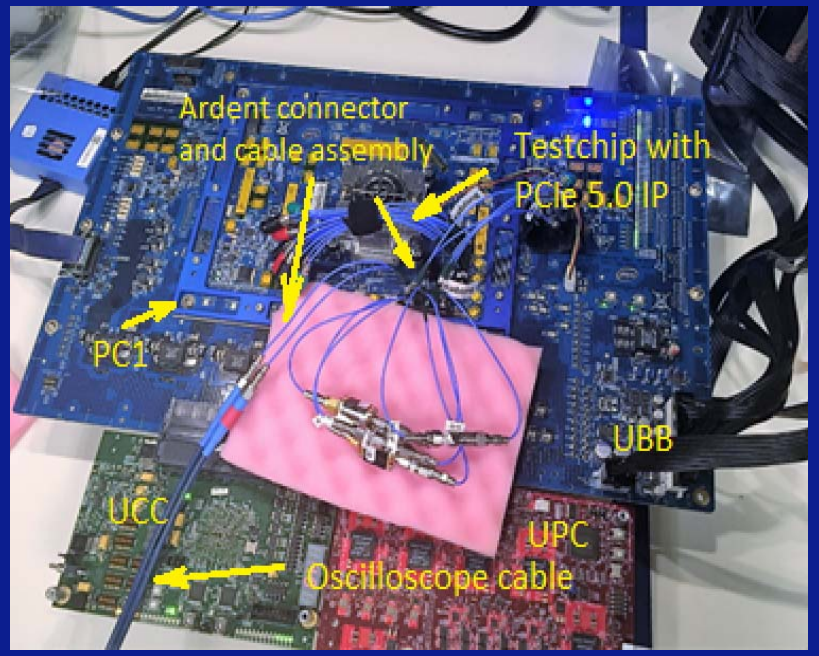


Via stub and non-functional pads

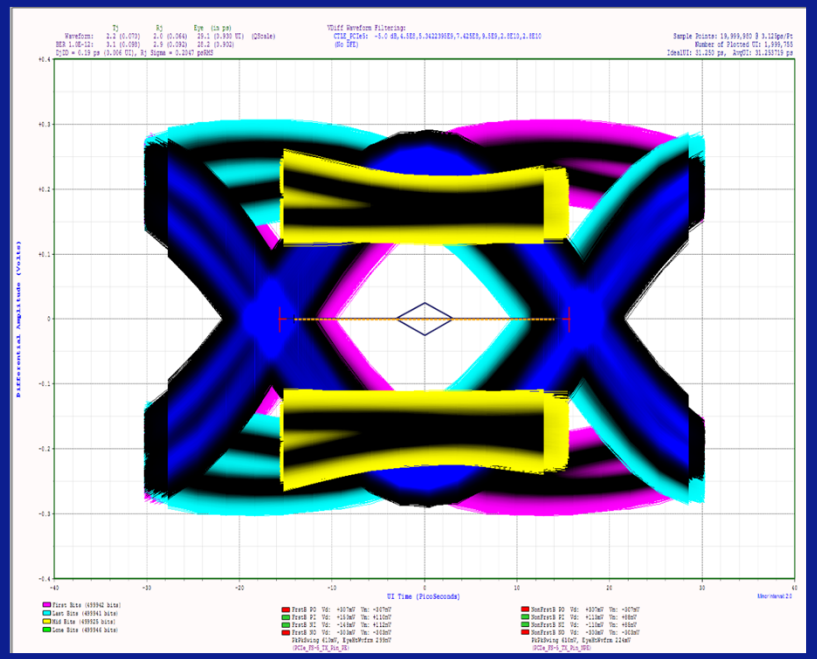


TDR impedance measurement

Testchip IPs Power-On Measurement Data



PCIe 5.0 validation system setup

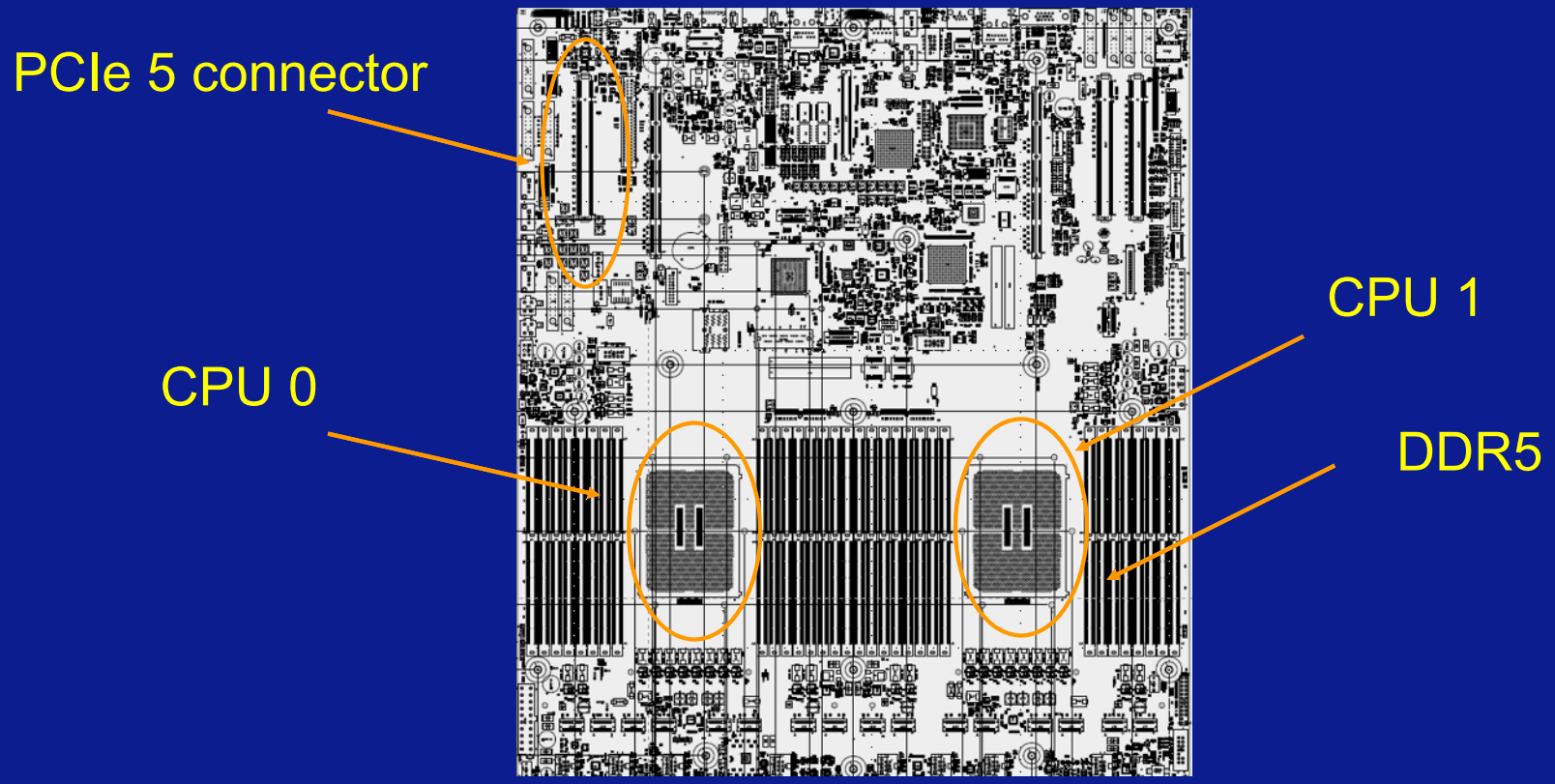


PCIe 5.0 Rx eye diagram

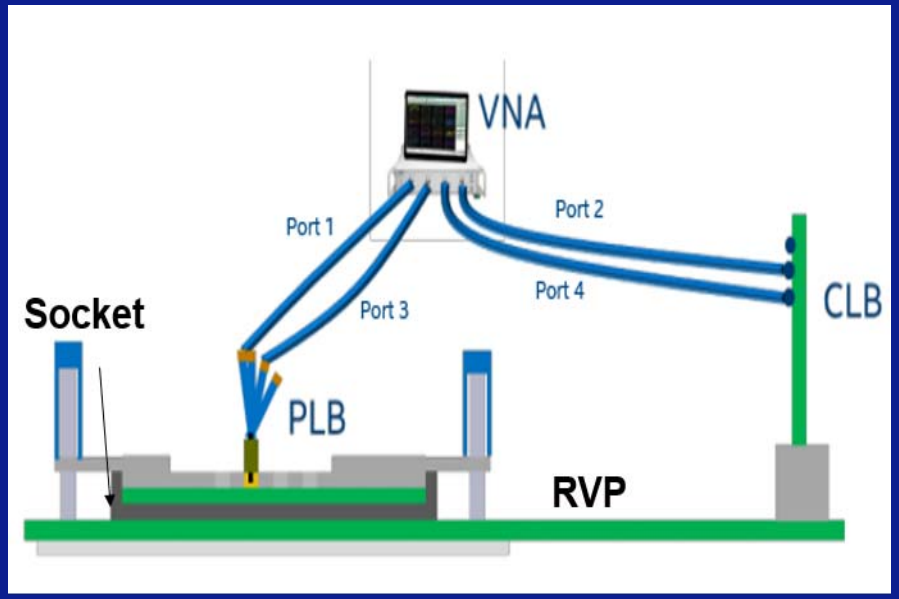
Compliance Testing Design and Implementation

- Design of a PCIe 5 reference validation platform (RVP)
- Development of compliance validation methodology
- Platform modeling and optimization
- Lab measurement
- Simulation, correlation and performance improvements

PCIe 5 Reference Validation Platform Design

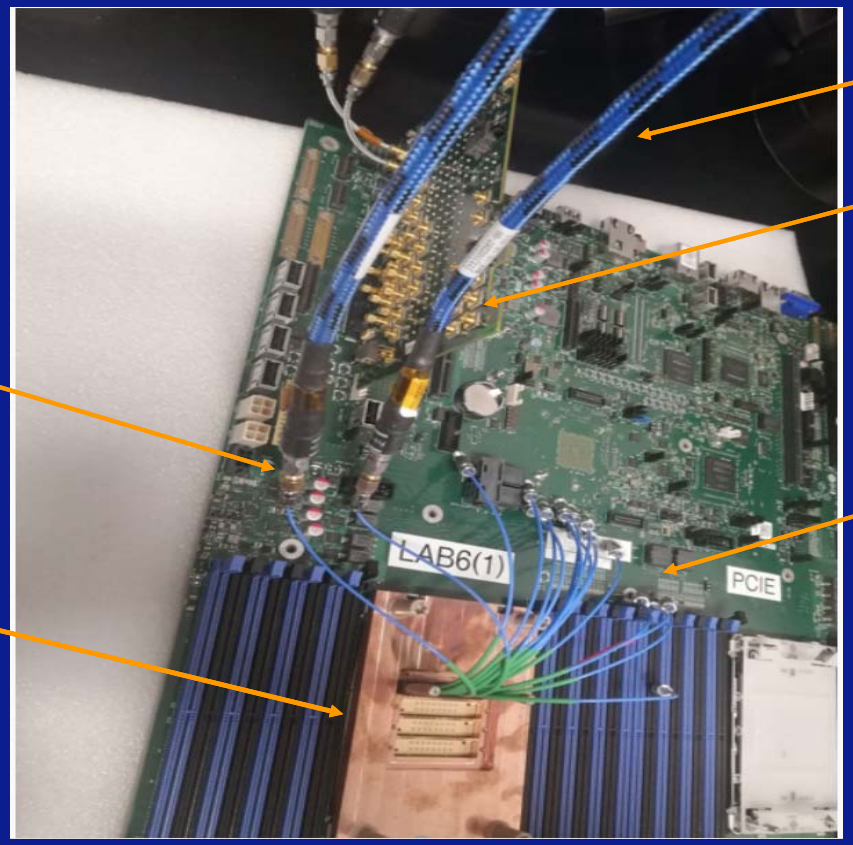


PCIe 5 Full Channel Measurement Configuration

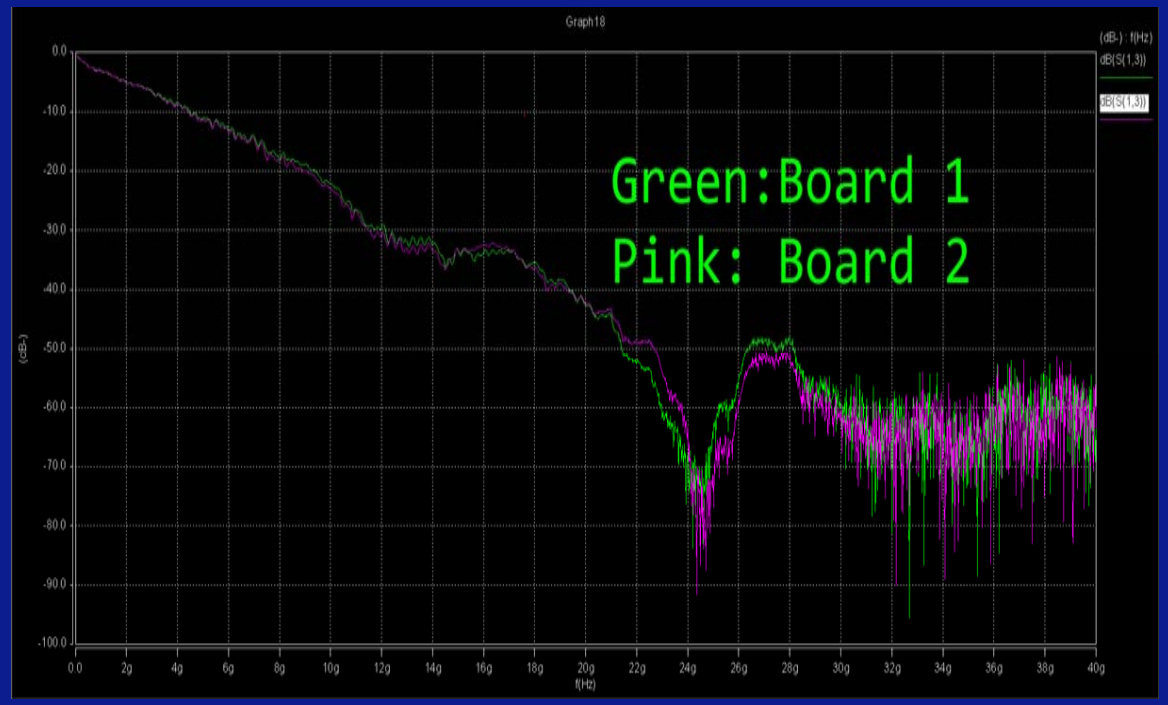


PLB: PCIe loading board
CLB: compliance loading board
RVP: reference validation platform
VNA: vector network analyzer

Lab Measurement Setup

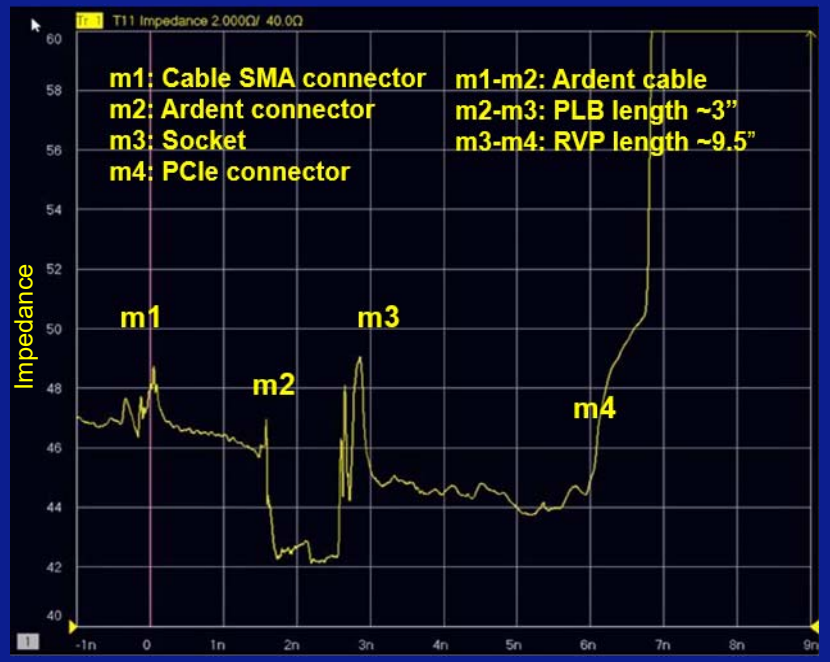


Frequency Domain Measurement Data

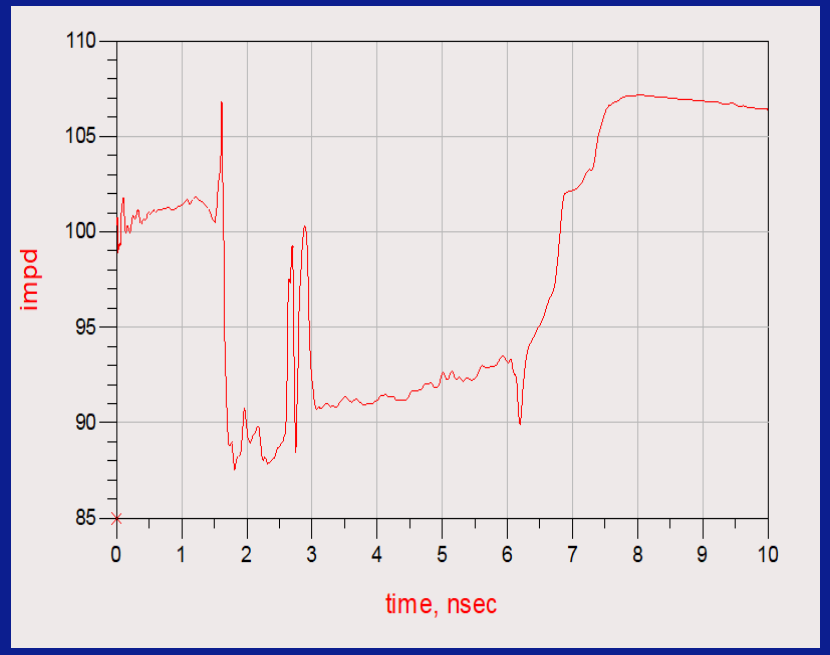


Two boards show reasonably close performance

Time Domain Measurement

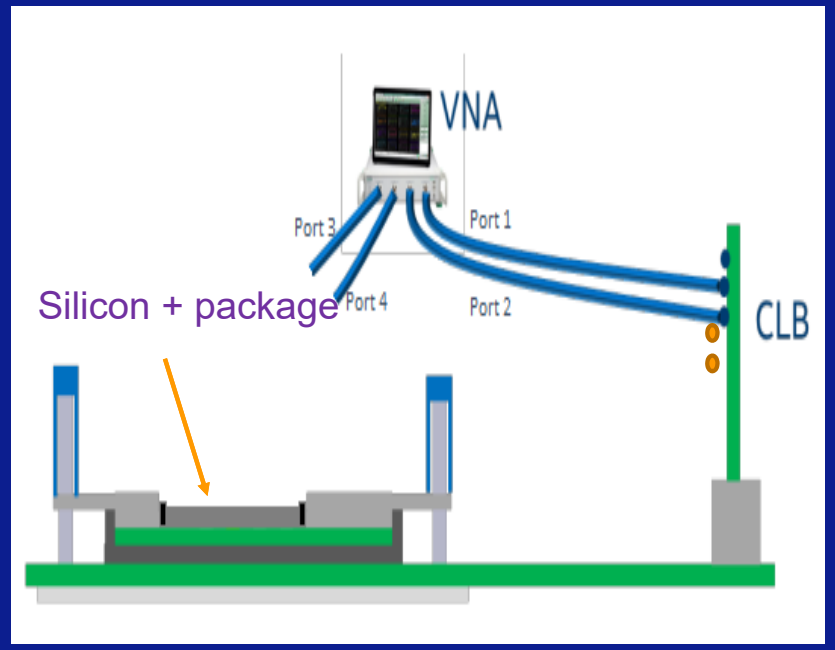


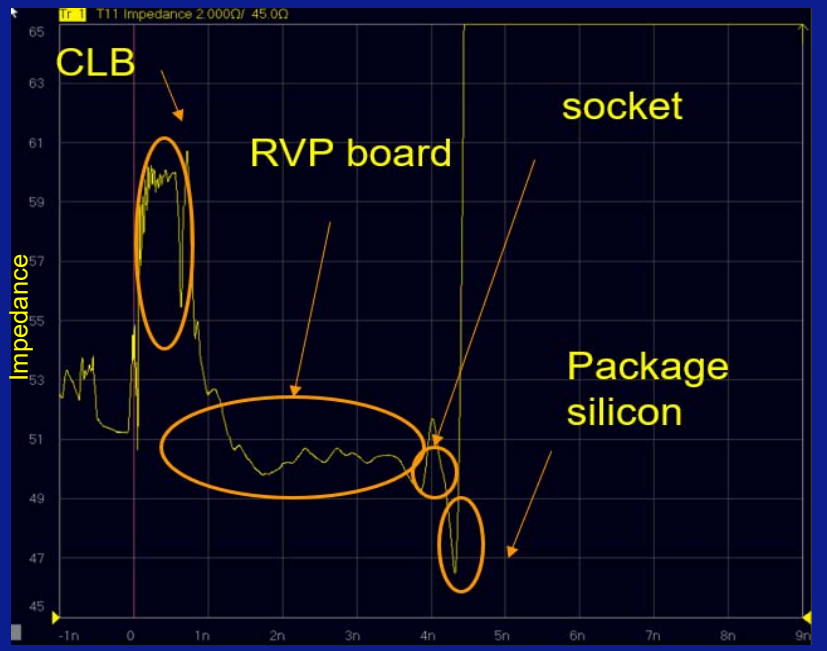
Single Ended TDR (from CPU)



Differential TDR (simulation)

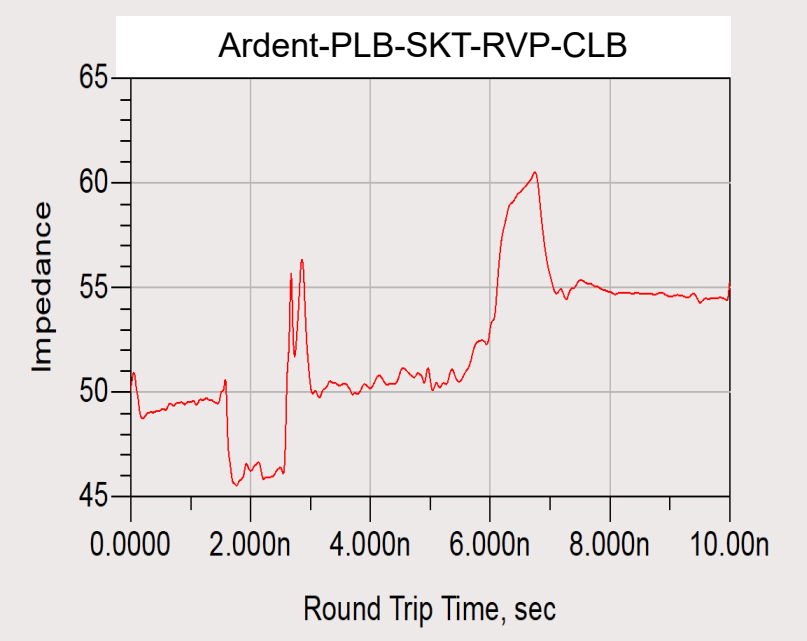
Time Domain Measurement



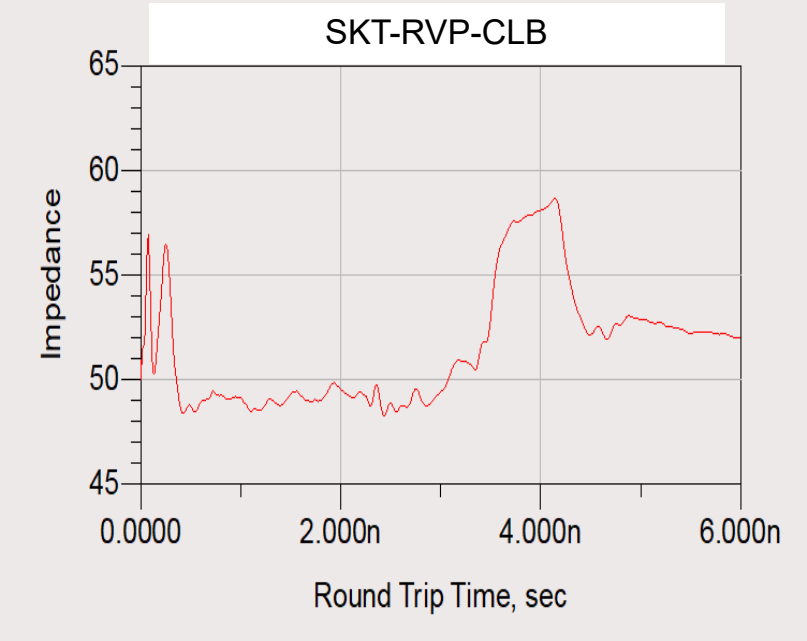


Single Ended TDR (from CLB)

TDR Impedance Before and After De-embedding



TDR before de-embedding



TDR after de-embedding

Summary

- PCIe 5.0 platform design is complex and challenging
- SI analysis and channel optimization are critical to achieve high performance
- Rigorous manufacturing process control guarantees platforms are of high quality
- Lab measurement and simulation correlation ensure design consistency

Acknowledgments

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