Demonstrating High-Speed 28 Gbaud PAM4 Wafer Probe Production Testing Capabilities

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Contents

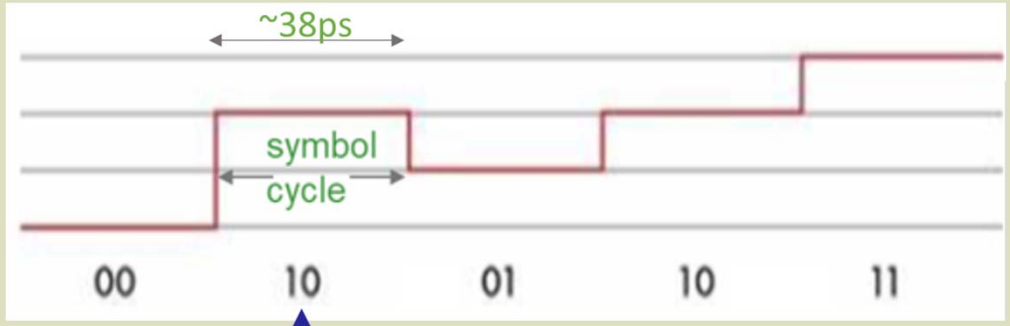
- The need for High-Speed I/O testing
- High-Speed I/O testing strategy
- Solution Elements
- Measurements
- Discussing the results
- Summary

What We Will Be Showing Today

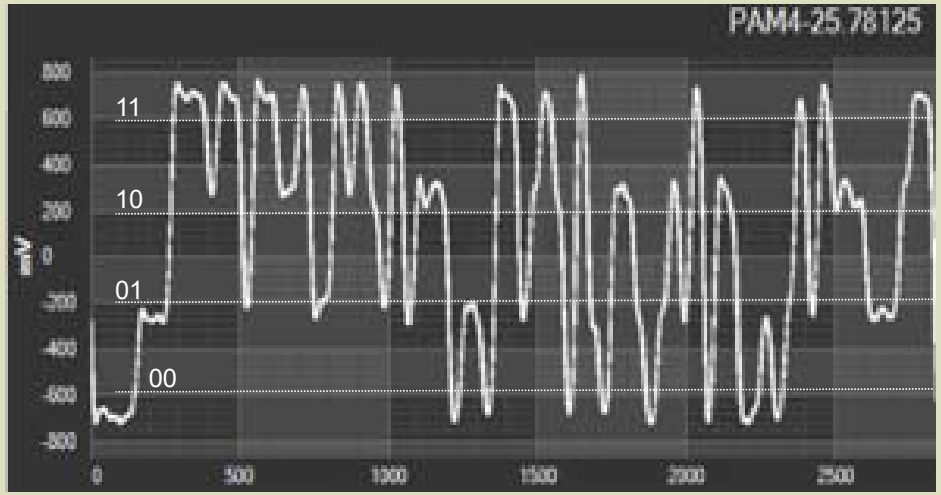
- High-Speed Production Testing Solution
  - Wafer Probe Measurement Results at 26.5625 Gbaud PAM4
    - 26.5625 Gbaud is a Gigabit Ethernet data rate used in 200GbE and 400GbE data center systems
- Solution Elements
  - Advantest V93000 Tester
  - MultiLane High-Speed BERT and Scope
  - Technoprobe Wafer Probing Technology

PAM4 Explained

26.5625 Gbaud PAM4 is ~52 Gbps

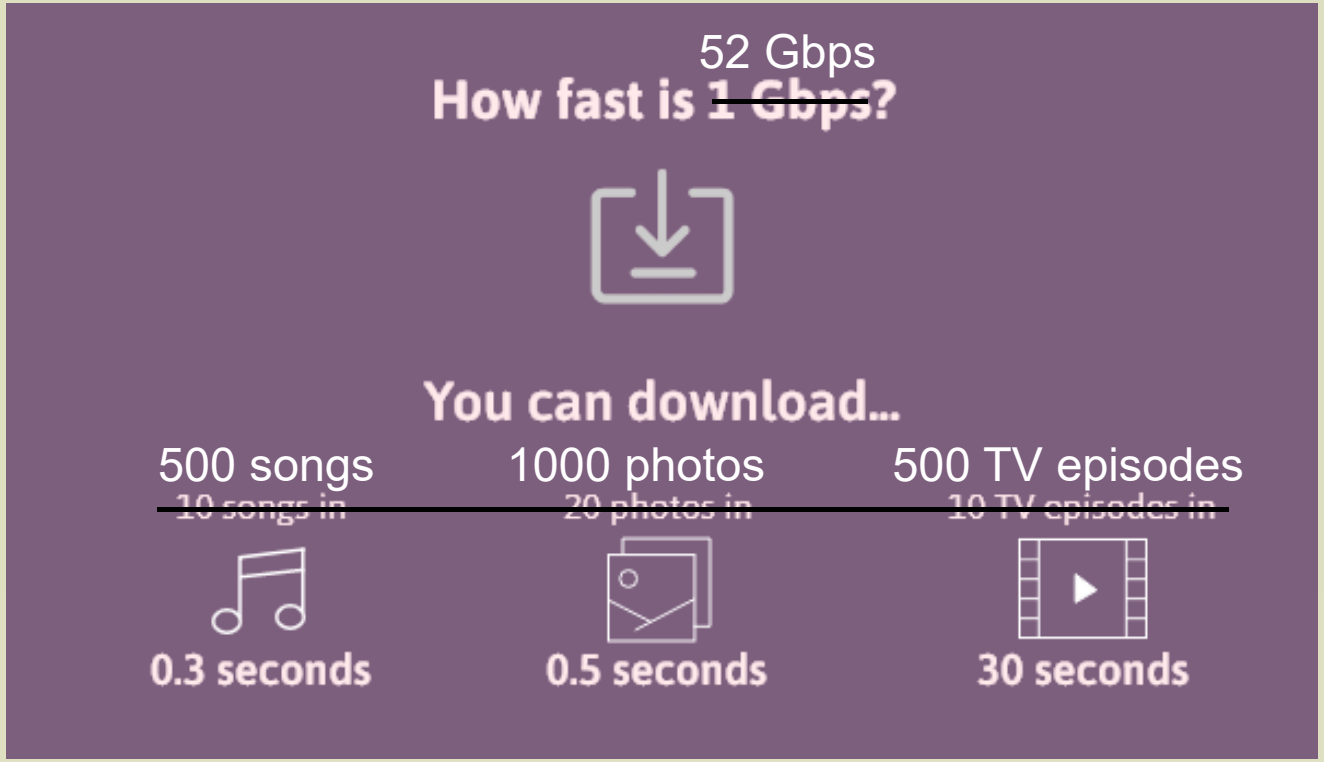


PAM4
2 bits per
symbol



Modulation	Data Rate	Symbol Rate	Nyquist
PAM4	50 Gbps	25 GBd	12.5 GHz
NRZ	50 Gbps	50 GBd	25 GHz

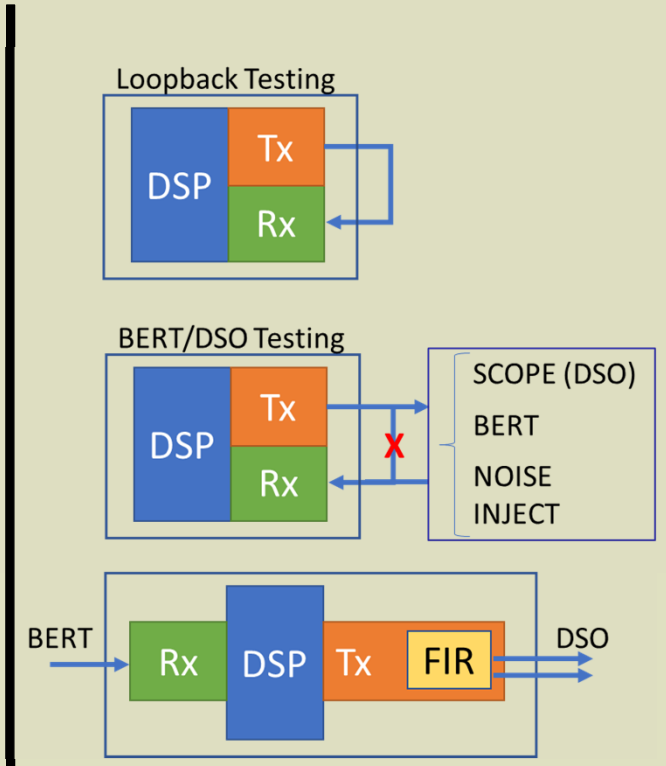
How fast is 52 Gbps?



Source: Aeri Gee, What Is 1 Gbps? - InMyArea.com

Why Are Companies Doing High-Speed Probe Testing

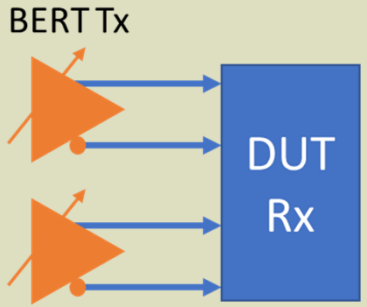
- Loopback testing is not always possible
  - Eg, Transimpedance Amplifiers (TIA), USB4, etc
- Loopback testing requires increasingly sophisticated BIST engines and may not cover all desired specs
- Customer may prefer a single calibrated measurement reference for quality purposes, rather than each DUT testing itself
- Wafer die are being attached directly to sophisticated multichip modules (MCM) , bypassing a testable packaged medium for high-speed tests



DUT Input/Output High-Speed Tests

From BERTs to DUT Rx

	Test Requirement	Feature
Voltage	Clean low-level signals at the DUT input	Adjustable eye parameters to worst-case test receiver
Timing	Frequency & phase offset as well as jitter	Independent real-world timing system with jitter injection
Signal Integrity	Worst-case signal	Realistic end-of cable signals can be delivered by ML BERT Tx
Error Correction	Error detection & correction circuitry	ML BERT can inject errors into PRBS data stream



TestConX™

High-Speed 28 Gbaud PAM4 Wafer Probe

7

2022

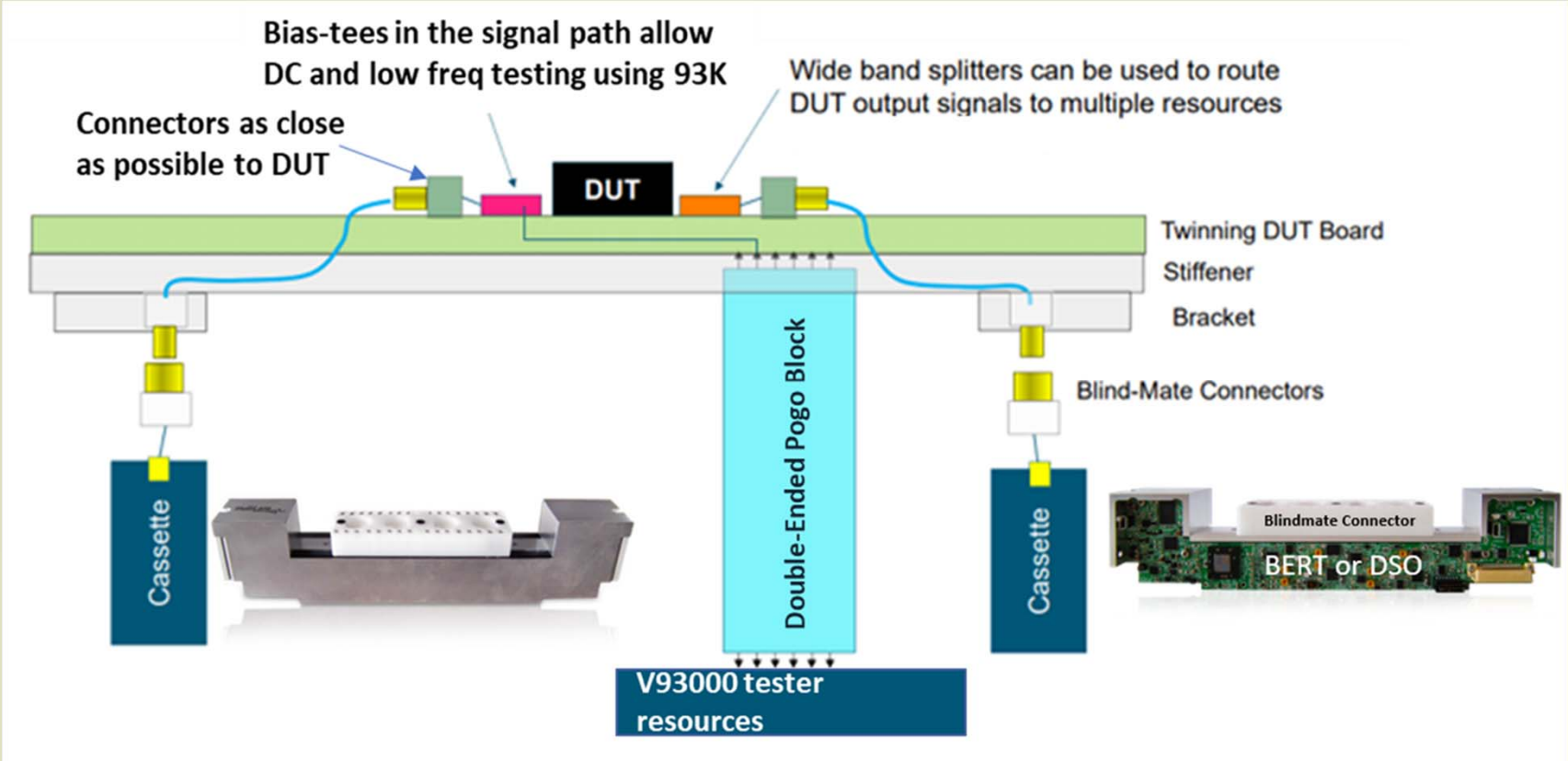
DUT Input/Output High-Speed Tests

From DUT Tx to DSO or BERT Rx

	Test Requirement	Feature
Voltage	DUT driver rise/fall times and amplitudes	10mVpp DSO input sensitivity
Timing	DUT Eye width and jitter at DUT output	Calibrated/traceable clocks & 200fs intrinsic jitter
Signal Integrity	Compensation controls work as designed	Visible impact. DSP in DSO can simulate end-use cable and confirm end-of-line eye characteristics.

Available HSIO Measurements	
▪ Eye Mask ▪ Eye Amplitude ▪ Eye Height ▪ Eight Width ▪ Jitter ▪ Noise	▪ SNR ▪ BER ▪ Extinction Ratio ▪ Vertical Eye Closure (VEC) ▪ Rise Time ▪ Fall time

High-Speed Testing Topology

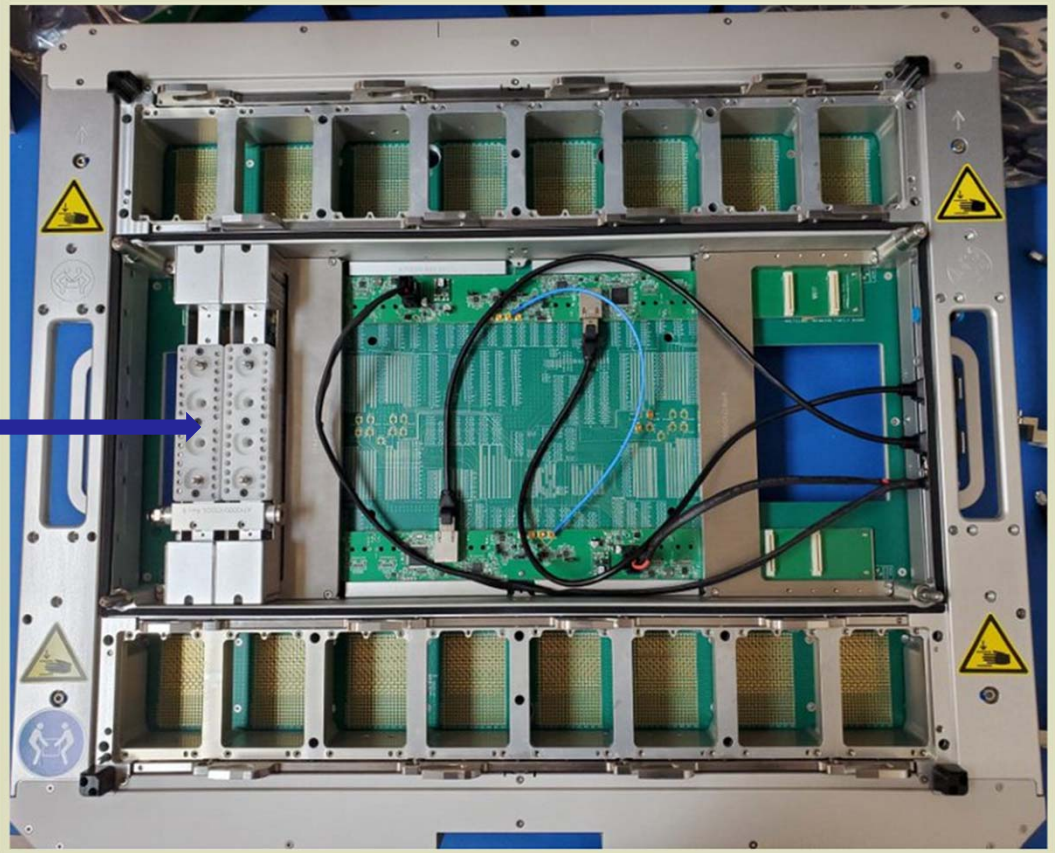


High-Speed Twinning Frame

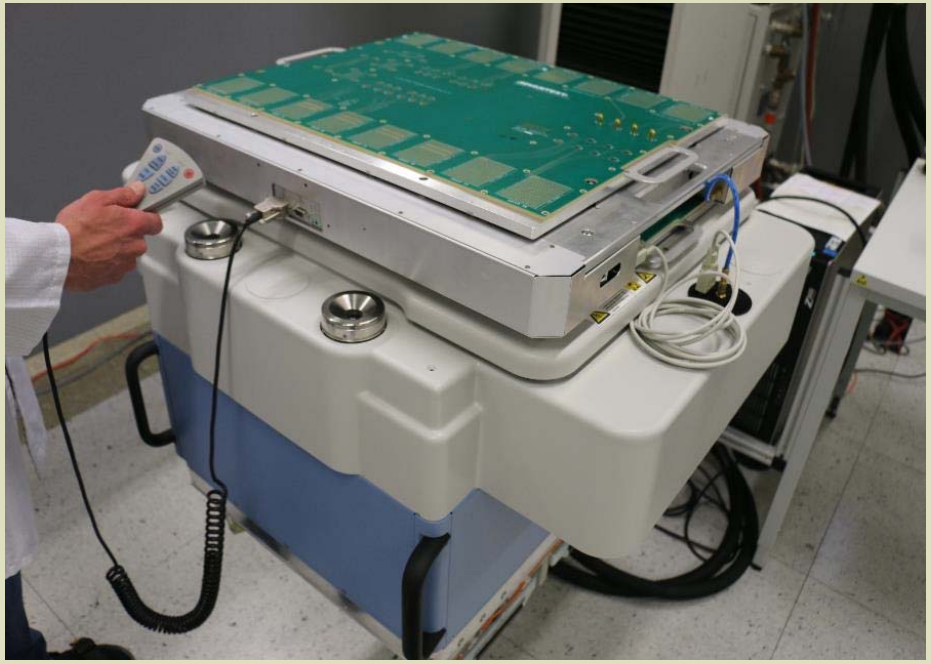
Twinning Frame – Top View

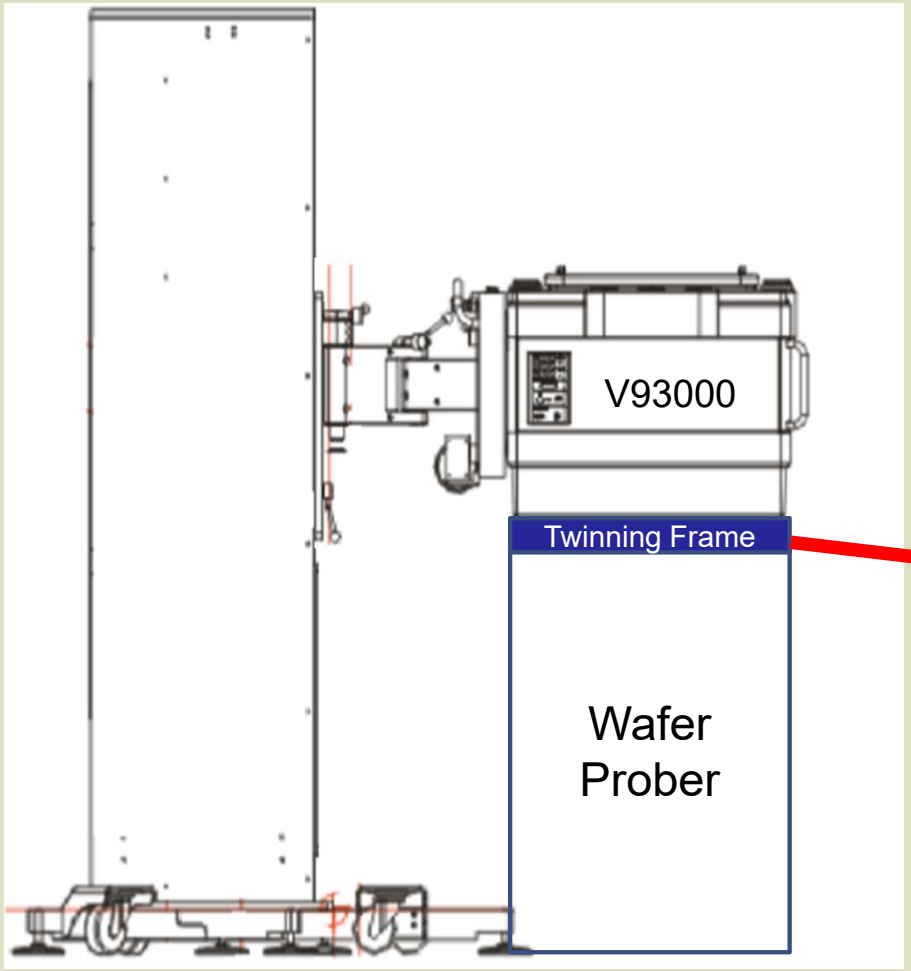
4-Lane BERTS
28/56 GBd
PAM4/NRZ

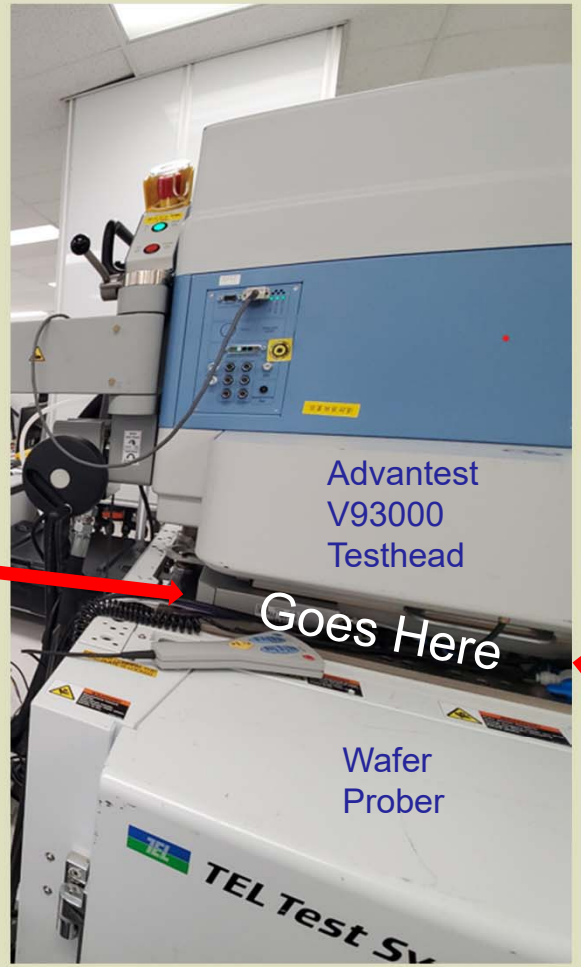
4-CH DSO
50GHz IBW



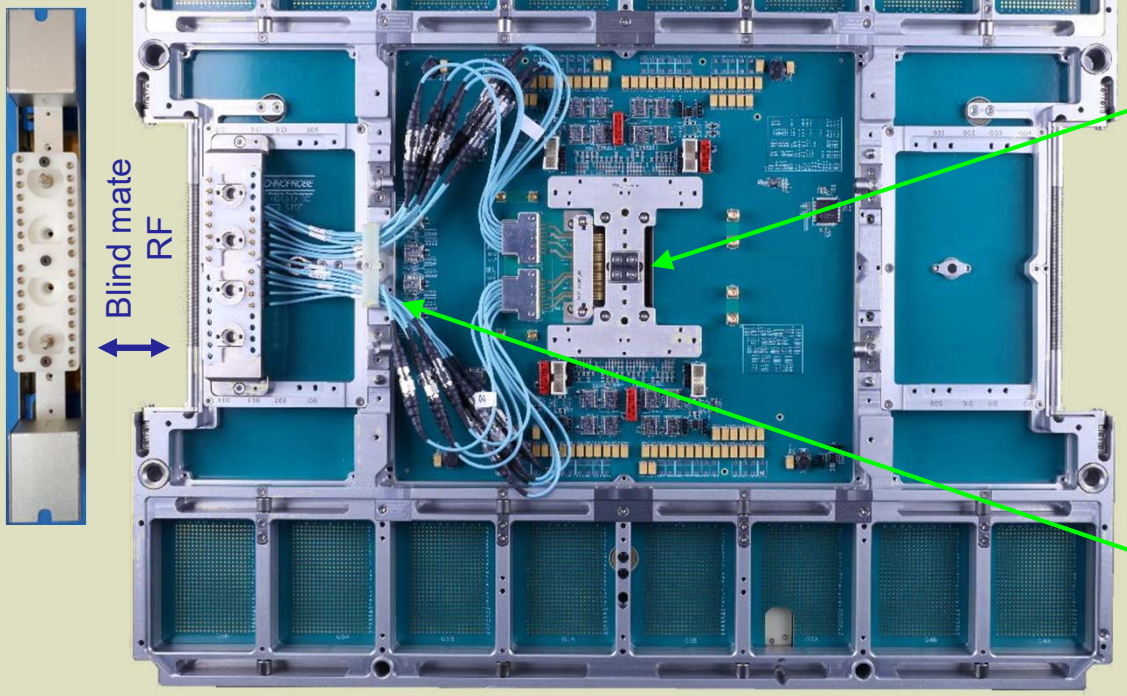
Twinning Frame Docked to V93000 CTH




V93000
Twinning Frame
Wafer
Prober


Advantest
V93000
Testhead
Goes Here
Wafer
Prober
TEL

DUT Wafer Sort Loadboard – Tester Side

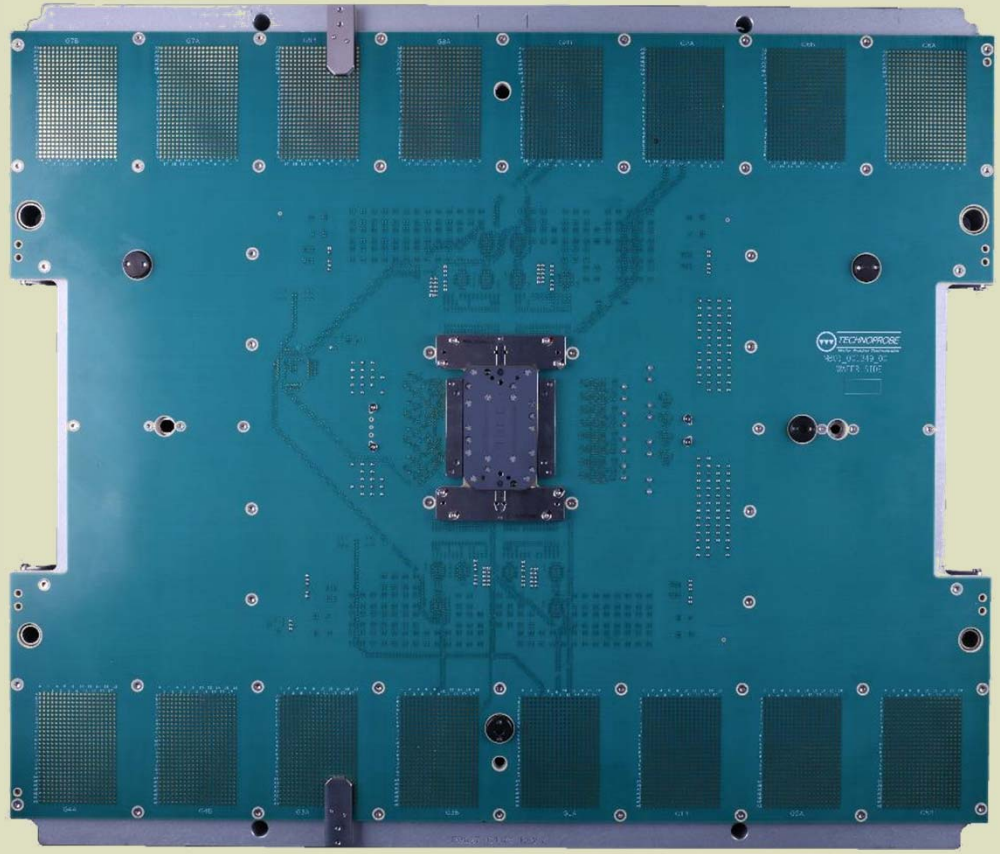


TECHNOPROBE
Wafer Probing Technologies

Solutions

- The larger application space in the twinning version of the V93000 makes the interface to the bridge beam even more important.
- Right angle, multi-coax cables with SMPM blind mate connectors for signal fidelity, signal density, blind mate, and limited height.
- Custom brackets to route cables to the MultiLane instruments without interfering in the direct docking

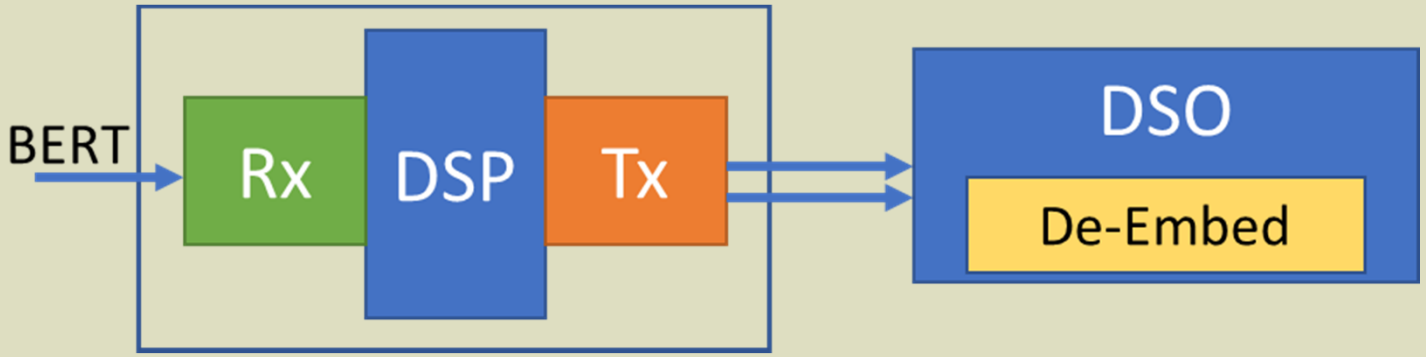
DUT Wafer Sort Loadboard – Wafer Side



TECHNOPROBE
Wafer Probing Technologies

Probe Card

- Phantom is a hybrid probe head architecture with replaceable needles
  - TPEG™ MEMS needles
  - RF space transformer
- Capable of probing larger arrays and multi-sites
- Fine pitch capability: 130 µm bump arrays and 70 µm peripheral pads
- Target markets
  - 28 and 56 Gbps for PAM-4 DSP, 400 gigabit Ethernet, TIA, and laser drivers
  - 28 and 39 GHz for 5G
  - 60 GHz for 802.11ad and 5G

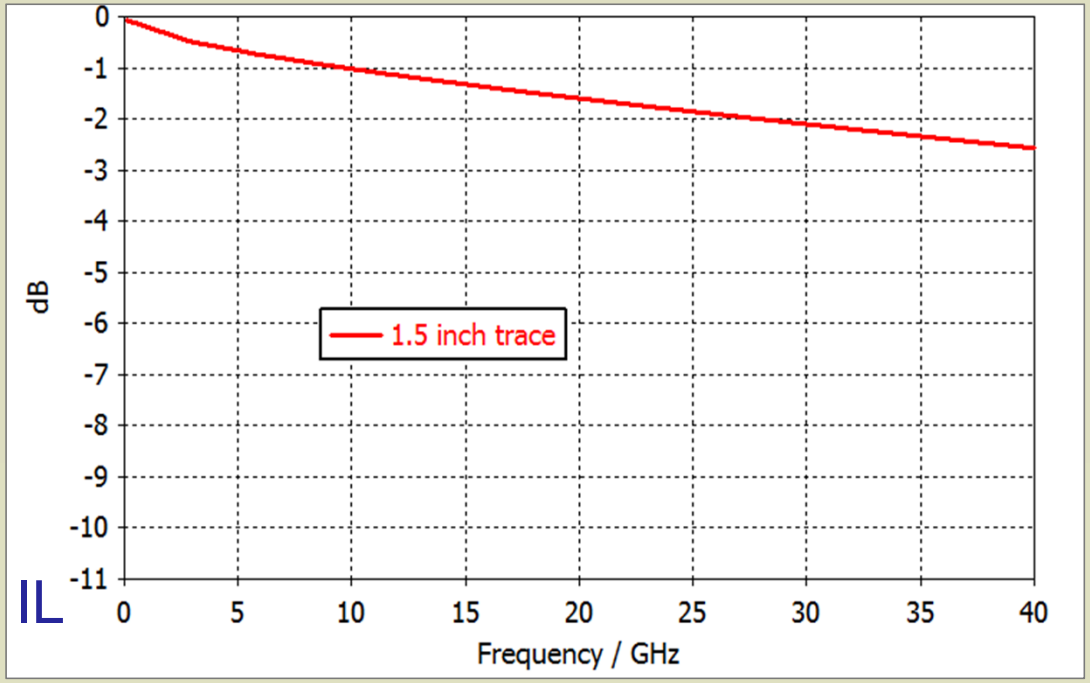


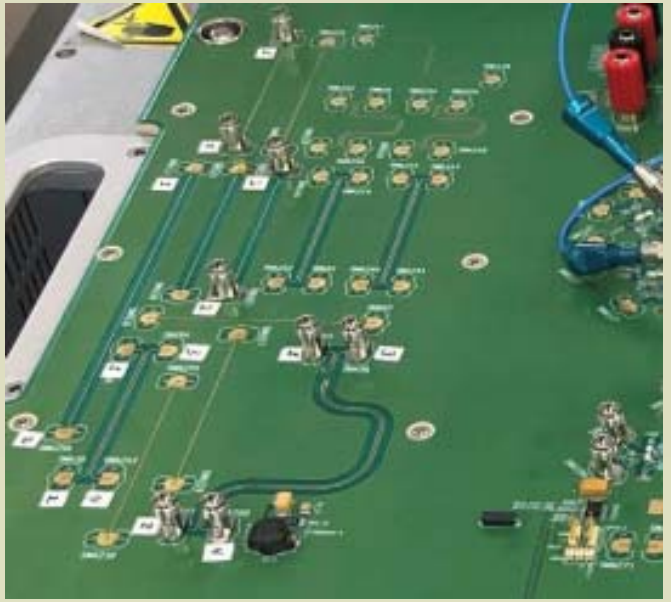
DUT LTX 26.5625 GBAUD PAM4

DSO DE-EMBEDDING OPTION

Signal Path Correction (De-embedding)

Example: Load board 1.5” trace from DUT to HS connector





Signal Path De-embedding

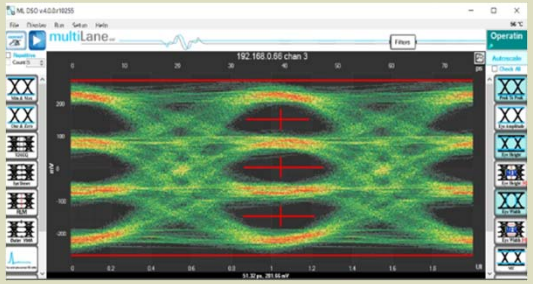
DSO

Traces, Vias,
Cables, Connectors

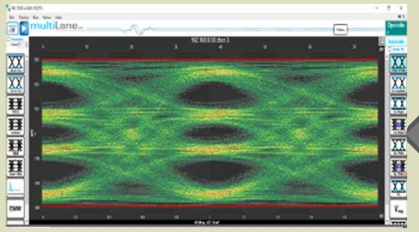
DUT

Wafer Probes

DUT Eye Output

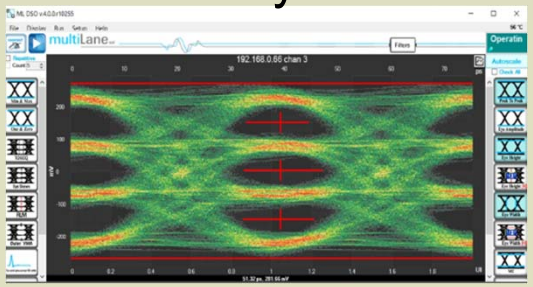


Unbalanced Eyes Due To Signal Path Distortion

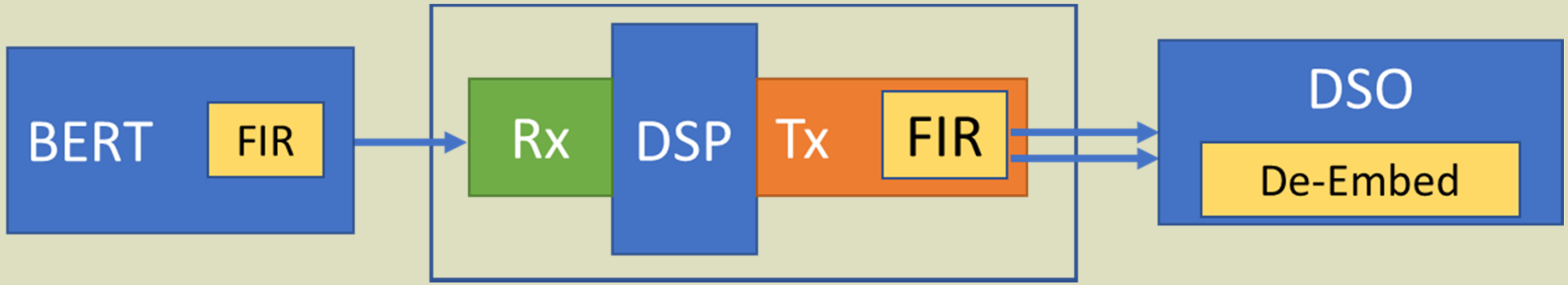


DSO Signal Path De-embedding

Balanced Eye Reconstruction

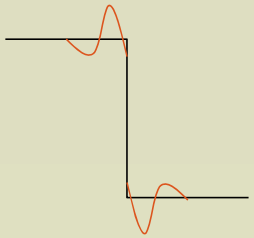


TestConX™



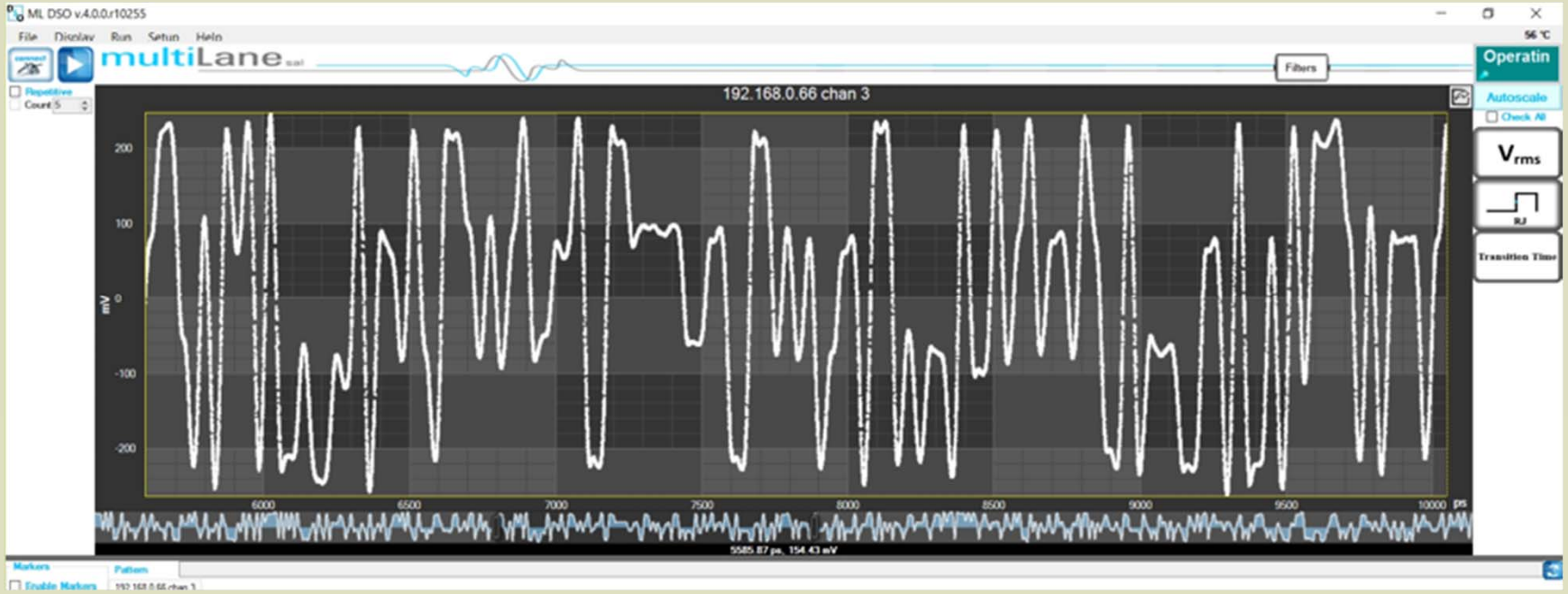
DUT LTX 26.5625 GBAUD PAM4

TRANSMIT FIR OPTION



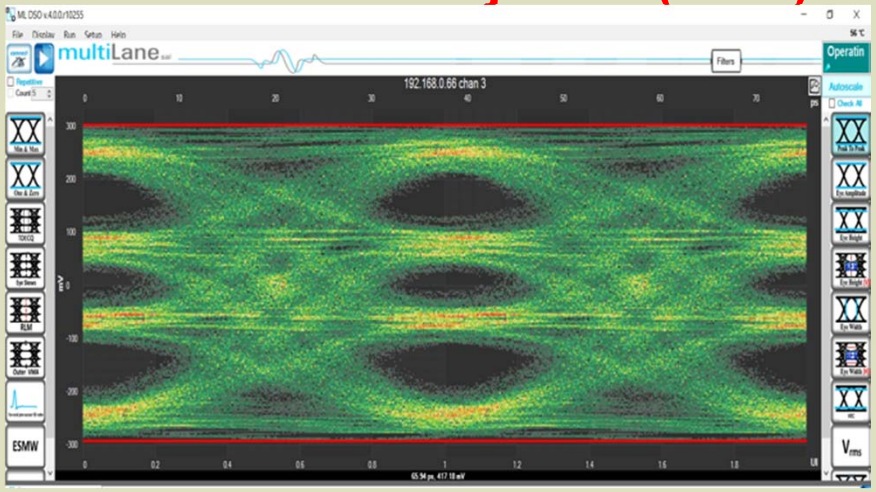
DSO Capture using DUT LTX 3-tap FIR

26.5625 GBd PAM4 Pattern Capture

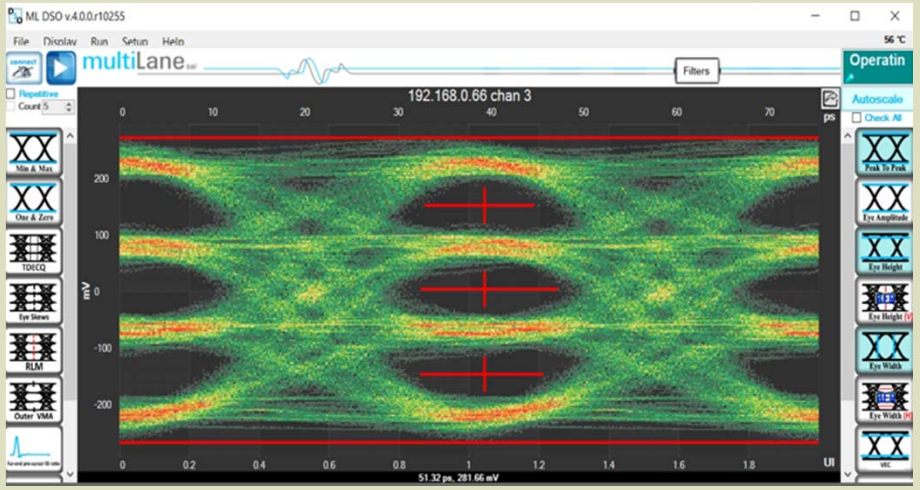


DSO Capture using DUT LTX 3-tap FIR

26.5625 GBd PAM4
Eye Measurement (No Correction)
DUT would be rejected (FAIL)

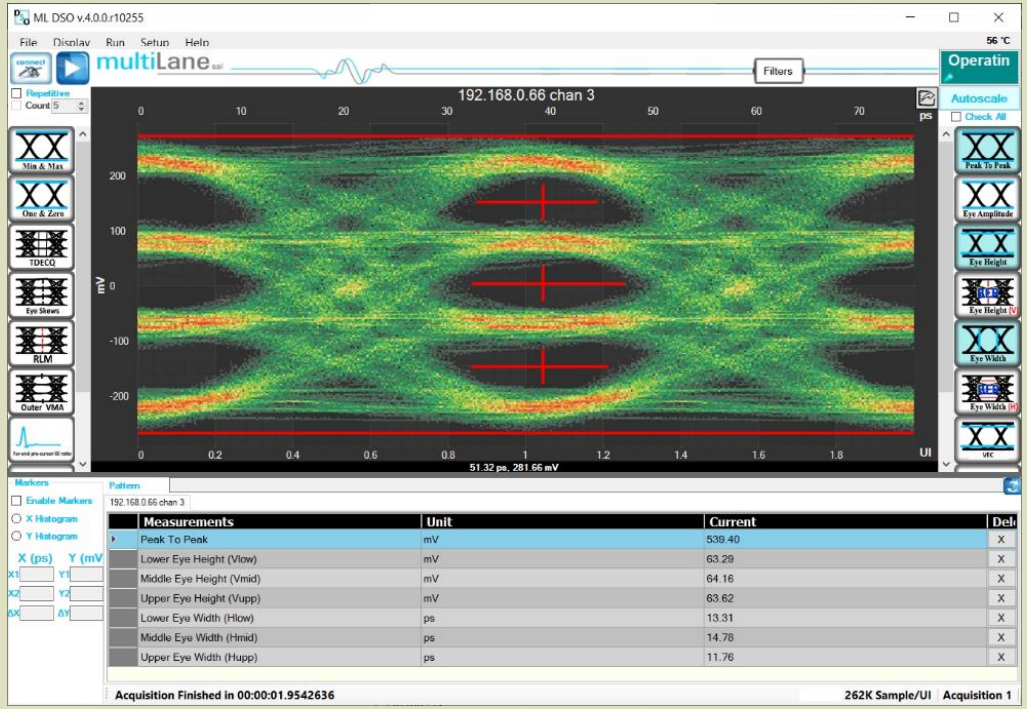


26.5625 GBd PAM4
Eye Measurement (3-Tap FIR)
DUT will PASS



DSO Capture using DUT LTX 3-tap FIR

Signal path compensation recovers DUT PAM4 data eyes



	Datalogger Measurements	Unit	Value
1	Pk-Pk	mV	539.40
2	Lower Eye Height	mV	63.29
3	Middle Eye Height	mV	64.16
4	Upper Eye Height	mV	63.62
5	Lower Eye Width	ps	13.31
6	Middle Eye Width	ps	14.78
7	Upper Eye Width	ps	11.76

Summary

- 26.5625 GBd PAM4 DUT signals were successfully sourced and measured at device wafer probe – multisite die testing – 4-site testing happening NOW
- High-speed DUT I/O signals can be reconstructed by removing signal path distortion
- Turnkey V93000 high volume production testing with integrated high-speed BERTs, Scopes and Wafer Probing Hardware are a reality and are available today

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