

TWENTY THIRD ANNUAL



TestConX™

May 1 - 4, 2022

DoubleTree by Hilton
Mesa, Arizona

Archive

An intelligent automation tool for ATE engineers

Senthilkumar D., Prabhakaran K. & Mark Berry
Caliber Interconnect Solutions Pvt.Ltd



Mesa, Arizona • May 1- 4, 2022





Table of Contents

- 01** Introduction
- 02** Program flow in testing
- 03** Why Test Automation?
- 04** Prototype
- 05** Test Automation Steps
- 06** On target
- 07** Conclusion



An intelligent automation tool for ATE engineers

2 2022

Introduction

Silicon Explosion

- Better, Smaller, Faster, Cheaper!
- Collect more data, store it, process it faster
- Oh and use less Power!

Need ways to develop cost effective test programs faster!

Biggest challenge?

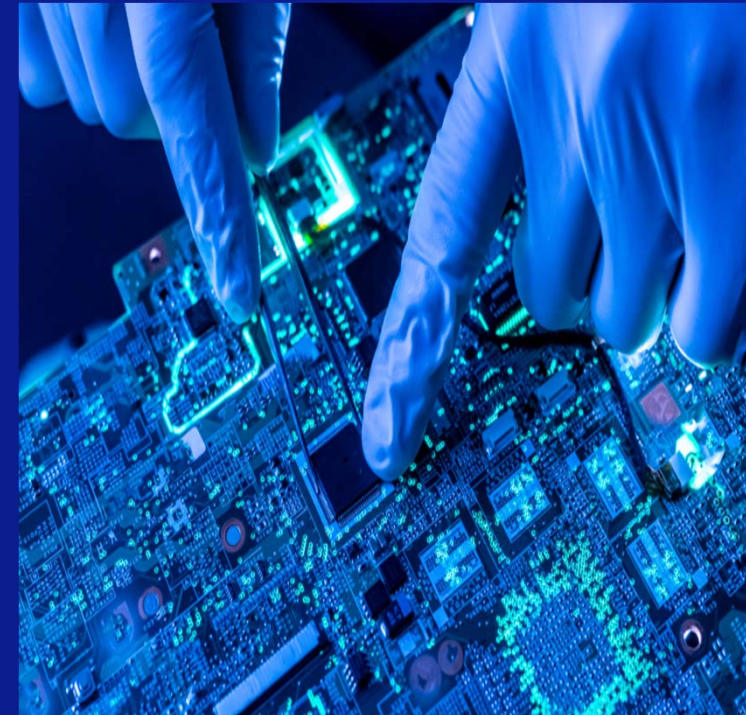
Reducing person hours for program dev & testing in post Si validation

Automation

Test provides an intelligent solution to reduce person hours and reduce human intervention (errors, opp cost)

Test Automation Tool

Aims to provide best possible automation in program generation in the absence of tester tool

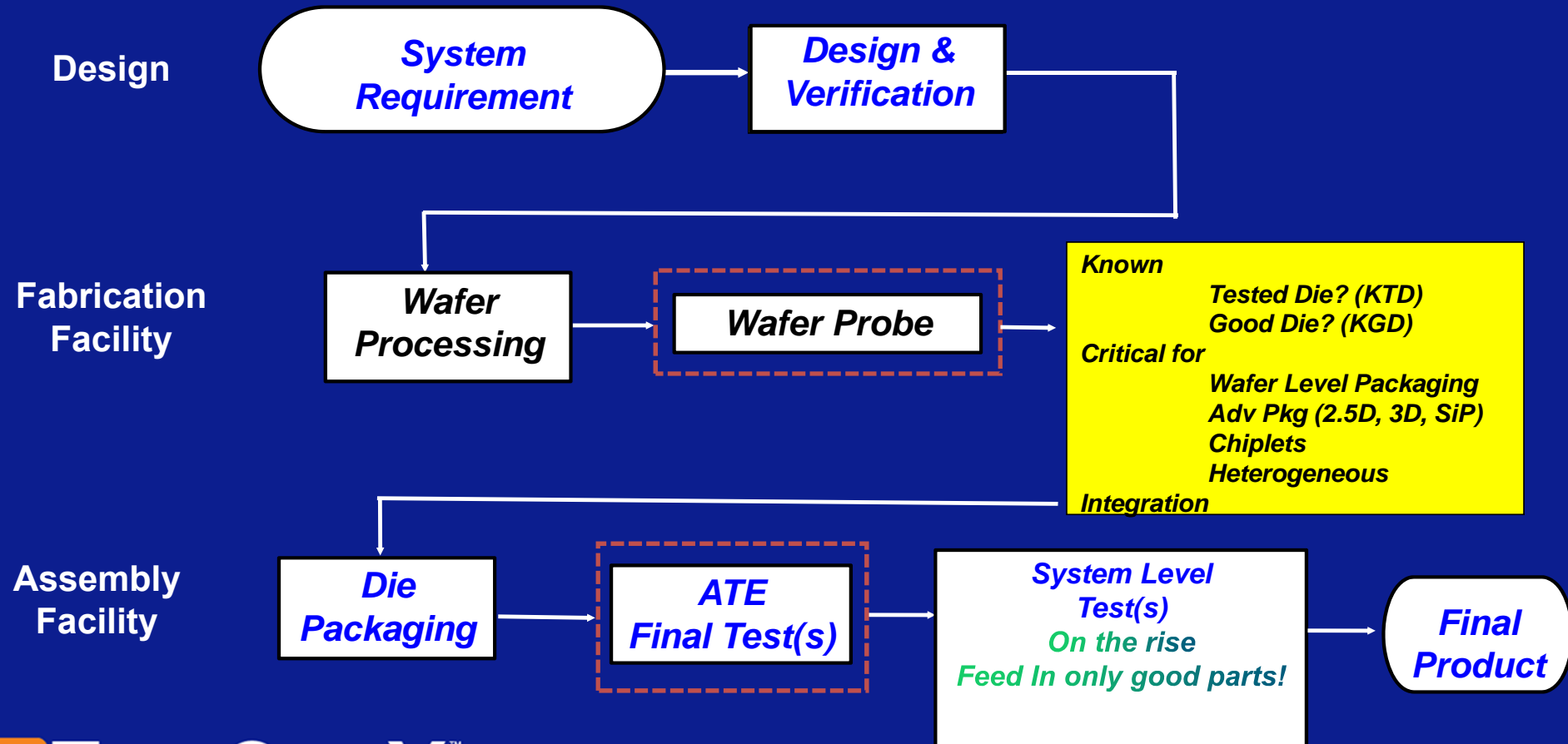


An intelligent automation tool for ATE engineers

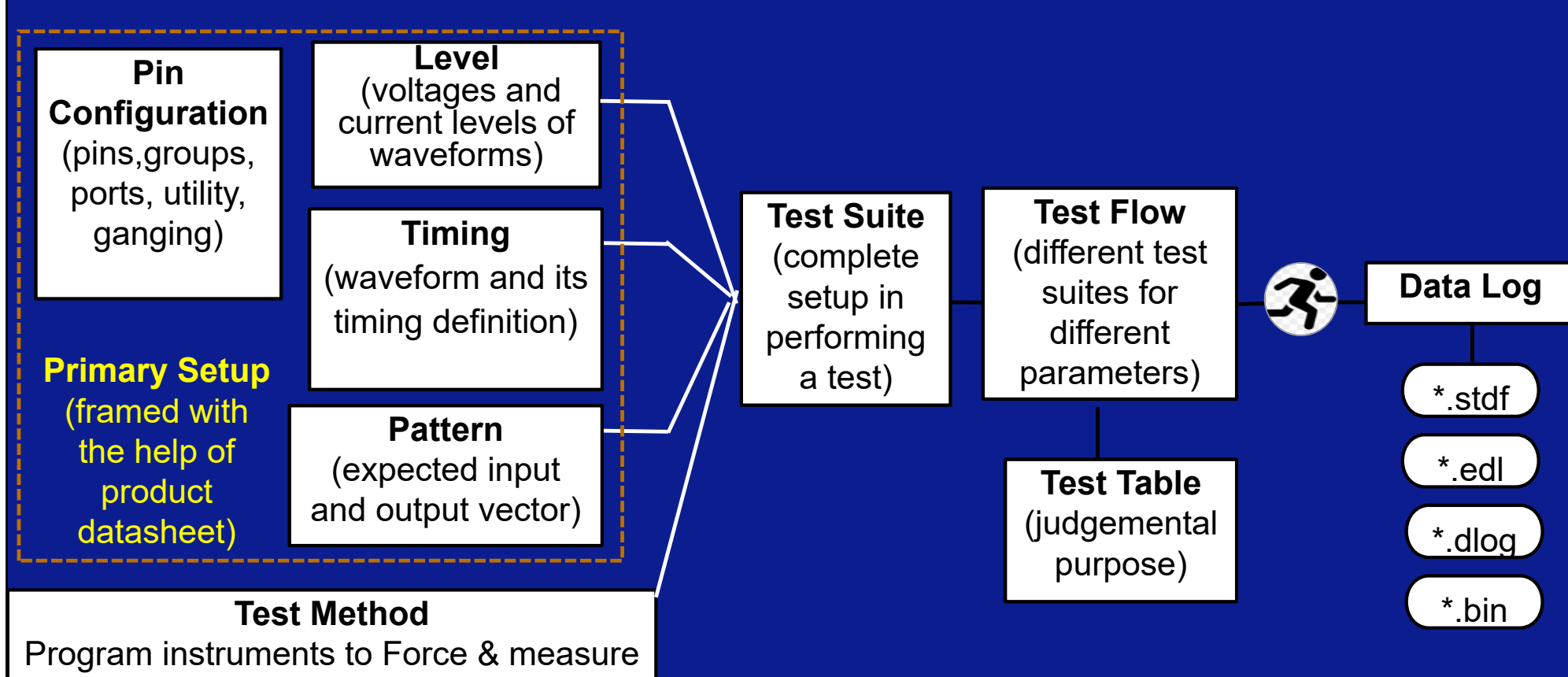
3

2022

Post Silicon Validation in Mfg Cycle



Test Program Development Flow

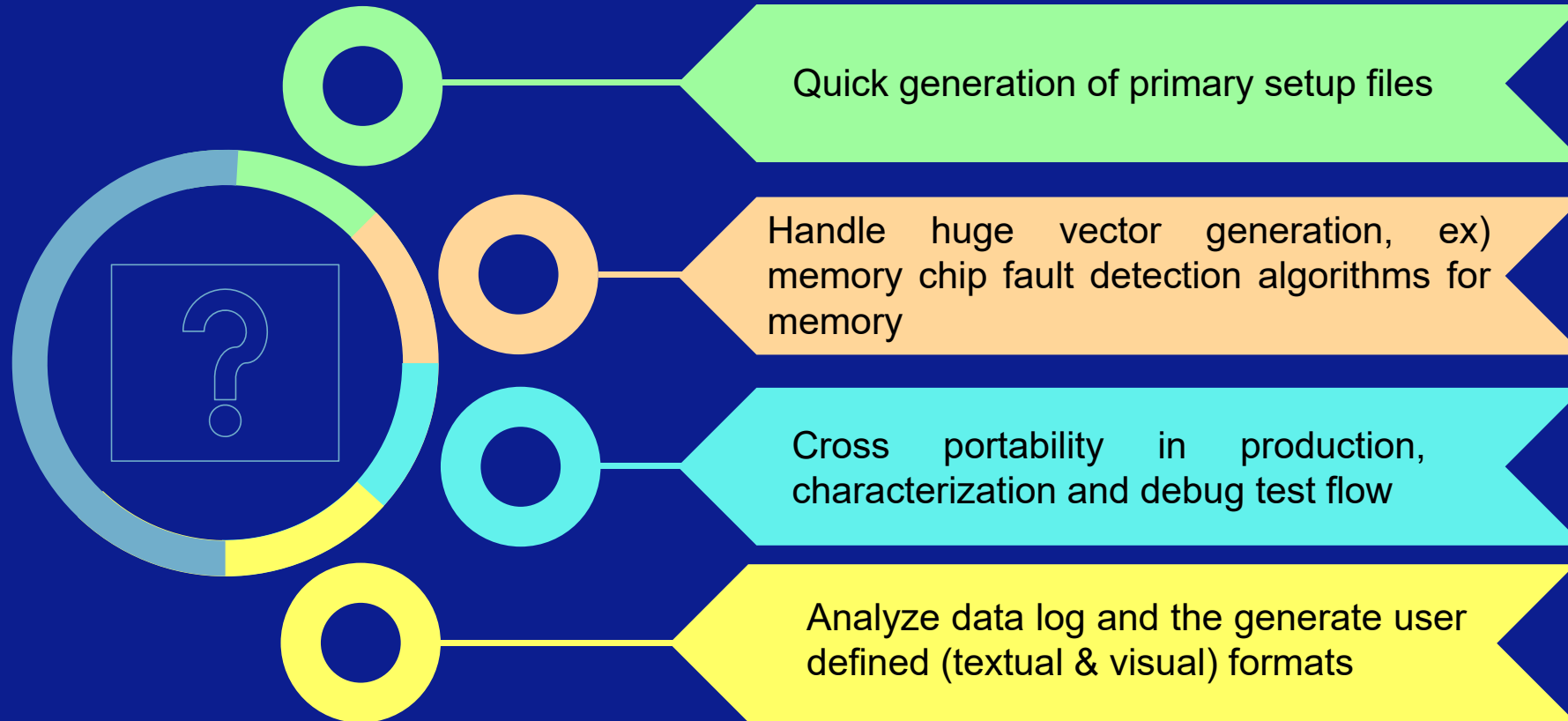


An intelligent automation tool for ATE engineers

5

2022

Why Test Automation?



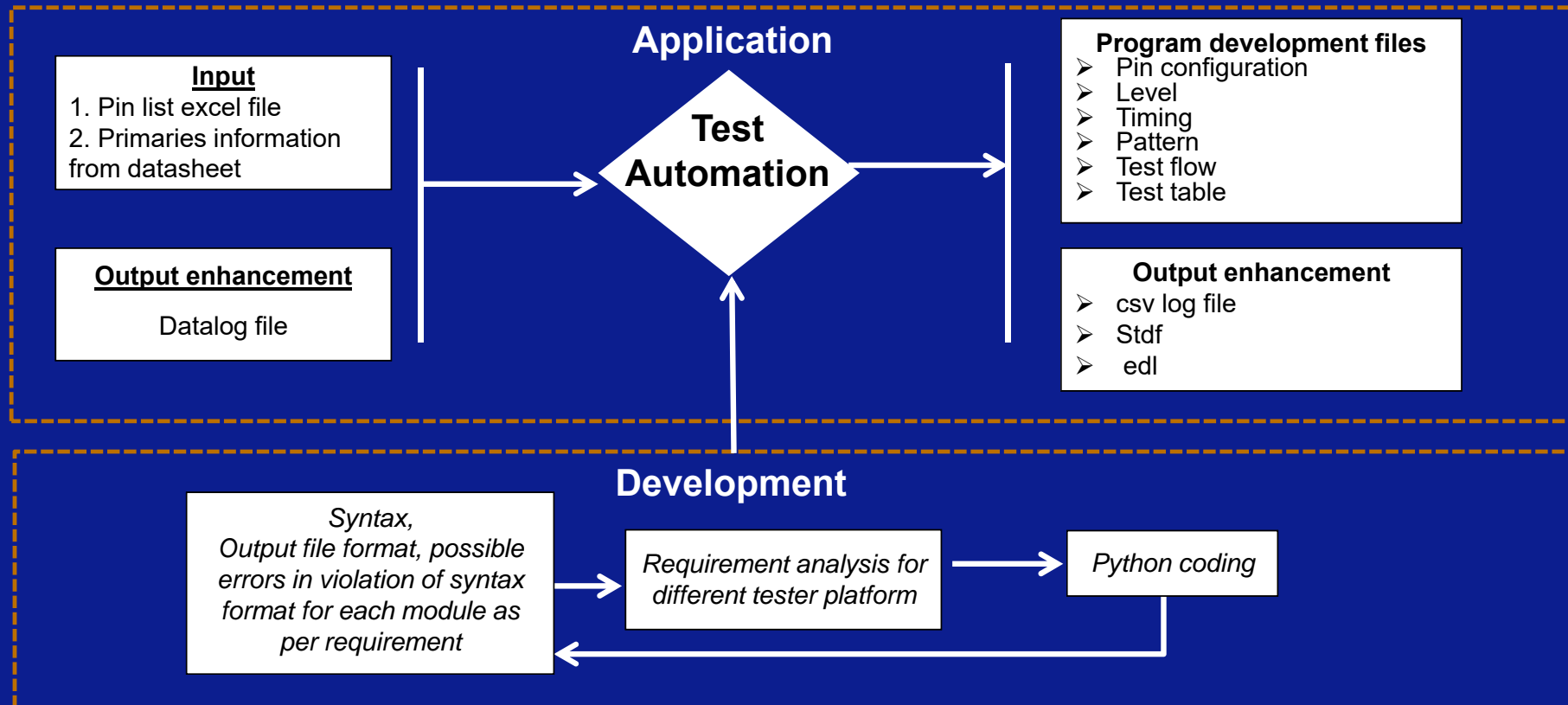
An intelligent automation tool for ATE engineers

6

2022

Prototype Model of Test Automation

Cyclic process: updated based on the new requirement

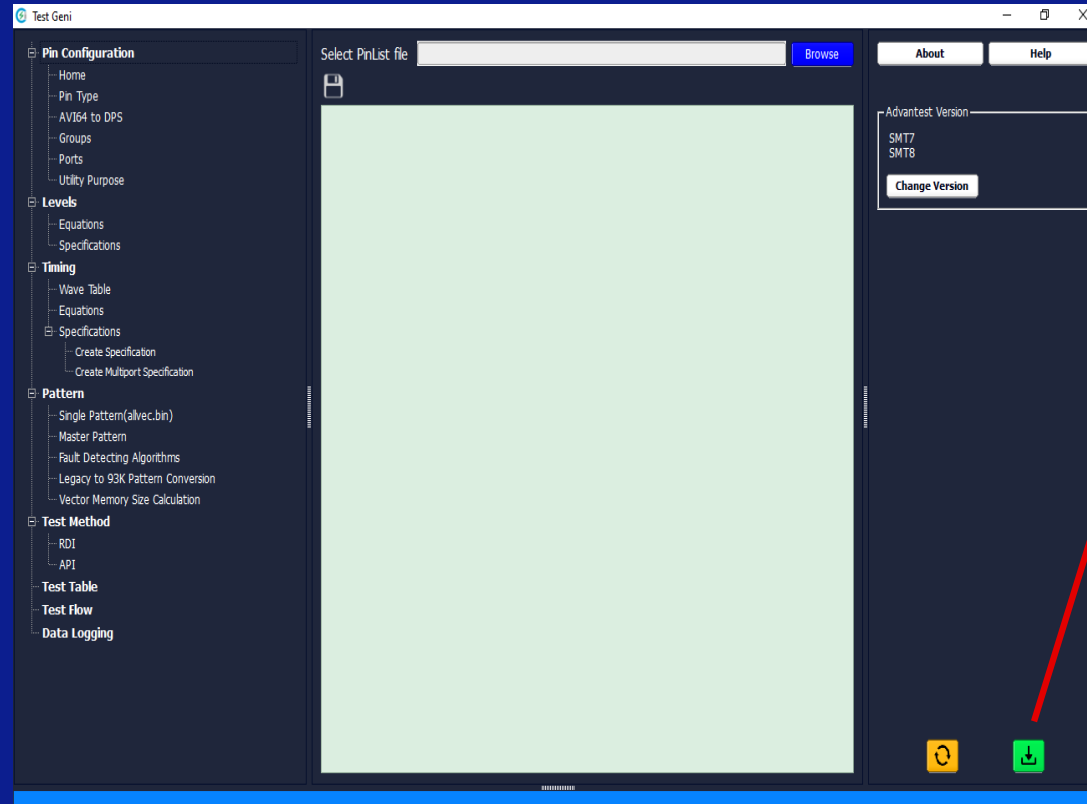


An intelligent automation tool for ATE engineers

7

2022

Test Automation UI



Ready to load test program files from TestGeni

- AC_FLAT_BITOFF_TIME.bin
- FTX1_9240_CONFIGURATION.cfg
- FTX1_9240_LEVEL.lev
- FTX1_9240_m40C-25C-85C_REV001.ttf
- FTX1_9240_TESTTABLE.csv
- FTX1_9240_TIMING.tim
- FTX1_9240_VECTORS.pmf

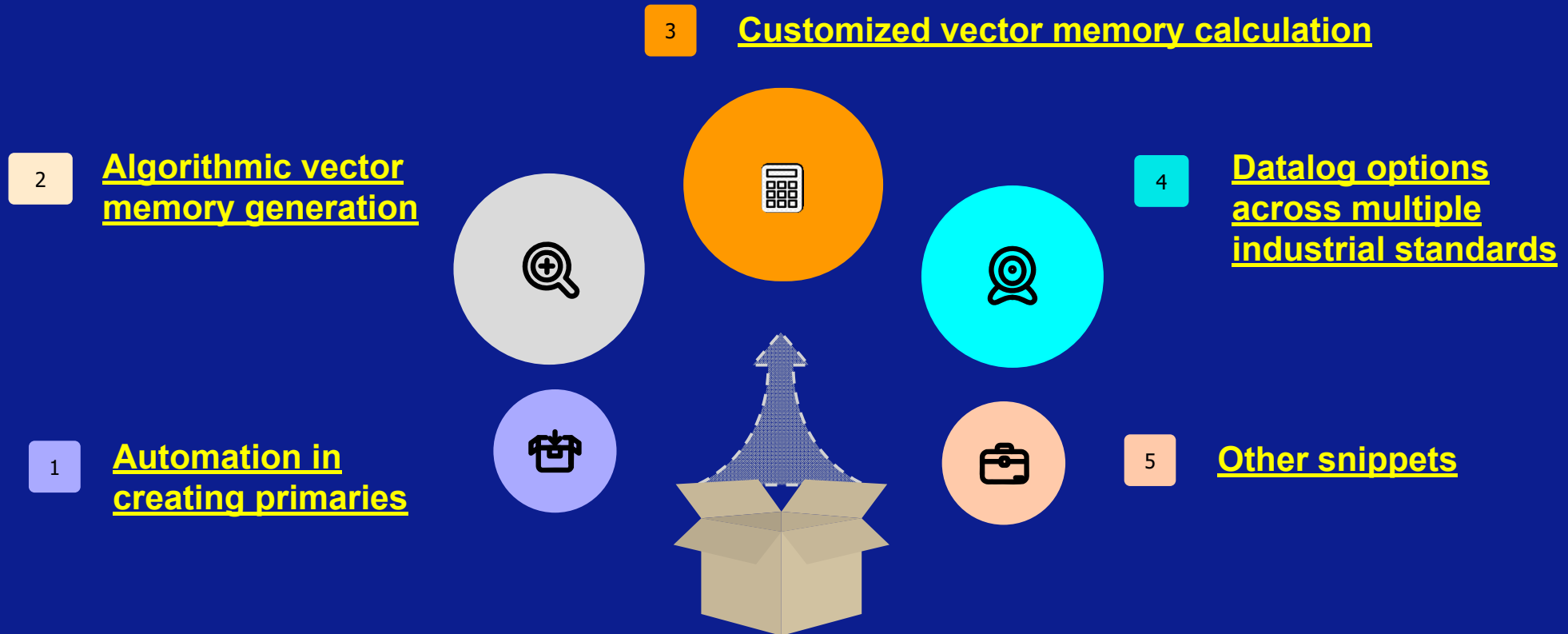


An intelligent automation tool for ATE engineers

8

2022

Glimpses of Test Automation Features



An intelligent automation tool for ATE engineers

9

2022

Steps in Automation for Primaries Generation

- ✓ Converts excel file into a loadable pin config file supported by tester tool
- ✓ Time reduction in feeding pins for primary setup file
- ✓ Customizable with any kind of pin info to tester compatible pin config
- ✓ Auto validates input parameters in all possible aspects

Select PinList file C:/Users/user/Downloads/single-site-list.xlsx Browse

	A	B	C	D
	Pin name	Pin no	Pin Type	Channel no
1	10E	50	IO	107
2	1A1	47	IO	107
3	1A2	46	IO	107
4	1A3	44	IO	107
5	1A4	43	IO	106
6	20E	48	IO	106
7	2A1	41	IO	105
8	2A2	40	IO	108
9	2A3	38	IO	107
10	2A4	37	IO	105
11	30E	25	IO	108
12	3A1	36	IO	103
13	3A2	35	IO	107
14	3A3	34	IO	105
15	3A4	32	IO	103
16	40E	24	IO	107
17	4A1	30	IO	10311

Open File

Look in: D:\TEST_GENI

My Computer user

Multi-site-Static.xlsx
Multisite-Static.xlsx
single-site-Static.xlsx

File name:

Files of type: Excel File (*.xls*)

Pin Name	Pin number	Channel Number	Channel Number_2	Channel Number_3
av1clr	20	32901	32902	32903
av1clk	21	32904	32905	32906
av2clr	22	33001	33002	33003
av2clk	23	33004	33005	33006
1clr	2	10603	10402	10403
1ck	1	10808	10404	10405
2clr	12	10501	10311	10312
2ck	13	10805	10414	10413
1qa	3	10605	10406	10205
1qb	4	10702	10301	10305
1qc	5	10616	10408	10407
1qd	6	10513	10303	10207
2qa	11	10608	10416	10415
2qb	10	10705	10302	10306
2qce	9	10802	10309	10308
2qd	8	10512	10304	10307
VCC	14	42901	22502	22505
Utility_1		UT1804	UT1102	UT1104



An intelligent automation tool for ATE engineers

10

2022

Automation in Creating Primary files

Defining Primaries in tester tools

```
EQUNSET 1 "LEV_EQUNSET_CONT_DPSSSHORT_01"
SPECS
    VCC [V]
    VIL [V]
    VIH [V]
    VOL [V]
    VOH [V]
    IOL [mA]
    IOH [mA]
    VT [V]
DPSPINS VCC
vout= VCC
vout_frc_rng=7
iout_clamp_rng=500
ilimit=500
t_ms=4
offcurr=act
#connect_state= UNGANG
LEVELSET 1 "LEVSET1_CONT"
PINS cont_pins

vil=VIL
vih=VIH
vol=VOL
voh=VOH
vt=VT
iol=IOL
ioh=IOH
```

Smart GUI for defining primaries

The GUI interface for defining primaries includes the following elements:

- EQUNSET:** A dropdown menu showing 'AC_Lev' with buttons for 'Create', 'Delete', and 'Rename'.
- EQUNSETs:** A list of EQUNSETs, including '1 | LEV_EQUNSET_CONT'.
- LEVELSET:** A dropdown menu for selecting a level set.
- LEVEL SETS:** A list of level sets (1-5) with buttons for 'Add >>', '<< Remove', 'Edit', and '@diff'.
- Available PINS/Groups:** A list of available pins/groups.
- Added PINS:** A list of added pins, including '10E,1A1,1A2,1A3,1'.
- SPEC Name:** A dropdown menu for selecting a specification name.
- SPEC Unit:** A dropdown menu for selecting a specification unit.
- SPECS:** A list of specifications (VCC, VIL, VIH, VOL, VOH, IOL, IOH, VT) with buttons for 'Add Spec', 'Remove Spec', and 'Edit Spec'.
- Result Table:** A table with columns for 'Source Param', 'Units & Rang', and 'Result'.
- SPECSET Tool:** A button for accessing the specification set tool.

- ✓ Time reduction in test program development
- ✓ Supports multi-tester platforms
- ✓ Avoids Manual syntax errors



An intelligent automation tool for ATE engineers

11 2022

User Friendly UI Primary File Generation

The screenshot displays the Test Geni GUI with the following sections and annotations:

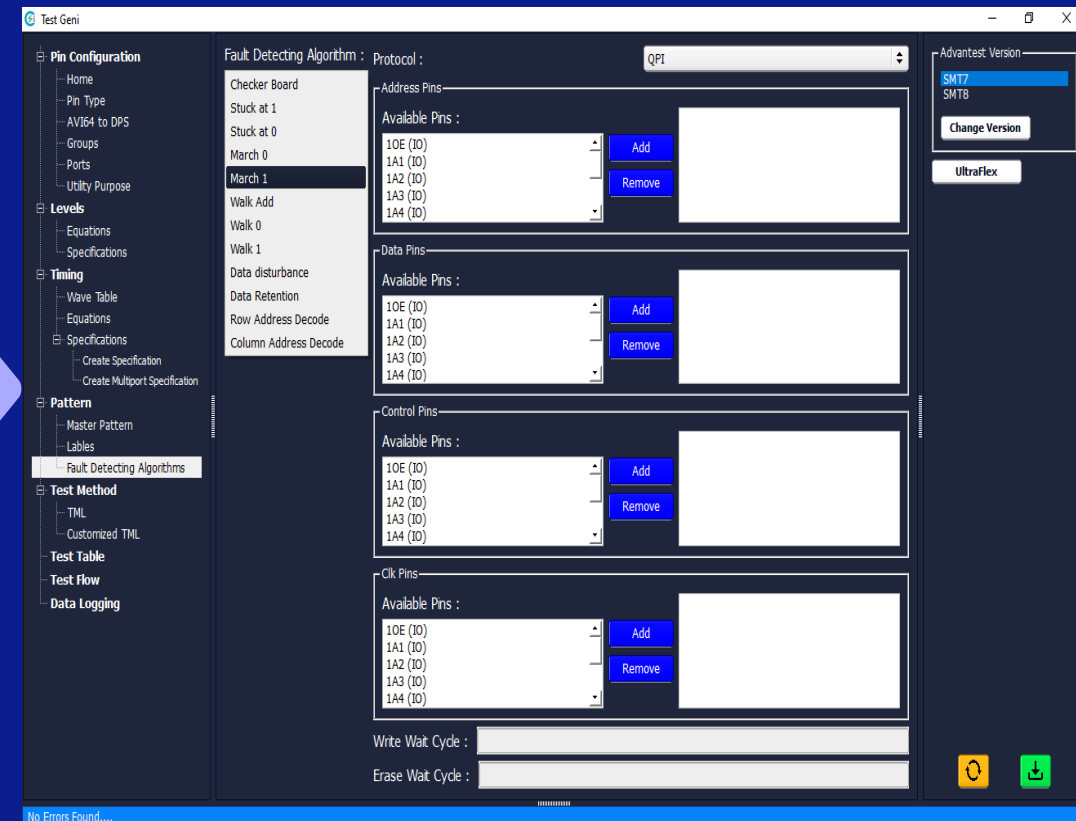
- Pin Configuration:** Includes a sidebar with 'Home', 'Pin Type', 'AVI64 to DPS', 'Groups', 'Ports', and 'Utility Purpose'. The main area shows 'WAVETBL Name:' with 'Create', 'Delete', and 'Rename' buttons. Below is a 'WAVETBLs:' list containing 'gross_func'.
- Timing:** A window titled 'Timing - PINS for Wavetable - gross_func' is open. It shows 'Available Pins/Groups:' with a list of pins (IN1, out, INN0, INN1, OUTN0, OUTN1, OUTN2, OUTN3) and their types (IO, O). A red box highlights this list with the text: "Adding pins, @diff definition are easy".
- Wave Forms:** A section showing the 'WAVETBL gross_func' definition. It includes 'DEFINES Dig' and a list of pins with their values: '0 "d1:0 d2:0 d3:0 d4:0" 0000', '1 "d1:1 d2:1 d3:1 d4:1" 1111', '2 "r1:L r2:L r3:L r4:L" LLLL', and '3 "r1:H r2:H r3:H r4:H" HHHH'. A red box highlights this section with the text: "Preview of GUI generated primary definition".
- Wave Form Errors:** A table listing errors in the wave form definition. A red box highlights this table with the text: "Prompting the spec, manual, syntax errors, once it is feed".

Simplistic Vector Generation

✓ Easy generation of huge vectors with the help of algorithms

✓ Communication protocol and algorithmic patterns are generated at once

✓ All fault detecting algorithms are enveloped



An intelligent automation tool for ATE engineers

13

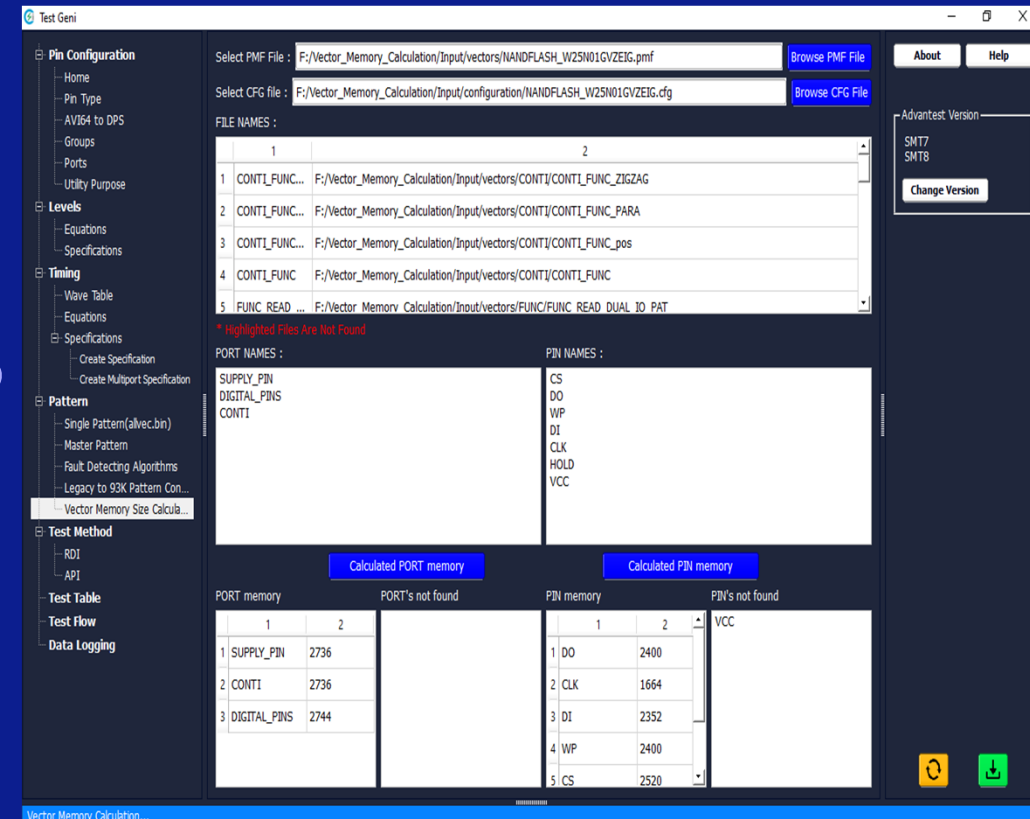
2022

Vector Memory Size Calculator

✓ Firmware commands are essential to individually assess the size of vector memory for each pin

✓ Tool facilitates user-friendly GUI with vector & config files

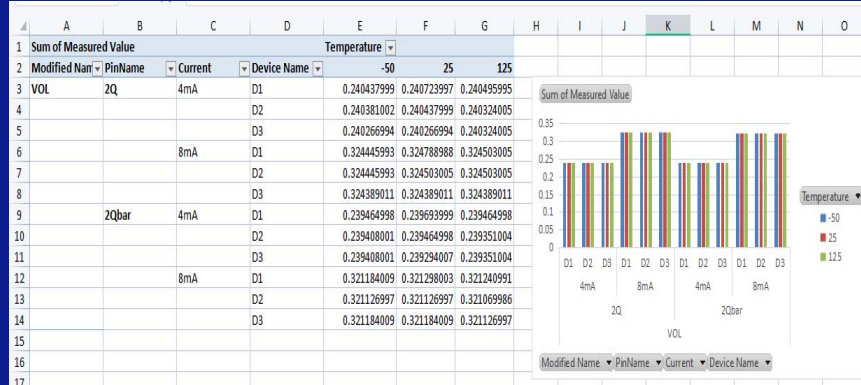
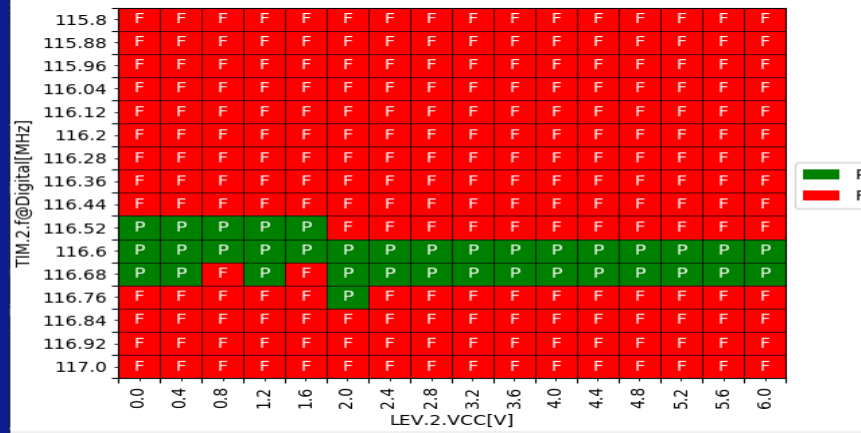
✓ Selected pin, port, vector wise memory size calculation



An intelligent automation tool for ATE engineers

14 2022

Data Logging



✓ Converting stdf file into an expansive csv file with easy accessibility & organized parametrics

✓ Data & test time crunching for quick reporting

✓ Shmoo plot gen from datalog file

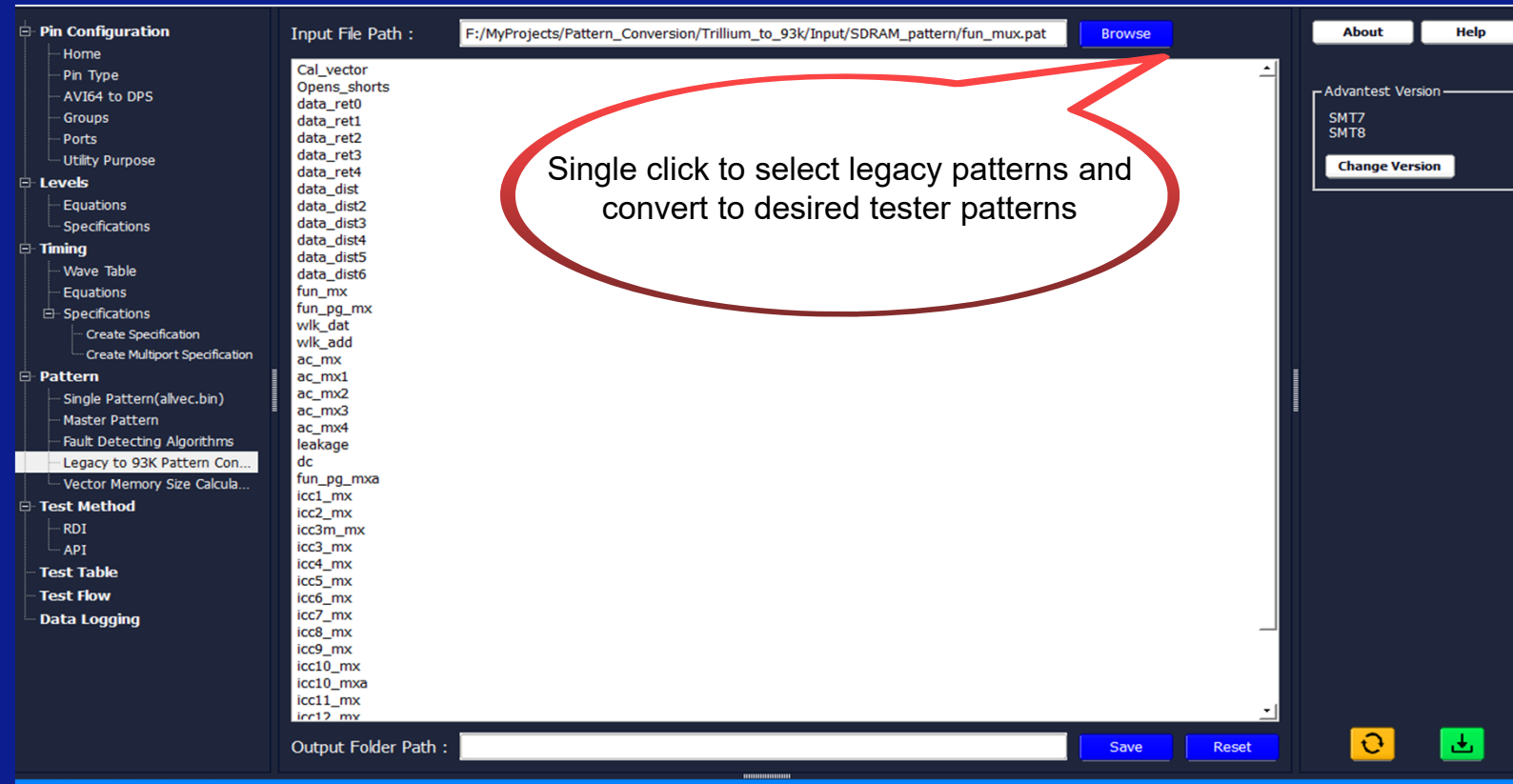


An intelligent automation tool for ATE engineers

15

2022

Expeditious Pattern Conversion

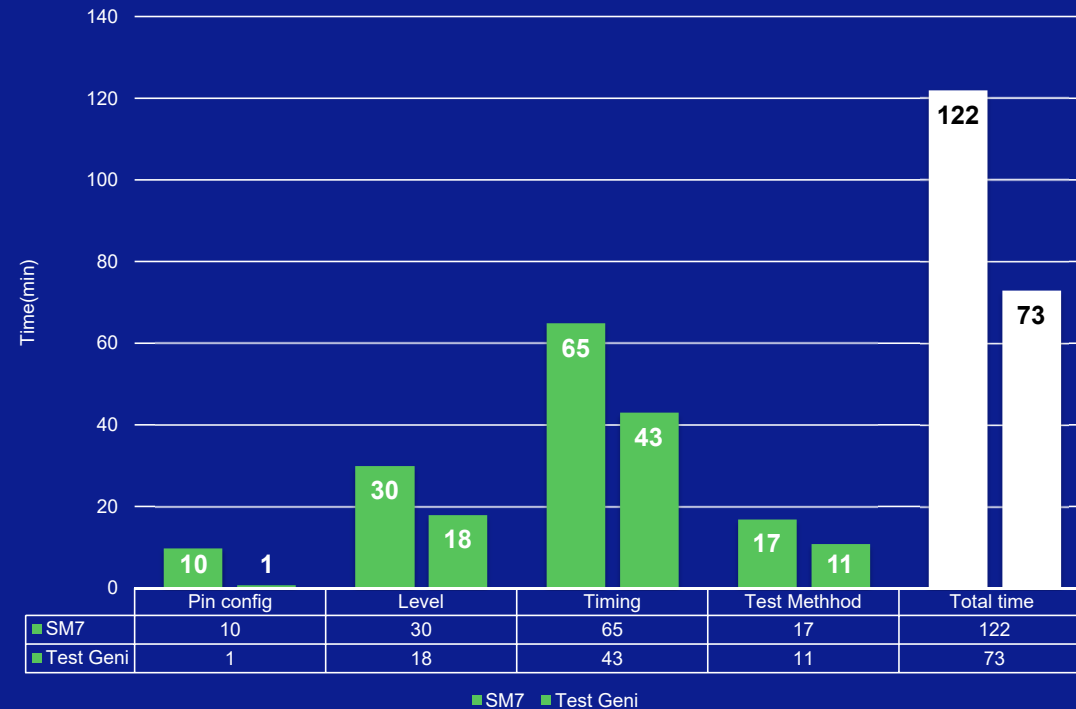


On Target

Use Case

- ✓ Digital ASIC
- ✓ Advantest 93000 & their SM7 tool
- ✓ Test Program Dev done using Tester tool & TestGeni for comparison
- ✓ Time saved? ~40%!

Development Time



An intelligent automation tool for ATE engineers

17 2022

Conclusion and Future Work

- TestGeni helps in automation needed for test program dev and aids in analyzing/reducing the test data to information – to save valuable test engineering person hours
- Incorporating new tester platform(J750, Uflex) for portability & support for additional tester platforms & more advanced features are in progress for greater optimization of time



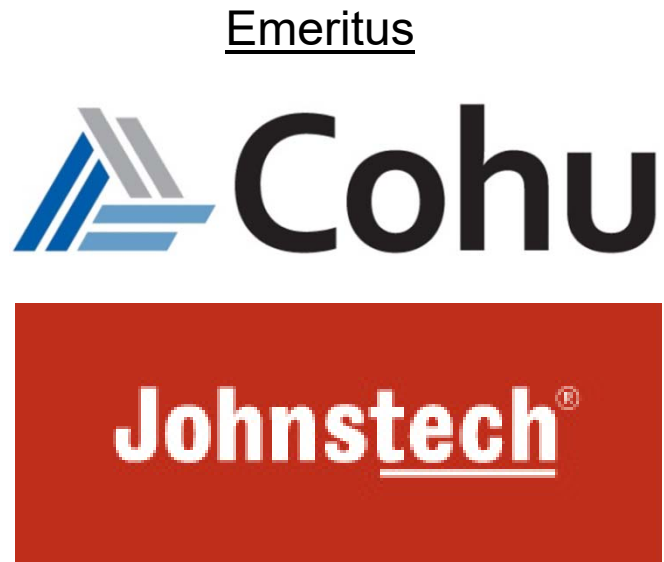
An intelligent automation tool for ATE engineers

18

2022

With Thanks to Our Sponsors!

Premier
HiCon



With Thanks to Our Sponsors!

Distinguished



Industry Partners



With Thanks to Our Sponsors!

Lanyards



Tutorial



Keynote

smiths
interconnect

Keycards



Totebag



Publication Sponsor



COPYRIGHT NOTICE

The presentation(s) / poster(s) in this publication comprise the Proceedings of the TestConX 2022 workshop. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the TestConX 2022 workshop. This version of the presentation or poster may differ from the version that was distributed at or prior to the TestConX 2022 workshop.

The inclusion of the presentations/posters in this publication does not constitute an endorsement by TestConX or the workshop's sponsors. There is NO copyright protection claimed on the presentation/poster content by TestConX. However, each presentation / poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

“TestConX”, the TestConX logo, and the TestConX China logo are trademarks of TestConX. All rights reserved.

www.testconx.org