An intelligent automation tool for ATE engineers

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Caliber Interconnect Solutions Pvt.Ltd

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Introduction

Silicon Explosion

- Better, Smaller, Faster, Cheaper!
- Collect more data, store it, process it faster
- Oh and use less Power!

Need ways to develop cost effective test programs faster!

Biggest challenge?

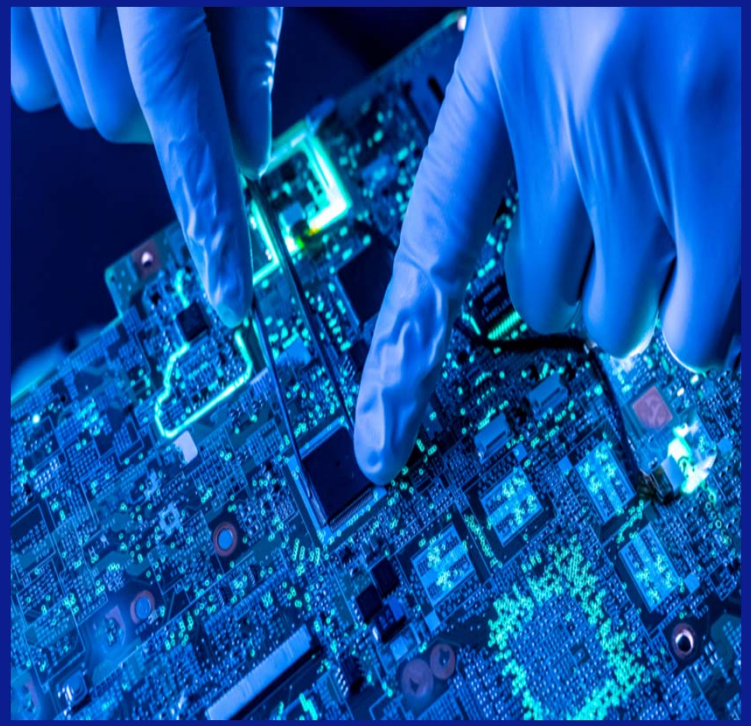
Reducing person hours for program dev & testing in post Si validation

Automation

Test provides an intelligent solution to reduce person hours and reduce human intervention (errors, opp cost)

Test Automation Tool

Aims to provide best possible automation in program generation in the absence of tester tool



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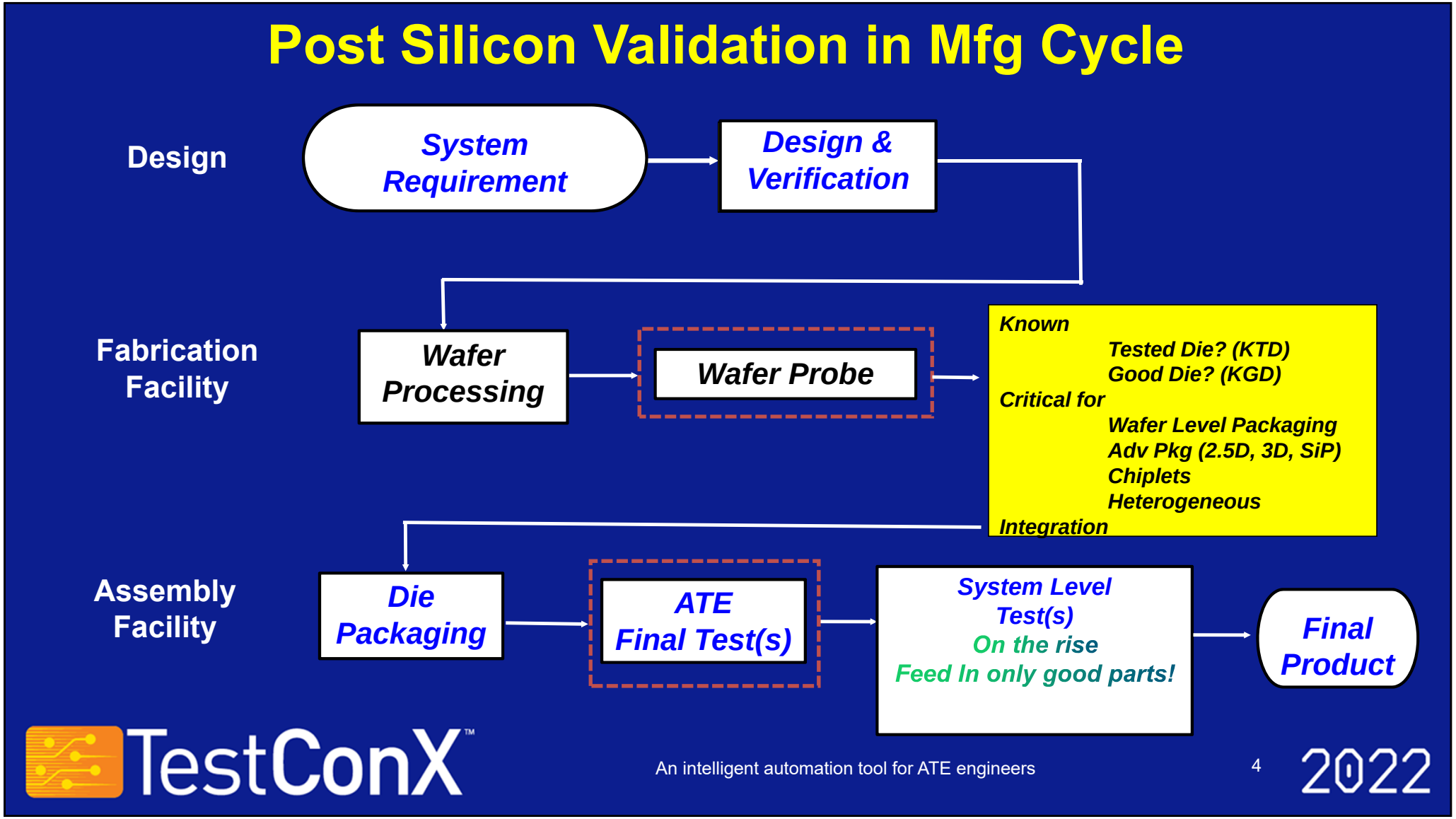
Post Silicon Validation in Mfg Cycle
Design
System Requirement
Design & Verification
Fabrication Facility
Wafer Processing
Wafer Probe
Known
Tested Die? (KTD)
Good Die? (KGD)
Critical for
Wafer Level Packaging
Adv Pkg (2.5D, 3D, SiP)
Chiplets
Heterogeneous
Integration
Assembly Facility
Die Packaging
ATE Final Test(s)
System Level Test(s)
On the rise
Feed In only good parts!
Final Product
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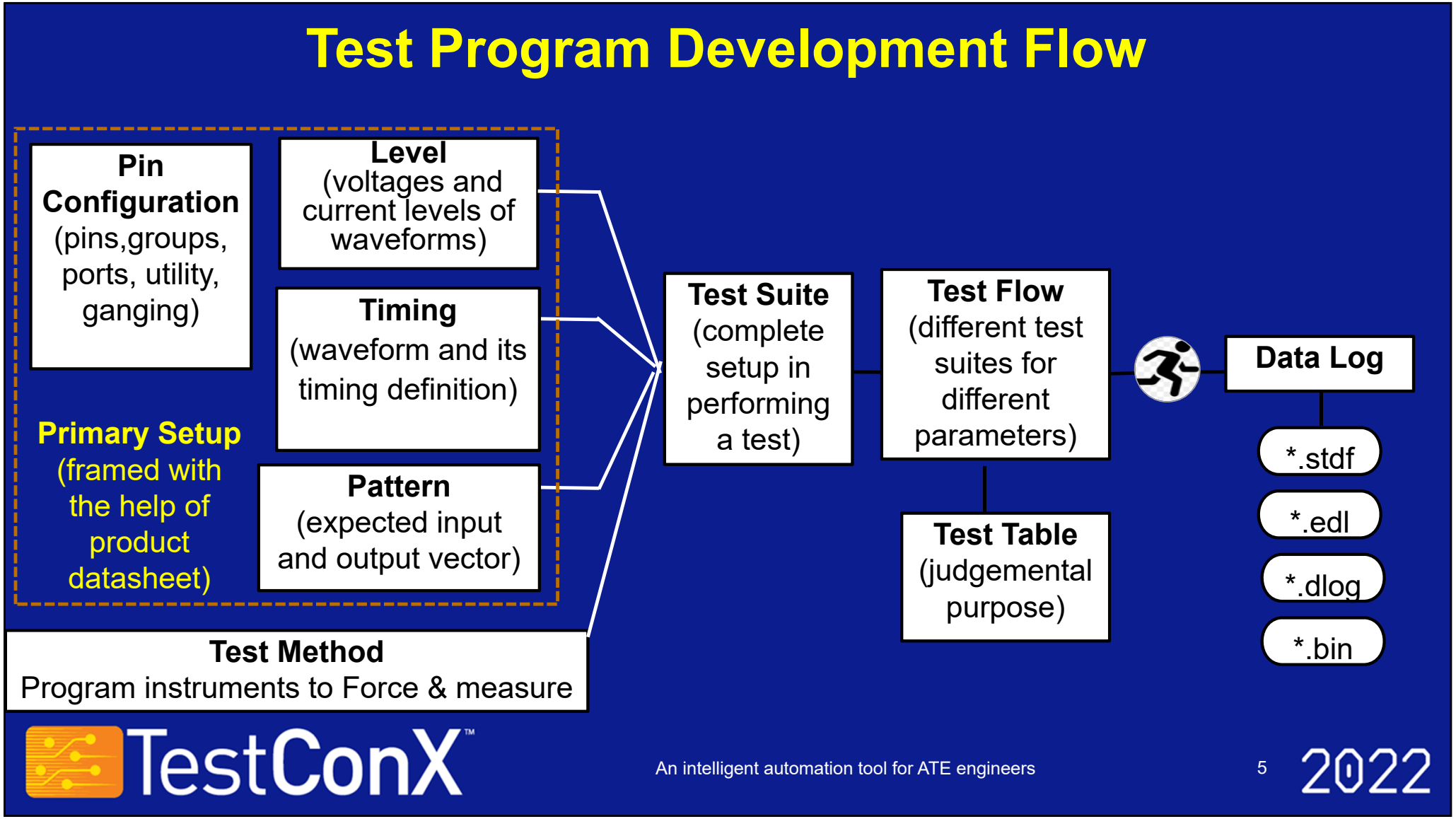
Test Program Development Flow
Pin Configuration (pins,groups, ports, utility, ganging)
Level (voltages and current levels of waveforms)
Timing (waveform and its timing definition)
Pattern (expected input and output vector)
Primary Setup (framed with the help of product datasheet)
Test Method
Program instruments to Force & measure
Test Suite (complete setup in performing a test)
Test Flow (different test suites for different parameters)
Test Table (judgemental purpose)
Data Log
*.stdf
*.edl
*.dlog
*.bin
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Why Test Automation?

- Quick generation of primary setup files
- Handle huge vector generation, ex) memory chip fault detection algorithms for memory
- Cross portability in production, characterization and debug test flow
- Analyze data log and the generate user defined (textual & visual) formats

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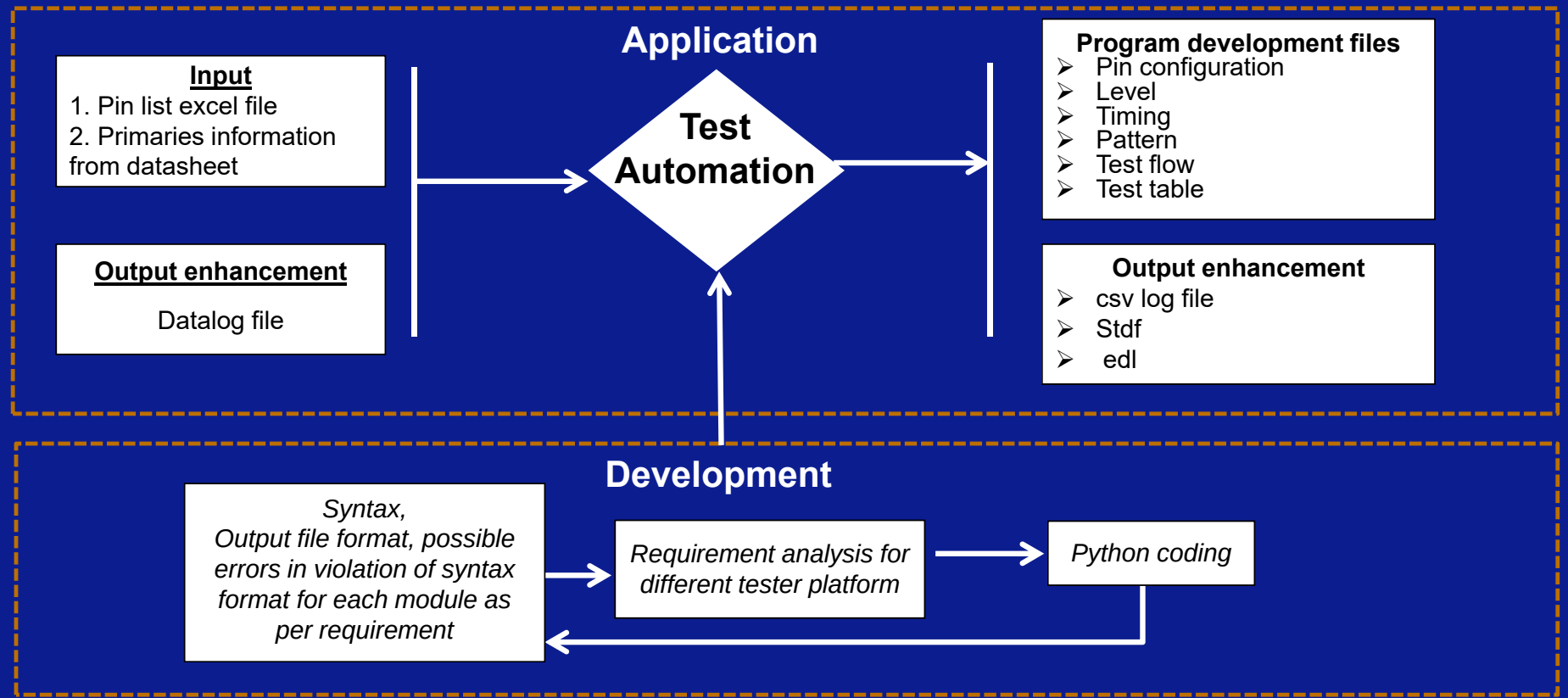
Prototype Model of Test Automation

Cyclic process: updated based on the new requirement



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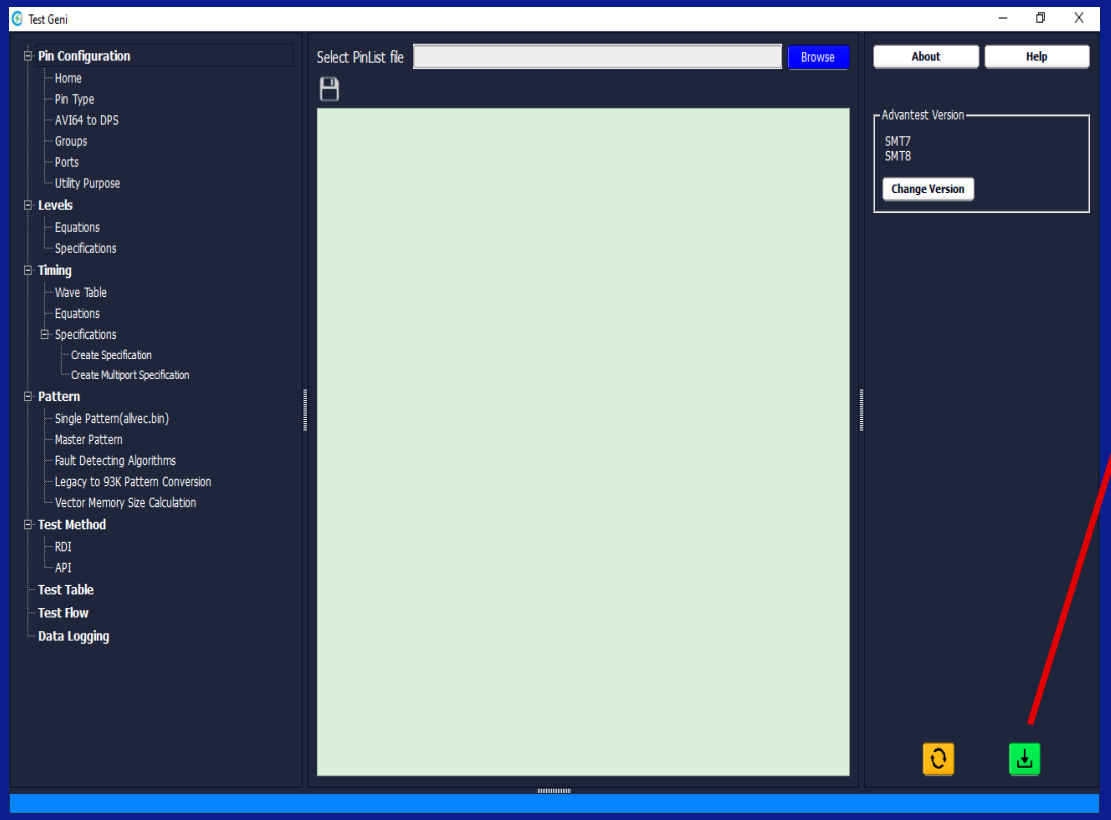
Test Automation UI



Ready to load test program files from TestGeni

- AC_FLAT_BITOFF_TIME.bin
- FTX1_9240_CONFIGURATION.cfg
- FTX1_9240_LEVEL.lev
- FTX1_9240_m40C-25C-85C_REV001.ttf
- FTX1_9240_TESTTABLE.csv
- FTX1_9240_TIMING.tim
- FTX1_9240_VECTORS.pmf

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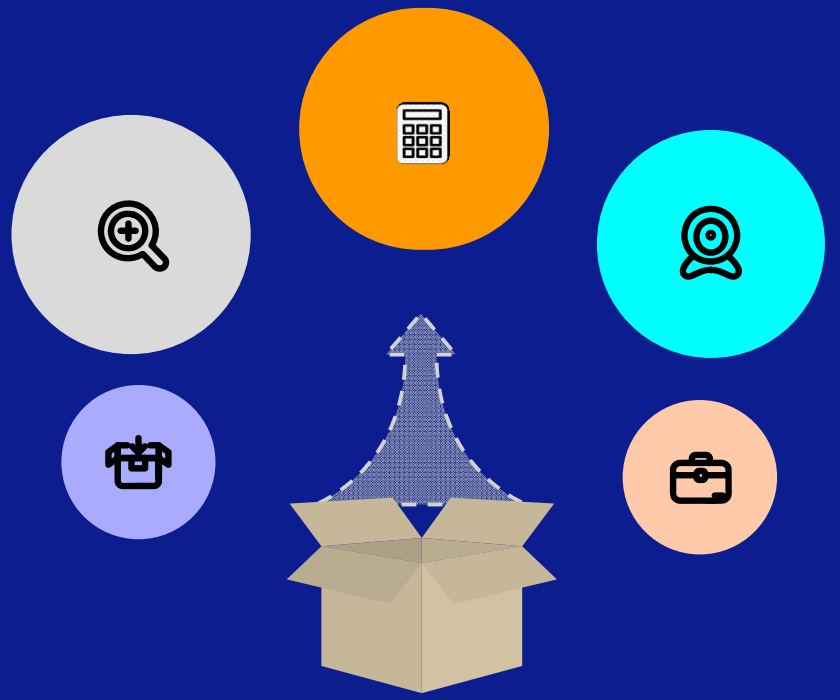
Glimpses of Test Automation Features

3 Customized vector memory calculation

2 Algorithmic vector memory generation

4 Datalog options across multiple industrial standards



1 Automation in creating primaries

5 Other snippets

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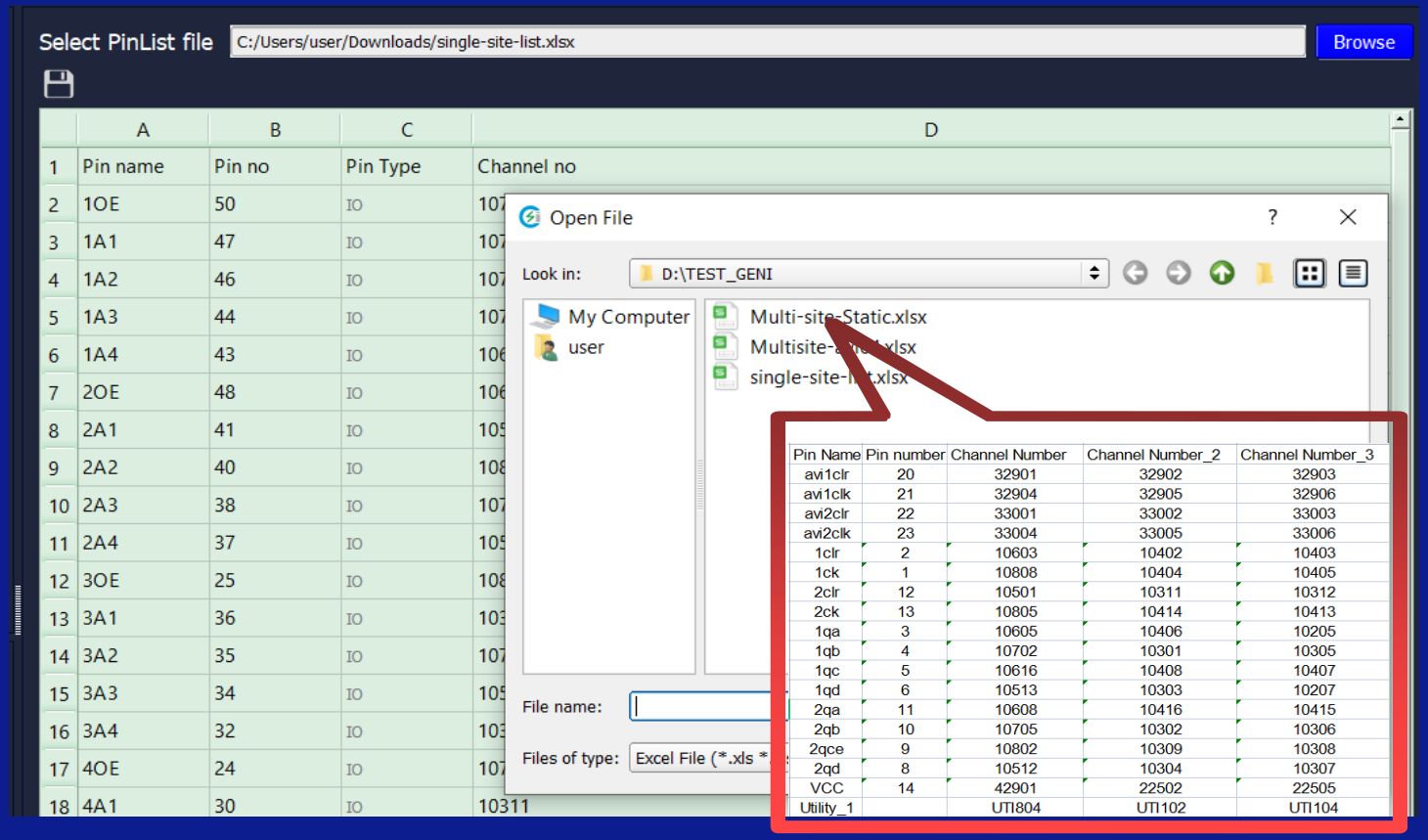
Steps in Automation for Primaries Generation

- ✓ Converts excel file into a loadable pin config file supported by tester tool
- ✓ Time reduction in feeding pins for primary setup file
- ✓ Customizable with any kind of pin info to tester compatible pin config
- ✓ Auto validates input parameters in all possible aspects



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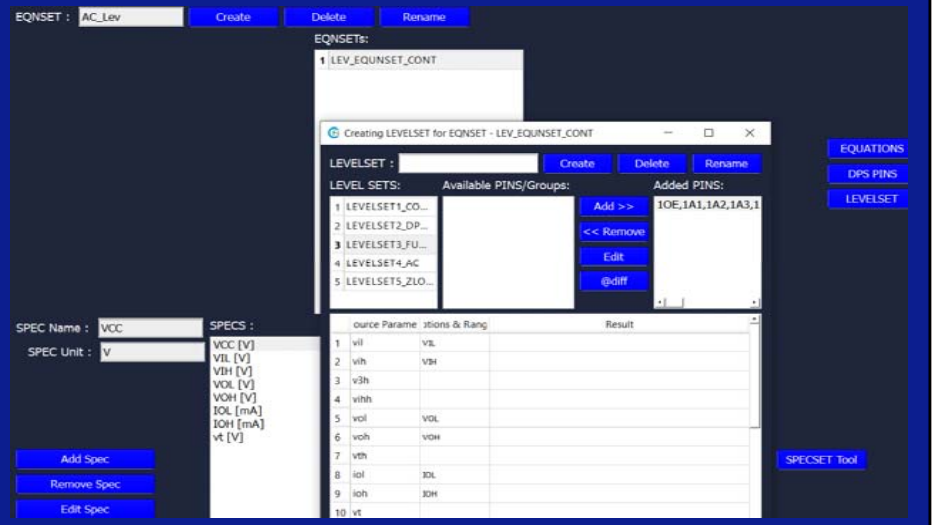
Automation in Creating Primary files

Defining Primaries in tester tools

```
EQNSET 1 "LEV_EQUNSET_CONT_DPSSHORT_01"
SPECS
     VCC [V]
     VIL [V]
     VIH [V]
     VOL [V]
     VOH [V]
     IOL [mA]
     IOH [mA]
     VT [V]
DPSPINS VCC
vout= VCC
vout_frc_rng=7
iout_clamp_rng=500
ilimit=500
t_ms=4
offcurr=act
#connect_state= UNGANG
LEVELSET 1 "LEVSET1_CONT"
PINS cont_pins

vil=VIL
vih=VIH
vol=VOL
voh=VOH
vt=VT
iol=IOL
ioh=IOH
```

Smart GUI for defining primaries



- ✓ Time reduction in test program development
- ✓ Supports multi-tester platforms
- ✓ Avoids Manual syntax errors

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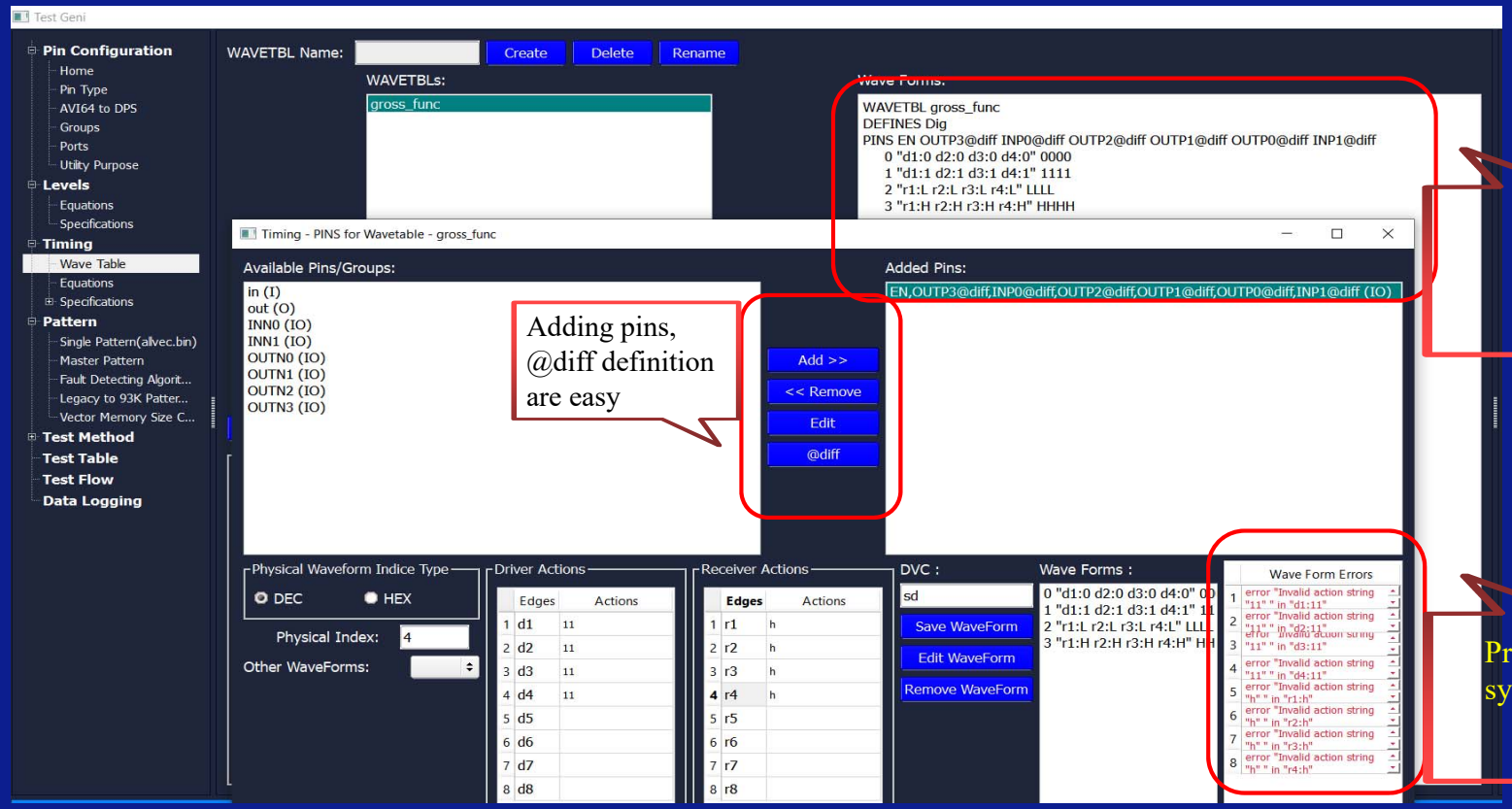
User Friendly UI Primary File Generation



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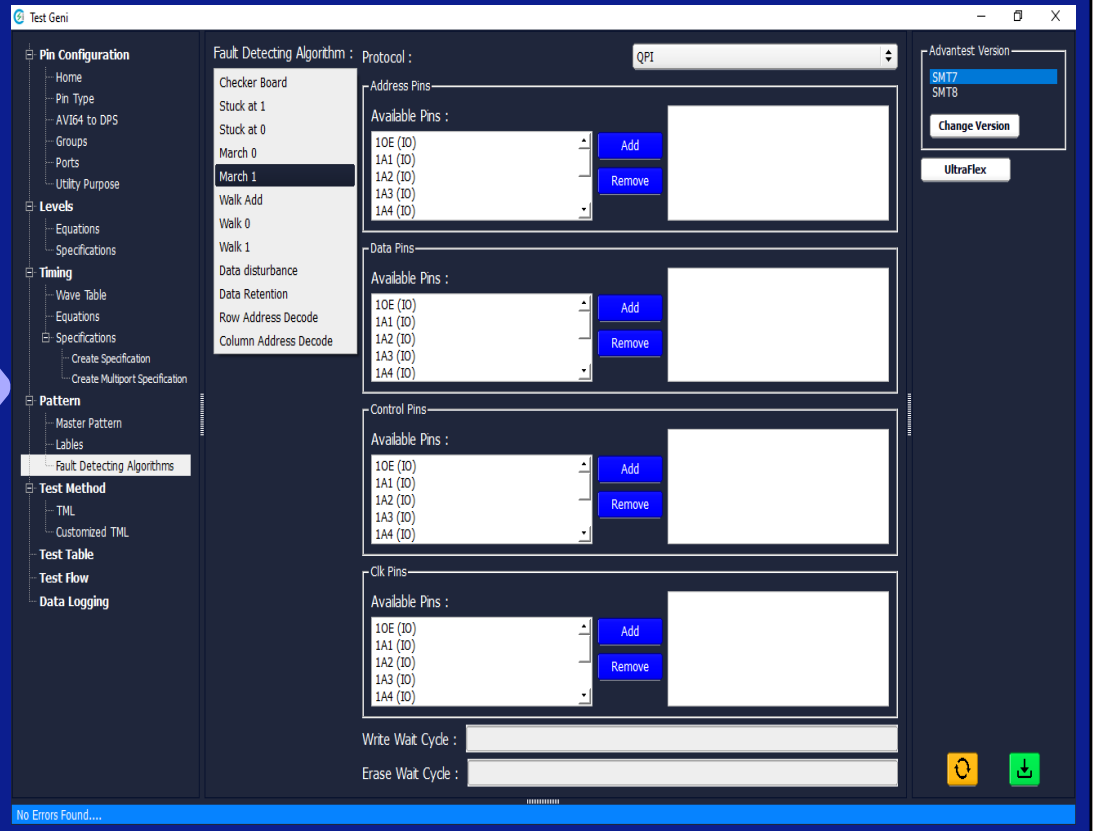
Simplistic Vector Generation

- ✓ Easy generation of huge vectors with the help of algorithms
- ✓ Communication protocol and algorithmic patterns are generated at once
- ✓ All fault detecting algorithms are enveloped



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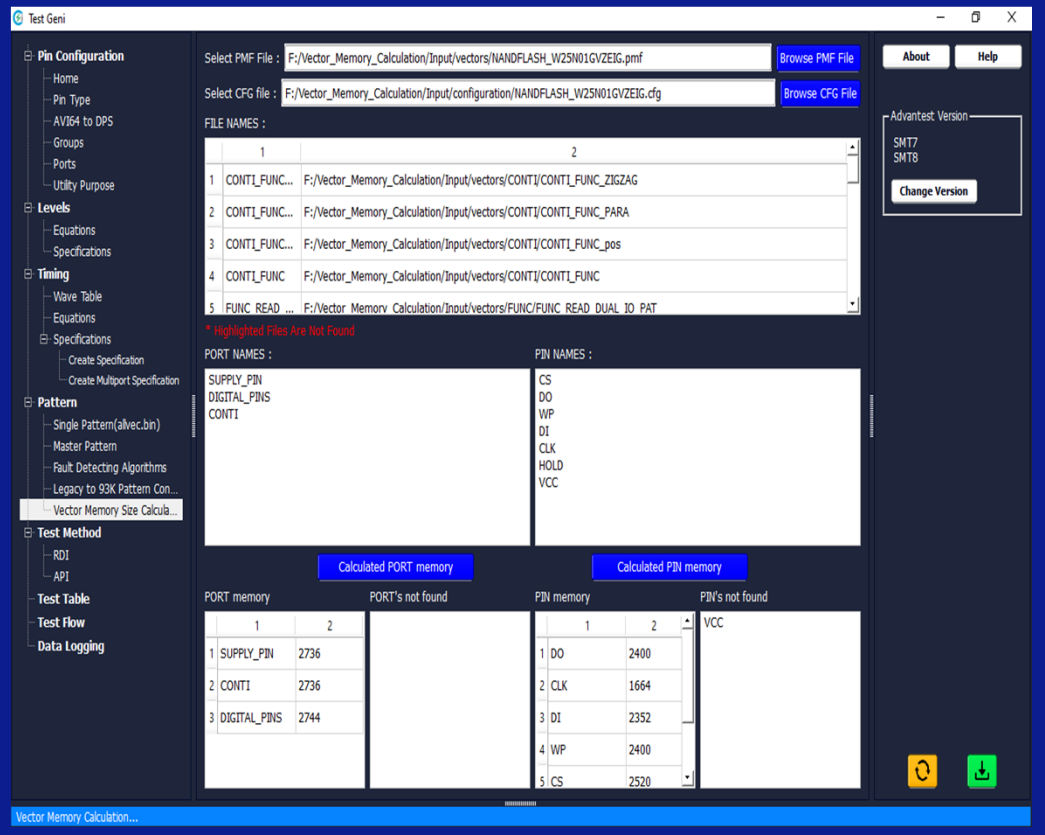
Vector Memory Size Calculator

- ✓ Firmware commands are essential to individually assess the size of vector memory for each pin
- ✓ Tool facilitates user-friendly GUI with vector & config files
- ✓ Selected pin, port, vector wise memory size calculation



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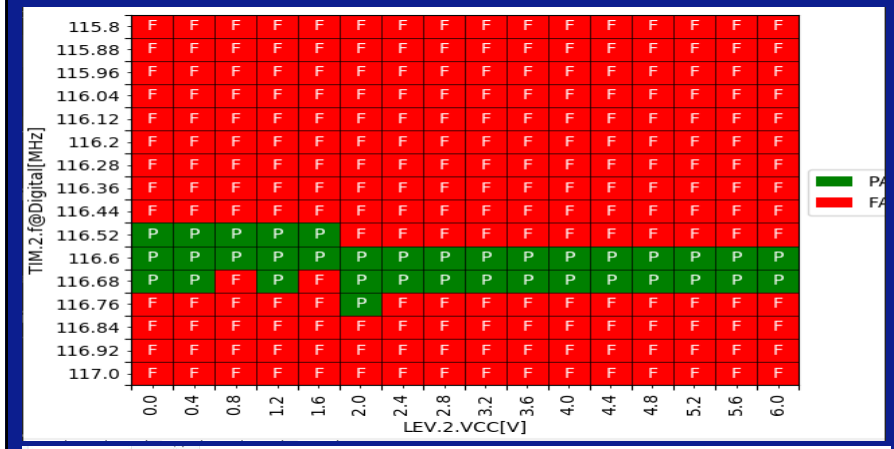
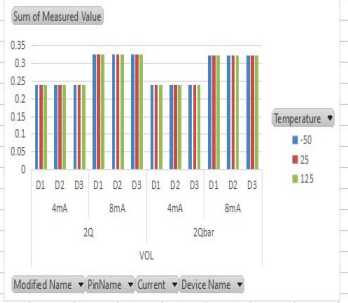
Data Logging



Sum of Measured Value				Temperature		
Modified Nam	PinName	Current	Device Name	-50	25	125
VOL	2Q	4mA	D1	0.240437999	0.240723997	0.240495995
			D2	0.240381002	0.240437999	0.240324005
			D3	0.240266994	0.240266994	0.240324005
		8mA	D1	0.324445993	0.324788988	0.324503005
			D2	0.324445993	0.324503005	0.324503005
			D3	0.324389011	0.324389011	0.324389011
	2Qbar	4mA	D1	0.239464998	0.239693999	0.239464998
			D2	0.239408001	0.239464998	0.239351004
			D3	0.239408001	0.239294007	0.239351004
		8mA	D1	0.321184009	0.321298003	0.321240991
			D2	0.321126997	0.321126997	0.321069986
			D3	0.321184009	0.321184009	0.321126997



- ✓ Converting stdf file into an expansive csv file with easy accessibility & organized parametrics
- ✓ Data & test time crunching for quick reporting
- ✓ Shmoo plot gen from datalog file

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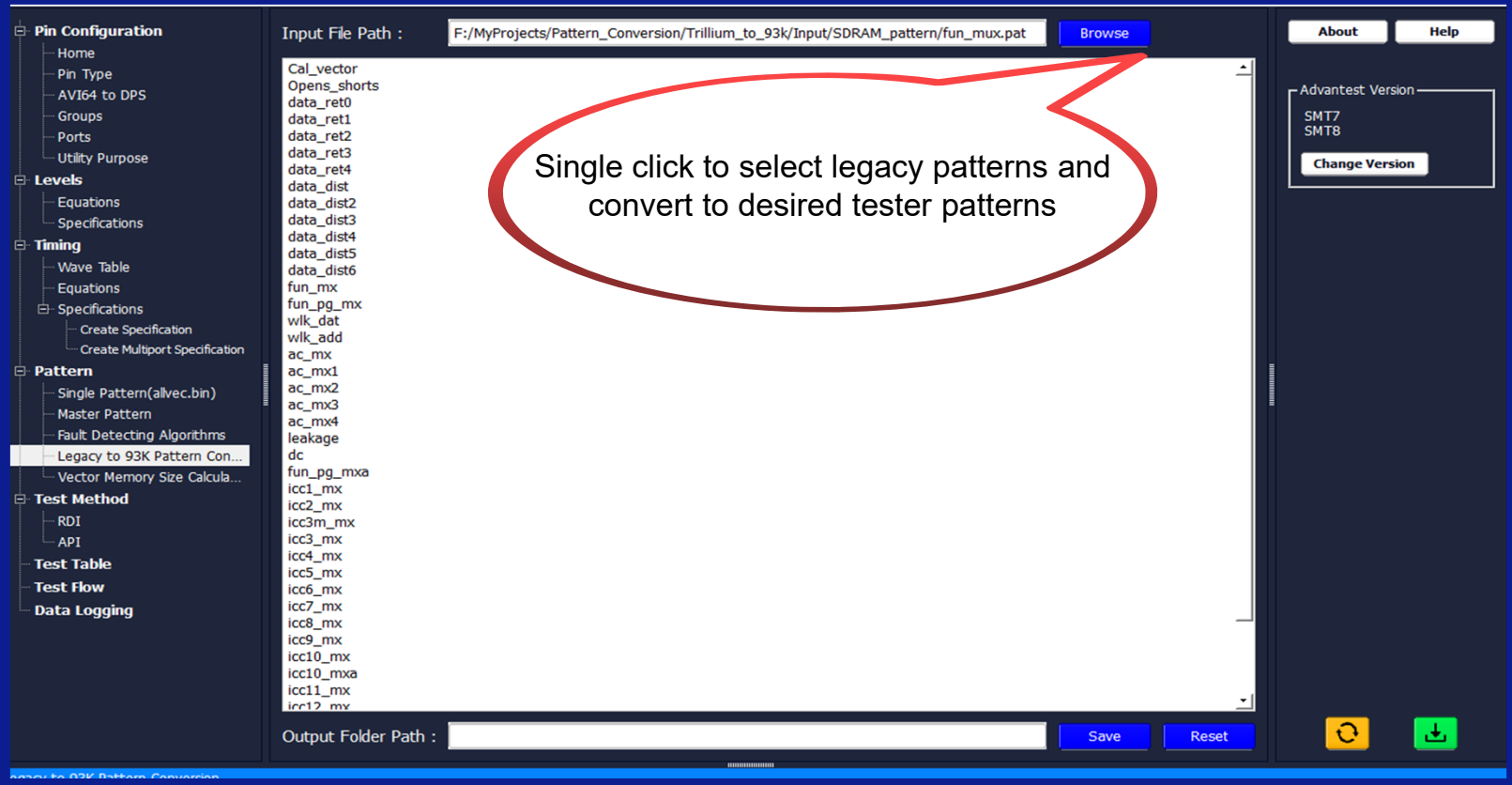
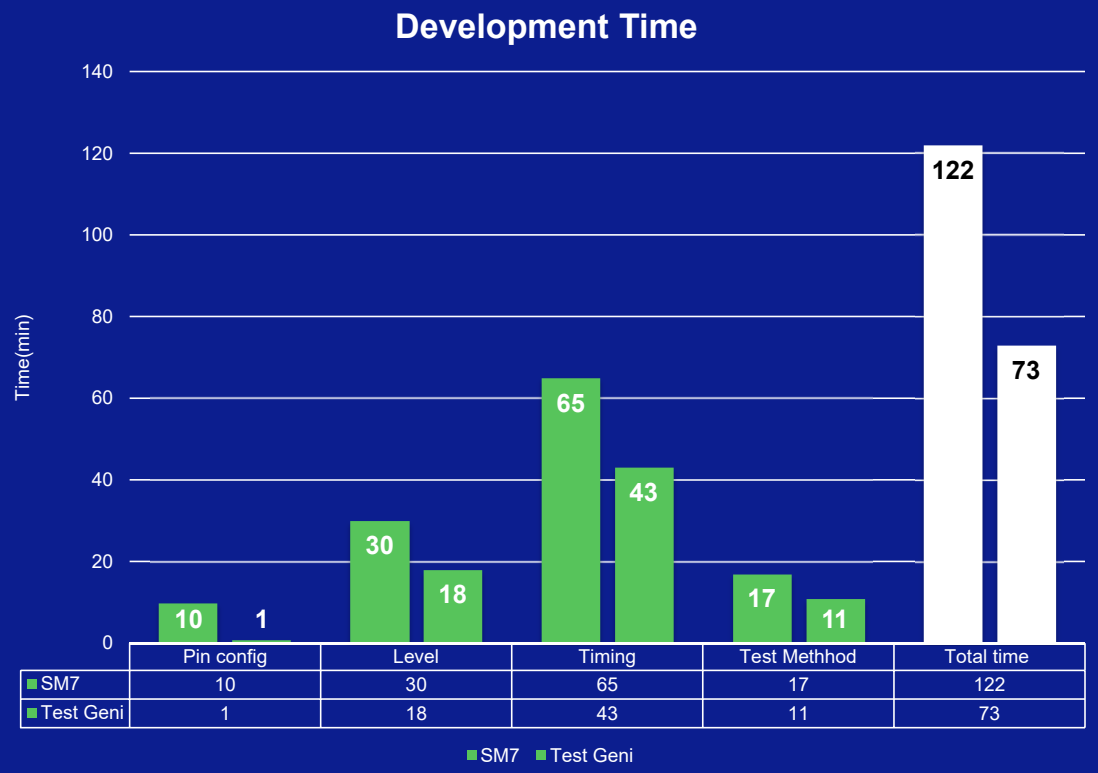
Expeditious Pattern Conversion



On Target

Use Case

- ✓ Digital ASIC
- ✓ Advantest 93000 & their SM7 tool
- ✓ Test Program Dev done using Tester tool & TestGeni for comparison
- ✓ Time saved? ~40%!



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Conclusion and Future Work

- TestGeni helps in automation needed for test program dev and aids in analyzing/reducing the test data to information – to save valuable test engineering person hours
- Incorporating new tester platform(J750, Uflex) for portability & support for additional tester platforms & more advanced features are in progress for greater optimization of time

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