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Moving magnetometer Final Test from Pick-and-Place to Wafer Level test handing

Michael Siebert

AEM Wafer Level Test Solutions

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Virtual ▪ October 26-29, 2021

AEM AFORE Wafer Level Test Solutions

Contents

- Objectives for Final Test
- Common Pick-and-Place process flow
- Optimized process using Wafer Level Final Test
- Wafer Level Final Test Solution
- A comparison
- Conclusions

Definition

Wafer Level Final Test

=

Calibration and Final Test of devices on wafer or strip substrates,

i. e. WL-CSP, BGA, LGA, QFN

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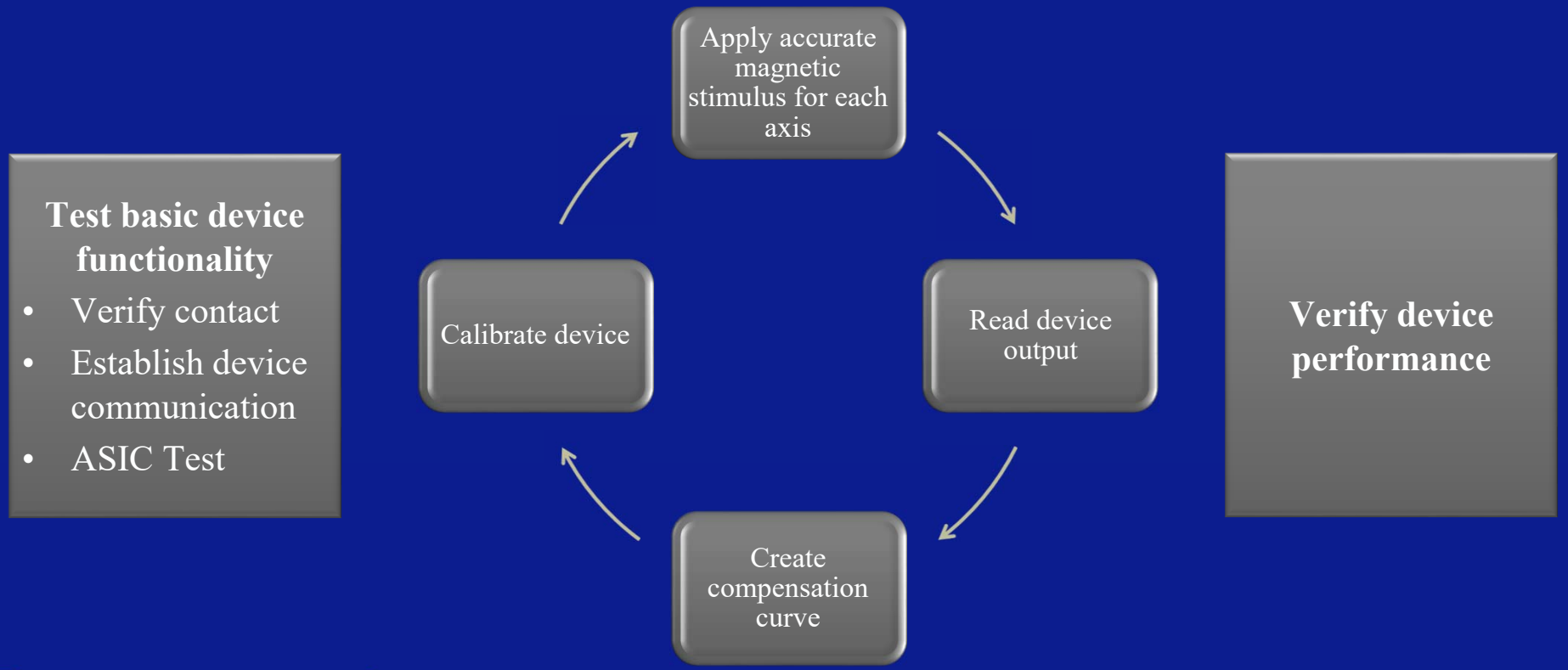
3

Sensor Final Test Objectives



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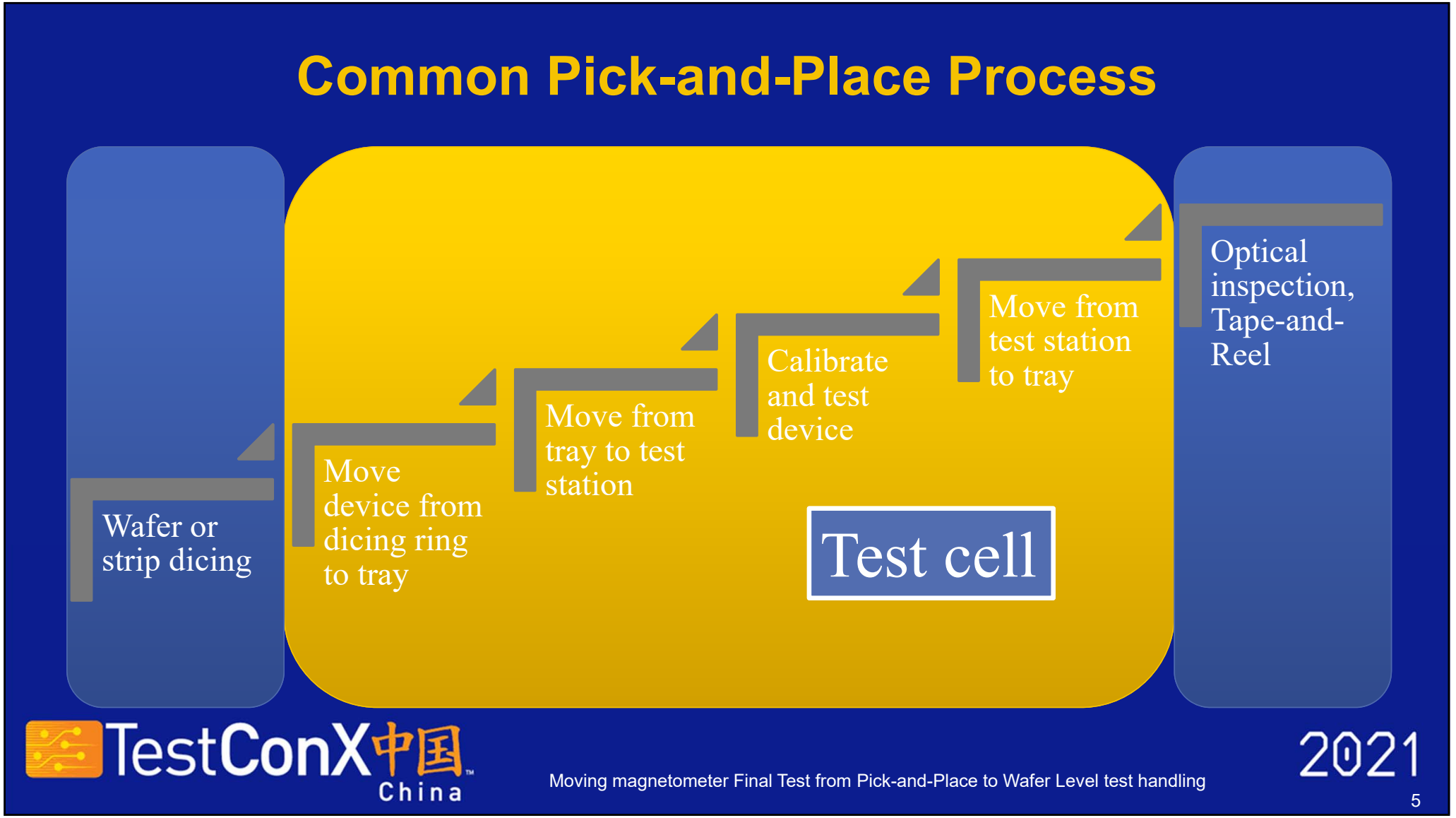
4


Common Pick-and-Place Process
Wafer or strip dicing
Move device from dicing ring to tray
Move from tray to test station
Calibrate and test device
Move from test station to tray
Optical inspection, Tape-and-Reel
Test cell
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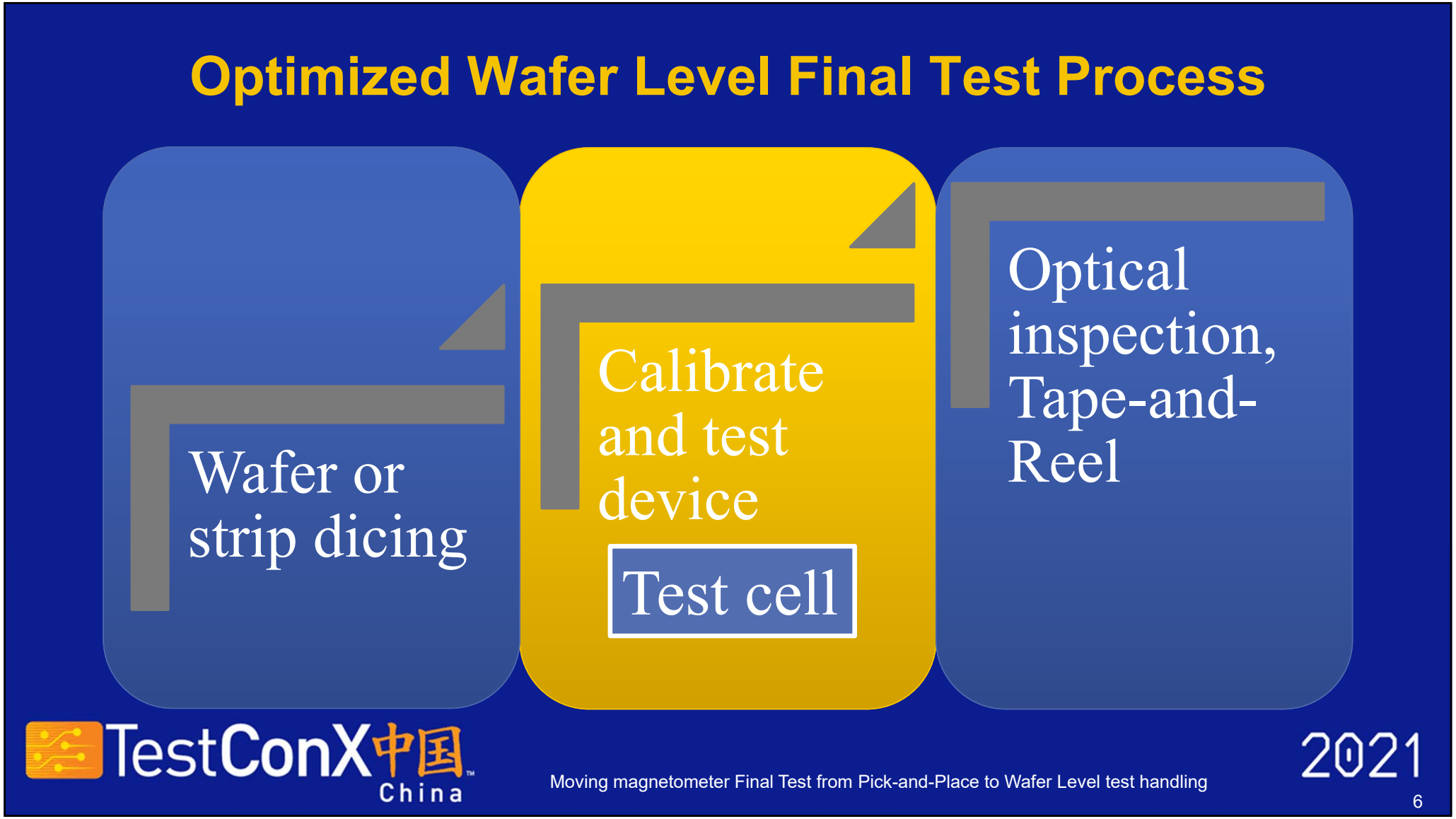
5


Optimized Wafer Level Final Test Process
Wafer or strip dicing
Calibrate and test device
Test cell
Optical inspection, Tape-and-Reel
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Wafer Level Final Test solution

- **Frame-probing station** designed for calibration of application specific devices like magnetometers
- **Capable to handle** wafer rings with **diced wafers or diced strips**
- **Allowing Final Test** of a wide range of packages
- Active alignment for **precise contacting on diced substrates**
- High end **3-axis magnetic stimulus**
- Optional temperature chuck
- Optional ATE and test development

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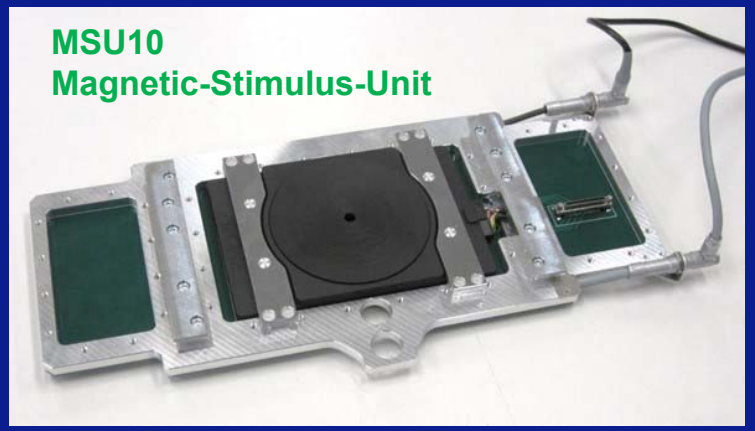
Wafer Level test solution with magnetic stimulus

- **Three axis, 10 mm x 10mm** magnetic field stimulus with integrated background noise reference sensor
- **≤1% homogeneity** across defined field area
- **Compact design**
- Chuck area compensation available



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8

A comparison - relevant variables

Probing of diced substrates	• Displacement of devices after dicing

Stimulus performance	• Stimulus quality
	  • Across contact area
	  • Across wafer / strip area

Units per Hour (UPH)	• Contact parallelism • Load / unload time • Test time
Cost of Test (CoT)	• Initial CAPEX • Change kit and contact device costs • UPH

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Device displacement thru dicing – a concern?

Stress caused by dicing and tape expansion

Major obstacles:

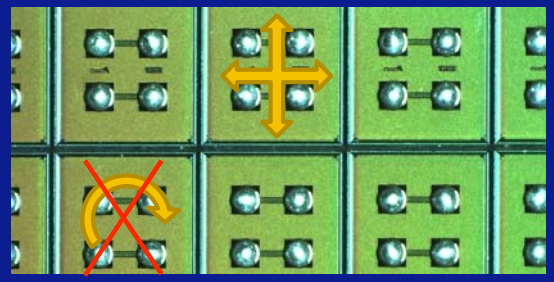
1. Angular dislocation of single devices across wafer
2. X / Y misplacement within one contact area
3. X /Y misplacement across the wafer

Angular displacement

AEM Afore has conducted a large range of measurements of diced wafers and substrates and found

only minor angular dislocations across the wafer

→ Angular compensation is not needed

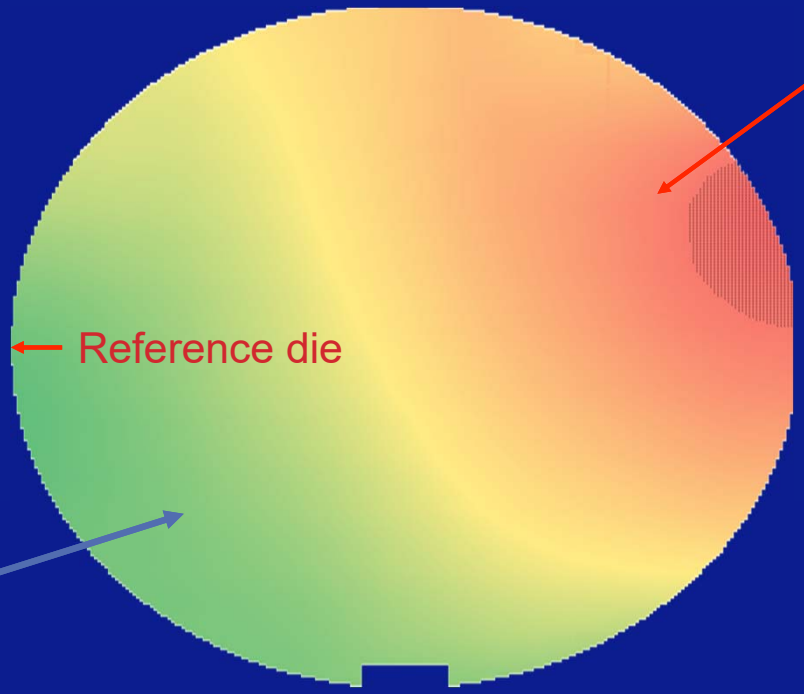


X / Y displacement

Typical x / y dislocation measurement of a 200mm wafer

-0,535	-0,537	-0,539	-0,539	-0,54	-0,541	-0,542	-0,542
-0,534	-0,536	-0,538	-0,539	-0,539	-0,54	-0,541	-0,541
-0,534	-0,536	-0,537	-0,538	-0,539	-0,539	-0,54	-0,54
-0,533	-0,535	-0,537	-0,537	-0,538	-0,538	-0,539	-0,54
-0,533	-0,534	-0,536	-0,537	-0,537	-0,538	-0,538	-0,539
-0,532	-0,534	-0,536	-0,536	-0,537	-0,537	-0,538	-0,538
-0,531	-0,533	-0,535	-0,535	-0,536	-0,536	-0,537	-0,537
-0,531	-0,533	-0,534	-0,535	-0,535	-0,536	-0,536	-0,537

Min: -0,542 mm
Max: -0,531 mm
Range: 0,011 mm



Min: 0,053 mm
Max: 0,061 mm
Range: 0,008 mm

0,061	0,06	0,059	0,058	0,056	0,055	0,054	0,053
0,061	0,06	0,059	0,058	0,057	0,056	0,055	0,053
0,061	0,06	0,059	0,058	0,057	0,056	0,055	0,054
0,061	0,06	0,059	0,058	0,057	0,056	0,055	0,054
0,061	0,06	0,06	0,059	0,058	0,057	0,055	0,054
0,062	0,061	0,06	0,059	0,058	0,057	0,056	0,055
0,061	0,06	0,059	0,058	0,057	0,056	0,055	0,054
0,06	0,06	0,059	0,058	0,057	0,056	0,055	0,054

High parallelism possible with diced substrates

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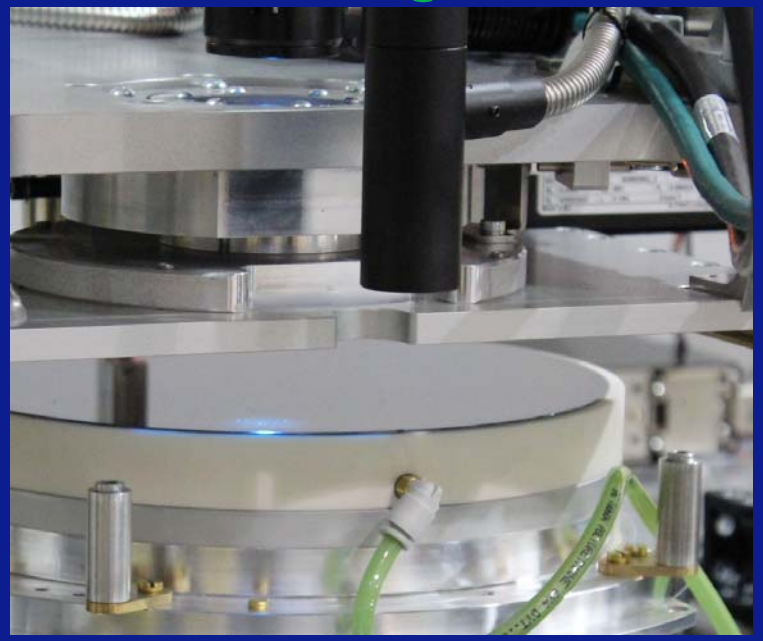
12

Device displacement - summary

Major obstacles:

1. Angular dislocation of single devices across wafer → **OK**
2. X / Y misplacement within one contact area → **OK**
3. X /Y misplacement across the wafer → **Requires action**

Active alignment



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13

A comparison - relevant variables

Probing of diced substrates	• Displacement of devices after dicing

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	  • Across contact area
	  • Across wafer / strip area

Units per Hour (UPH)	• Contact parallelism • Load / unload time • Test time
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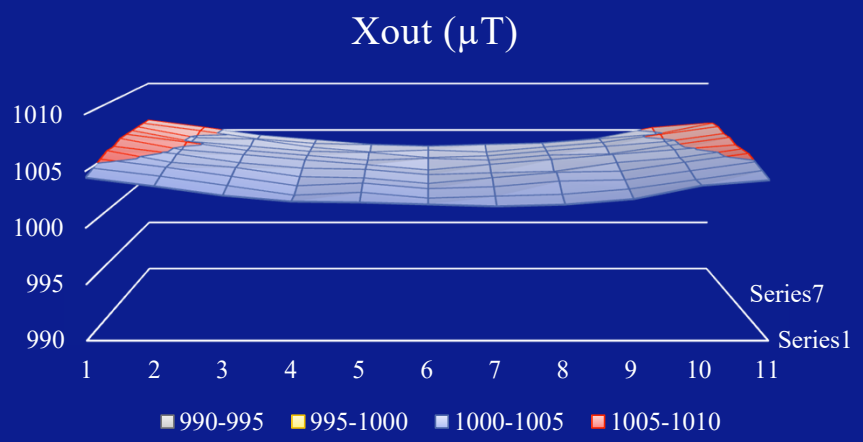
Stimulus performance

Typical field homogeneity
~ 0.5% across 10 x 10 mm²

Typical area homogeneity
depends on local conditions



- Magnetic material inside the system
  -> Remove magnetic material from test area
- Magnetic fields surrounding the system
  -> AEM offers a means to quantify background field and create a calibration table for compensation

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15

A comparison - relevant variables

Probing of diced substrates	• Displacement of devices after dicing	☑

Stimulus performance	• Stimulus quality
	  • Across contact area
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		☑

Units per Hour (UPH)	• Contact parallelism • Load / unload time • Test time	
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UPH and CoT

	Pick-and-Place + Tape-and-Reel	Wafer-Level + Tape-and-Reel
Parallelism	256	64
Test time	36 seconds	25 seconds
Unit per Hour UPH	25k (100%)	20k (80%)
Output per month	12,5M (100%)	10M (80%)
Amortization period	5 years	
Monthly operating hours	500	
CAPEX	100%	43%
Cost of Test (CoT)	100%	55%
Change kit required	Yes	No
Contact head required	Yes	Yes

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17

A comparison - relevant variables

Probing of diced substrates	• Displacement of devices after dicing

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18

Conclusions

- High multi-site factors can be achieved after dicing
- High parallelism does not guarantee low Cost of Test
- Wafer Level Final Test can be an attractive alternative to the traditional Pick-and-Place approach
- Be open to alternative test approaches and process flows

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