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The Trouble with Wide-Bandgap Semiconductors

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Teradyne

TestConX 中国 China

Virtual ▪ October 26-29, 2021

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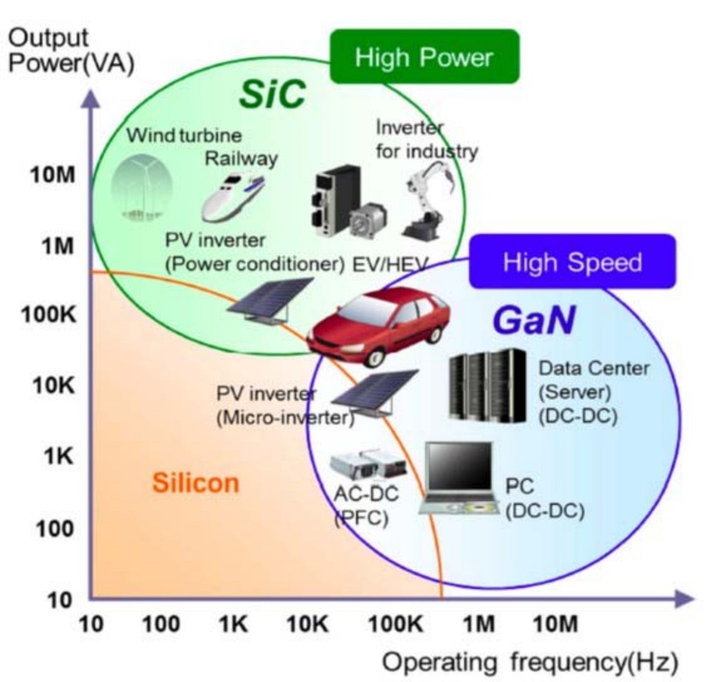
Agenda

- What is a wide-bandgap semiconductor?
- Testing FETs
  - Testing Wide-Bandgap Devices
- RDSON
  - Dynamic RDSON
  - Quality challenges
- Measurement Challenges
  - Switching Speeds
- Measurement Path
- Intrinsic Characteristics
- Gate Driver

What Is a Wide-Bandgap Semiconductor? Why Should We Care?

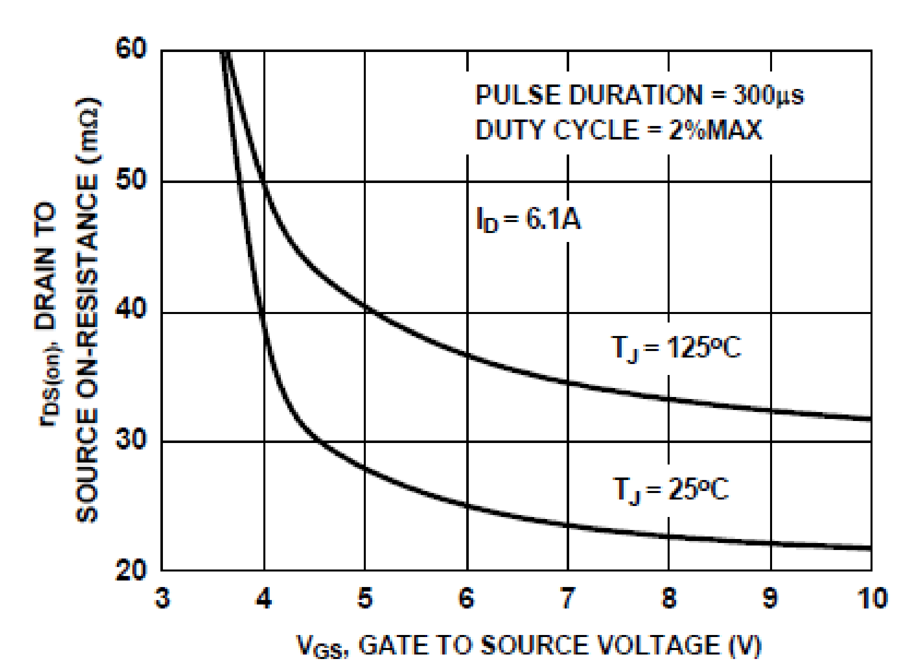
- Band-Gaps in the 2-4eV range (higher than Si)
- Functionality at higher voltage, higher current, higher temperature, and higher frequency
- **Higher efficiency power conversion**



From Georgia Tech's Graham Lab

Before Using a FET, Can We Prove It Works? Traditional RDSON

- Apply a voltage across Gate-Source
- With a given current source, ID, measure the voltage drop across Drain-Source
- RDS(on) = VDS / ID
EASY!



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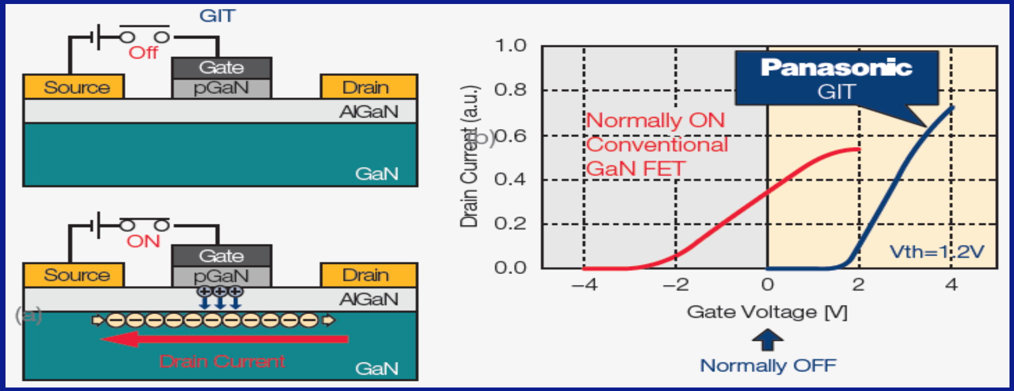
Can We Prove A Wide-Bandgap Device Works?

New processes come with new problems

- Current collapse due to dislocations from thermal coefficient between epitaxy layers
- Detected with Dynamic Rdson



From Keysight Pathwave case study, in conjunction with Panasonic, 2019, 5992-2752EN

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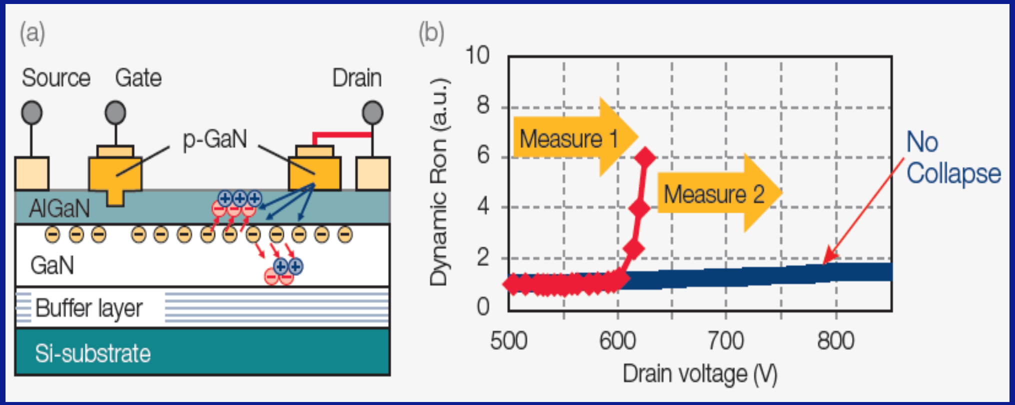
Adding the Cascode FET to Prevent Current Collapse

Process improvements can mitigate challenges

- High energy electrons trapped by dislocations, interfering with functionality (Measure 1)
- Cascode FET to inject holes to recombine with electrons (Measure 2)



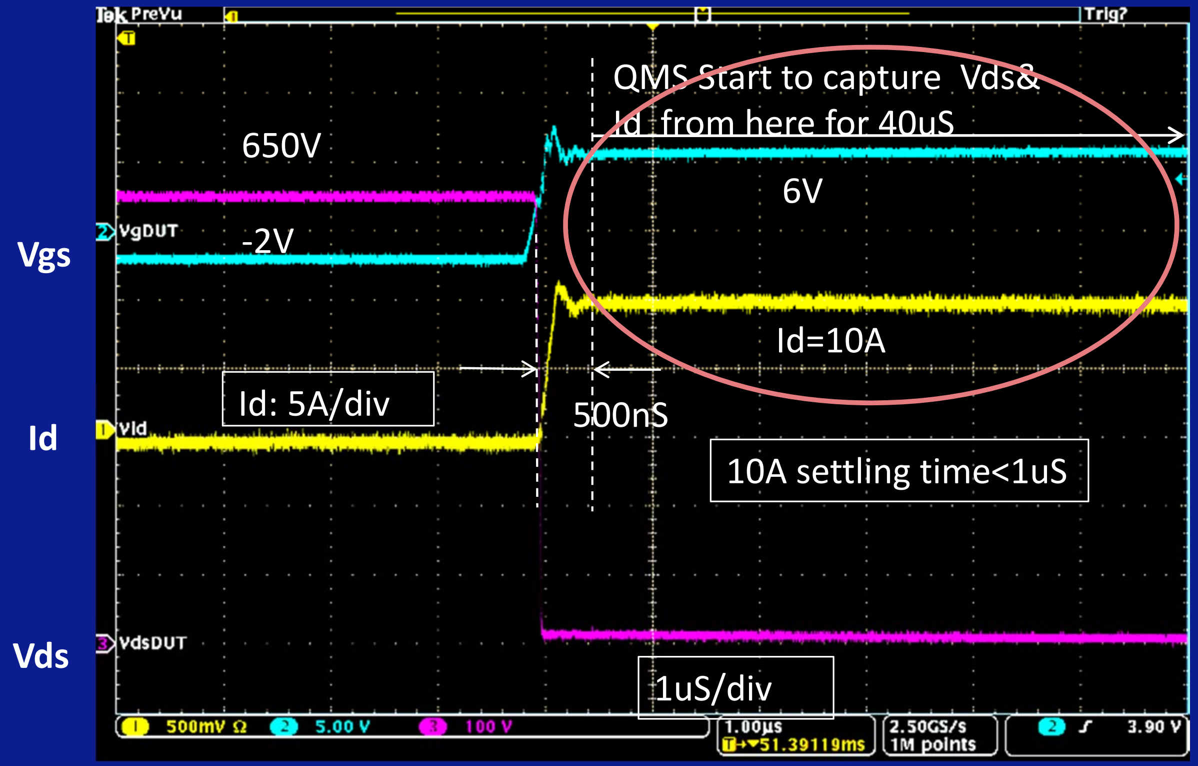
From Keysight Pathwave case study, in conjunction with Panasonic, 2019, 5992-2752EN

Quality Challenge - GaN Dynamic Rdson

Testing Soft Switching

- Time between stress voltage and Rdson measurement set by relay switching

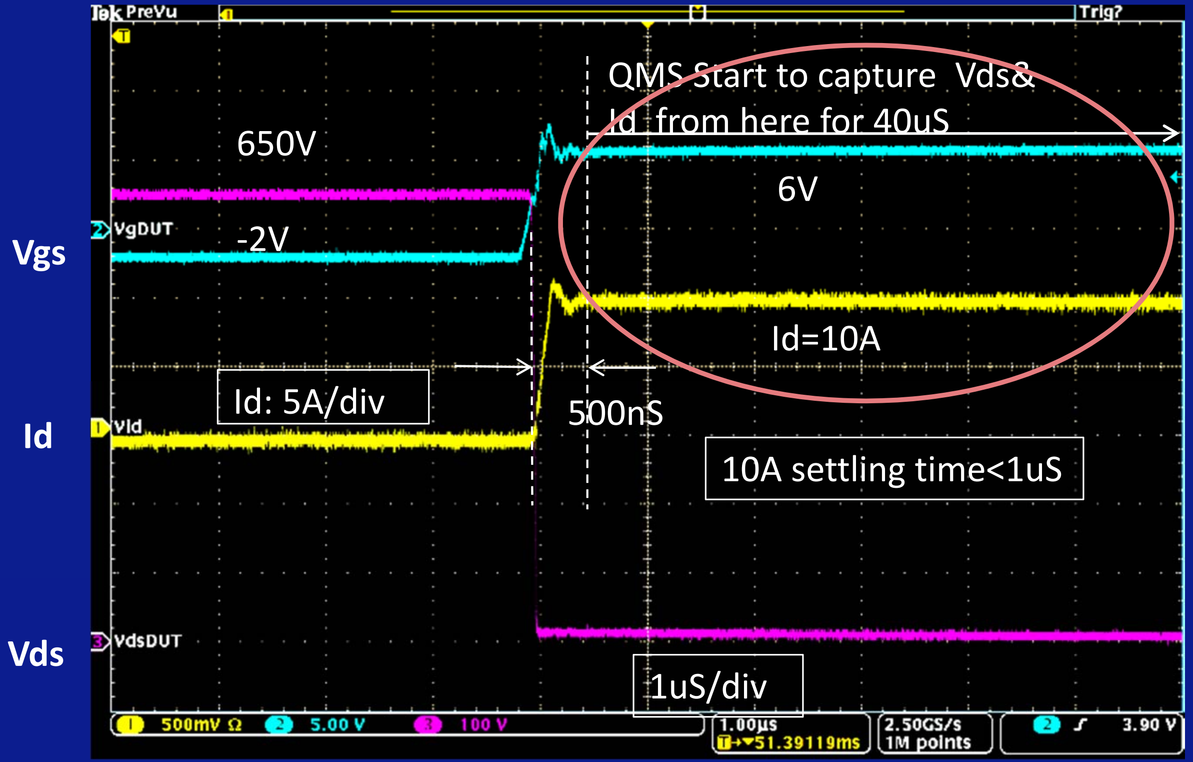
1. Trapped charge causes Rdson to be high after stress
2. Charge can dissipate quickly, or can last until UV exposure (current collapse effect)



Quality Challenge - GaN Dynamic Rdson

Testing Hard Switching

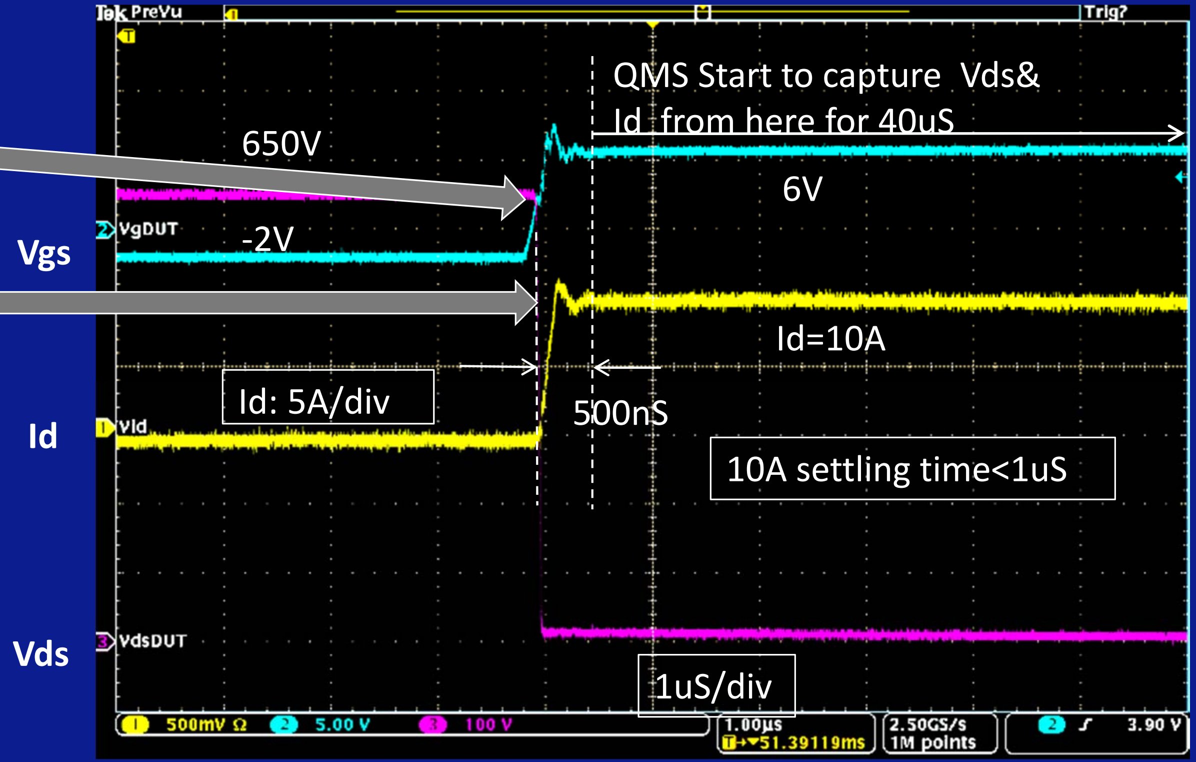
- Time between stress voltage and Rdson measurement as close to stress transition as possible (<1usec)
- Temperature and correlating Soft Switching and Hard Switching Rdson



Measurement Challenge - Switching Speed

Gate Control
- Limits switching

Parasitic Inductance
- Managing overshoot
- Minimizing unstable Id period



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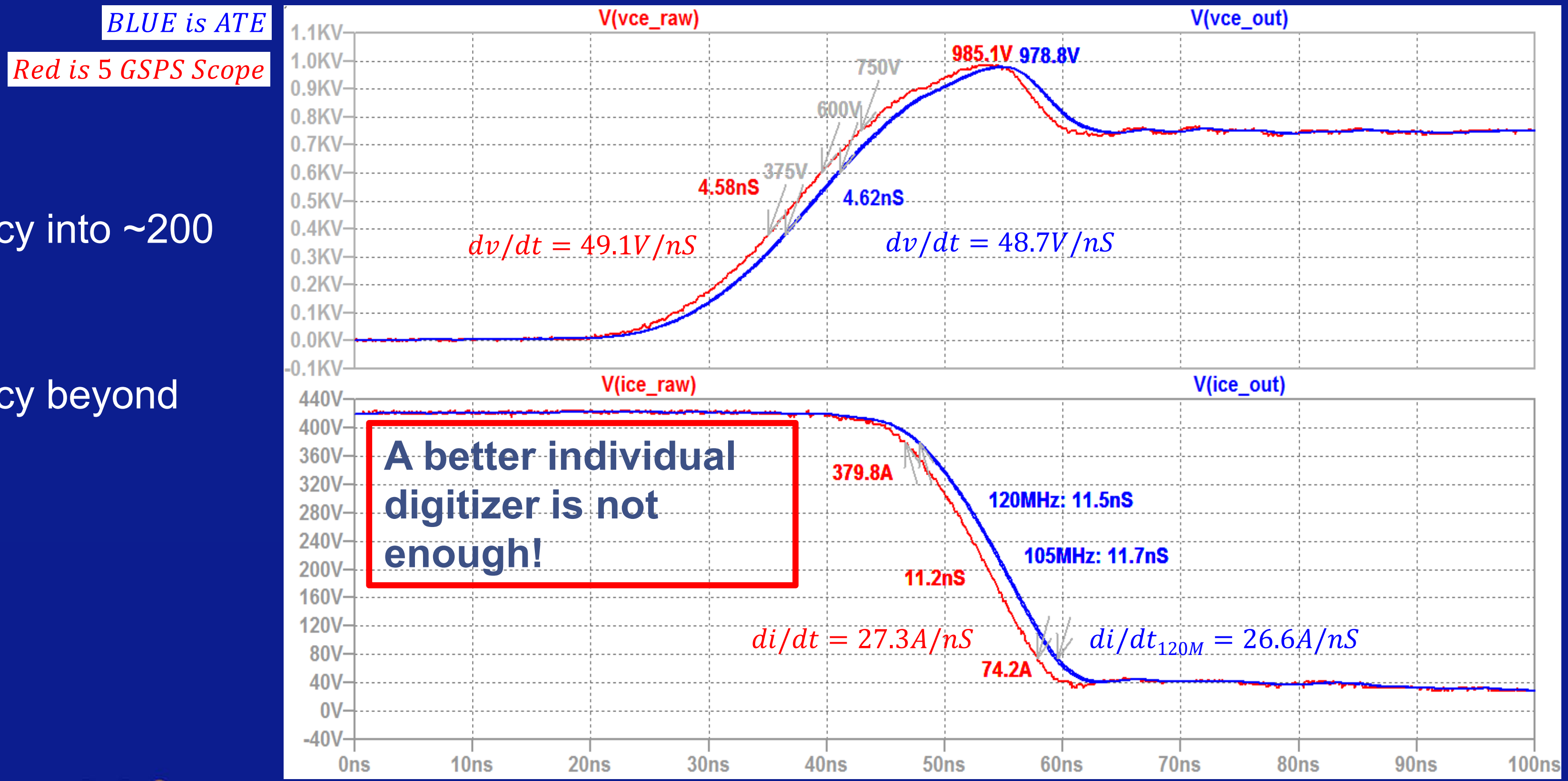
Increased switching speeds require a better digitizer *system*

SiC FET
- Peak efficiency into ~200 KHz

GaN FET
- Peak efficiency beyond SiC



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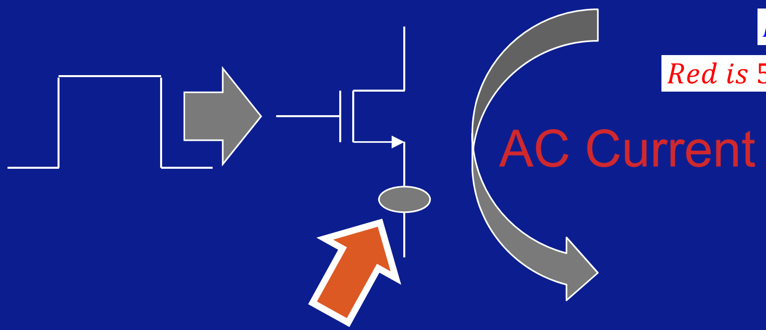
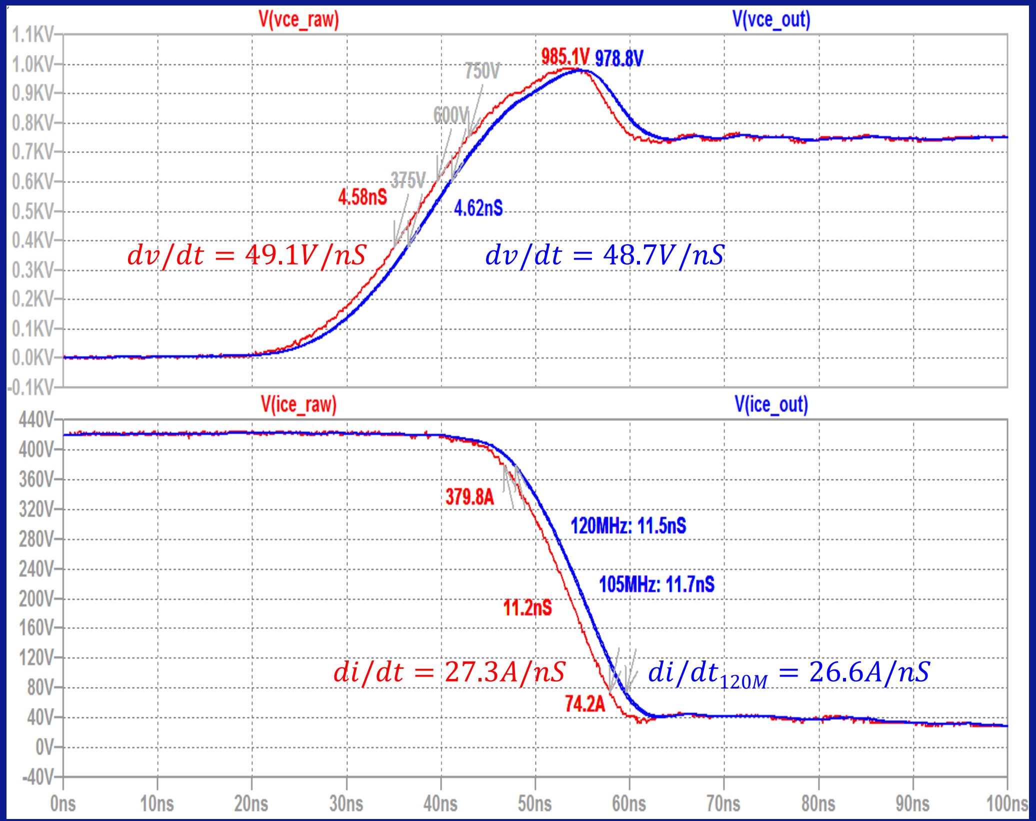
Measurement Path Limits Edges



BLUE is ATE

Red is 5 GSPS Scope



What happens if current sensor or divider path to digitizer does not have as much bandwidth?

- di/dt and dv/dt will exhibit slow down compared to direct measure
- Leads to difference between ATE and Bench
- Influences device specifications

Why not just use the scope?

- Does this effect test time?
- Does the wiring have a clean path to DUT?

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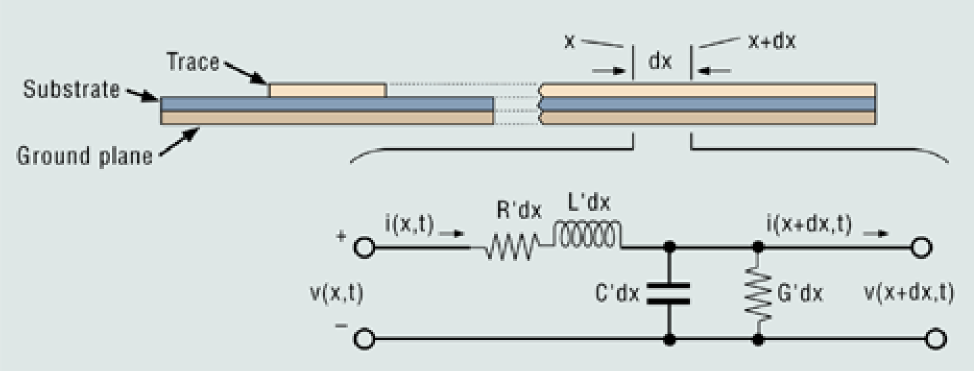
Every Path Is a Collection of Parasitics

DUT to digitizer can be a challenge to guarantee a high bandwidth path since every via and layer overlap runs the risk of adding inductance and capacitance

Even simple cabling down to a DUT can exhibit abnormally high parasitics for an oscilloscope



EDN - High Speeds and Fine Precision Knock PCB Traces Off Pedestal, 2000

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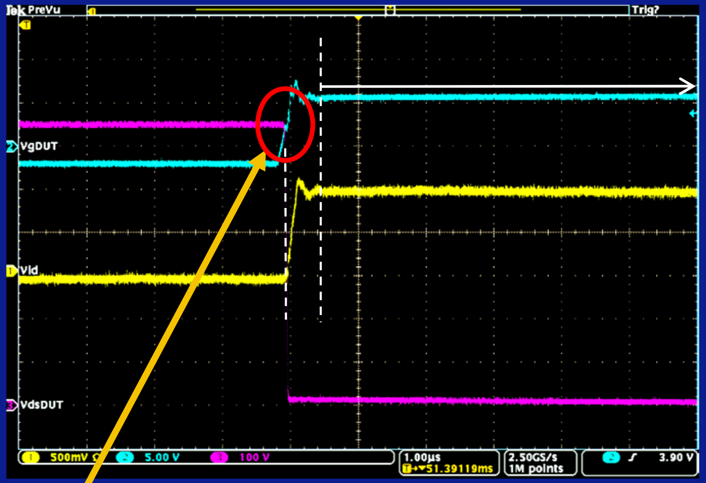
Intrinsic Characteristics Can Also Pose a Challenge

Pulse Gate Current
- Pulse can be significantly higher than average
- Some require some gate current for ‘on’ state

Gate Charge
- Narrow Cgd (Miller Plateau) in SiC and GaN vs Silicon
- Faster switching
- Gate has to be driven negative to turn off device

Leakage Currents
- Typically higher than expected



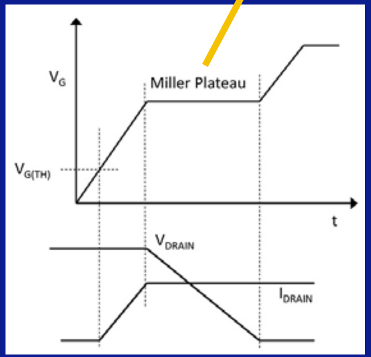
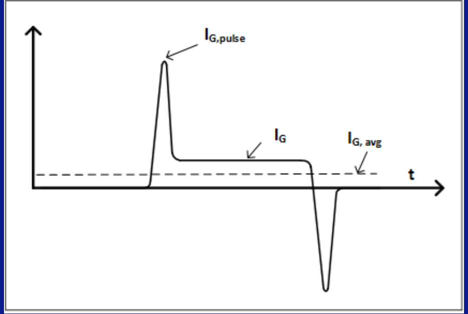


Figure 27 Gate current switching waveform



The Gate Driver Gains Greater Importance

Gate Driver Requirements

- Isolated, but also span negative and positive voltage relative to common mode
- Provide high pulse current and still be able to provide several milliamps of on-current
- Drive low gate resistances
- In a test environment, provide some ramp control (Vth) or dedicated current drive (Qg)

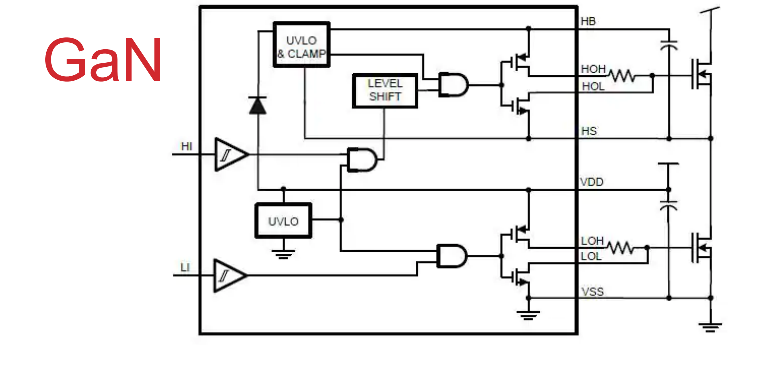
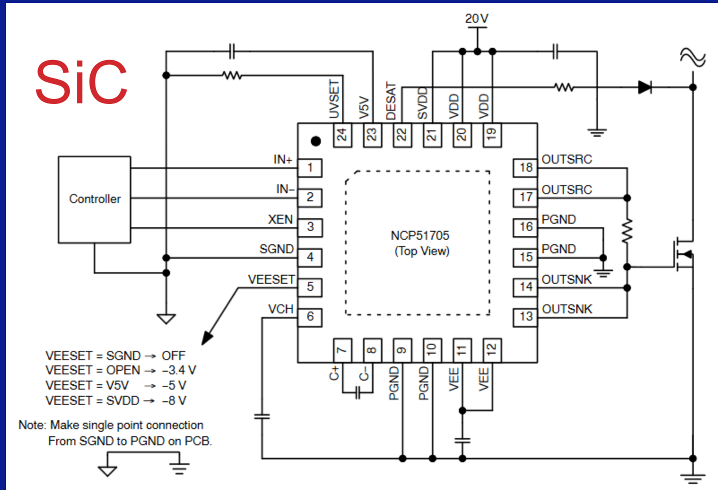


Figure 1: Optimized to drive both high- and low-side eGaN FETs, TI's driver LM5113 offers separate sink and source outputs.



(a) Low Side Switching Configuration

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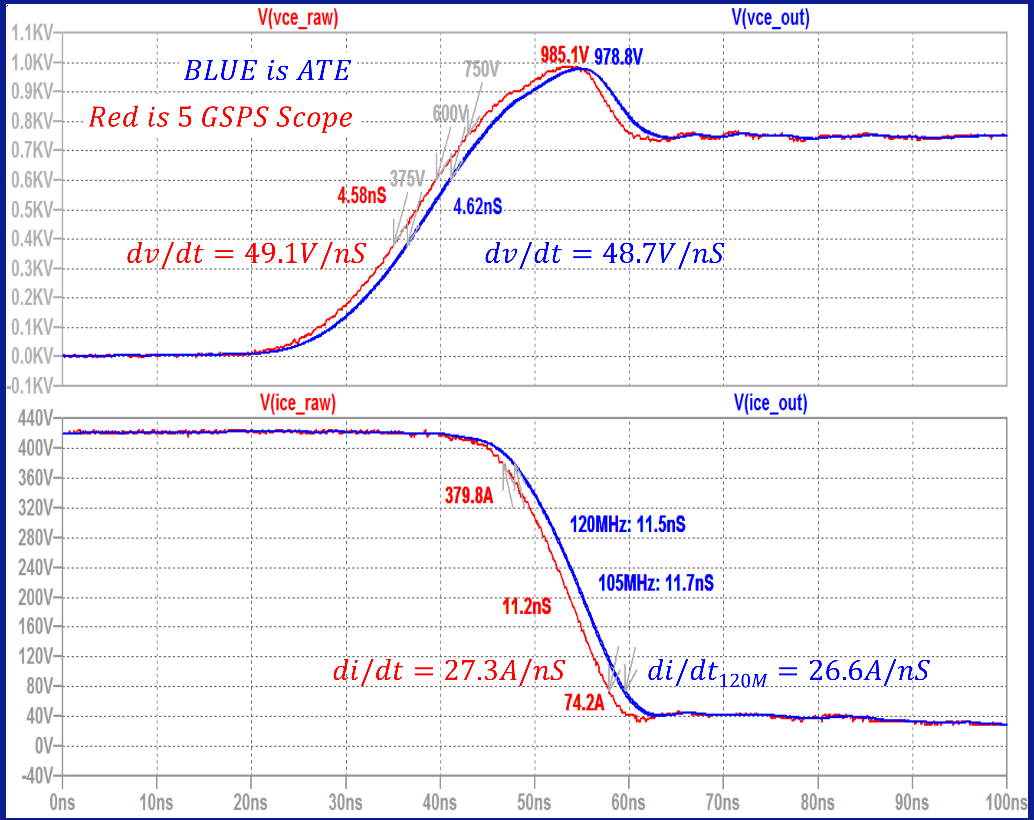
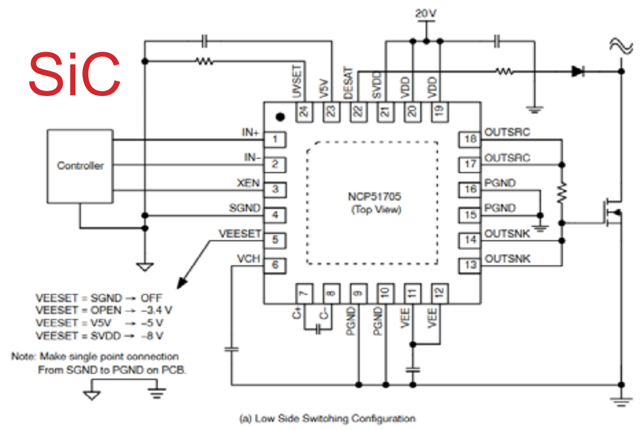
AC Testing Requires the Fastest Possible Slew





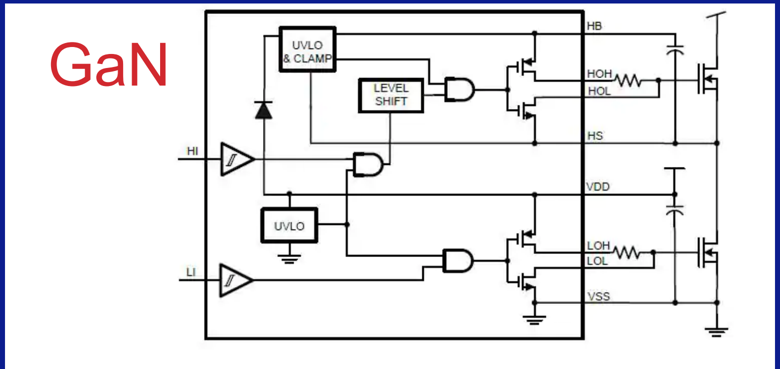


Figure 1: Optimized to drive both high- and low-side eGaN FETs, TI's driver LM5113 offers separate sink and source outputs.

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GaN Still Has Another Trick-Reverse Conduction

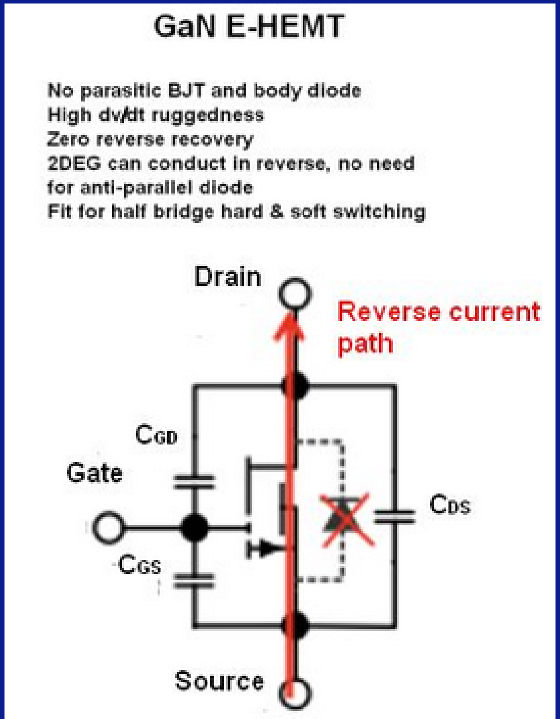
No Body Diode

- Not needed and can badly influence efficiency

Conduction in the 3rd Quadrant

- $V_{gd} = V_{sd}$ is greater than V_{th} (simplification)
- V_{gs} at 0.0V

Important for efficiency, and gives a measure for GaN resistance



Power Electronics Tips, Oct. 2017

New Processes Always Require New Effort

- Catching Process Problems
  - Dynamic Rdson
- Higher speed switching in power devices
  - Requires better design and sensing
  - Digitizer system
- Intrinsic differences
  - Require adaptations of existing techniques and designs

References

We are excited to face the challenges of wide-bandgap device testing with you!

Citations:

Slide 3 Image - http://grahamlab.gatech.edu/research-2/ultra-wide-band-gap-semiconductor-materials/

Slide 4 Images - Keysight Pathwave case study, in conjunction with Panasonic, 2019, 5992-2752EN

Slide 12 Image - EDN - High Speeds and Fine Precision Knock PCB Traces Off Pedestal, 2000

Slide 17 Image - https://www.powerelectronictips.com/common-misconceptions-about-the-mosfet-body-diode/

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