VIRTUAL EVENT

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A New Desktop Socketing Approach to Boost Operating Frequencies

Emad Al-Momani, Kevin Doran, Cory Mason, Hayley Klug

Intel Corporation

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Virtual Event • May 3 - 7, 2021

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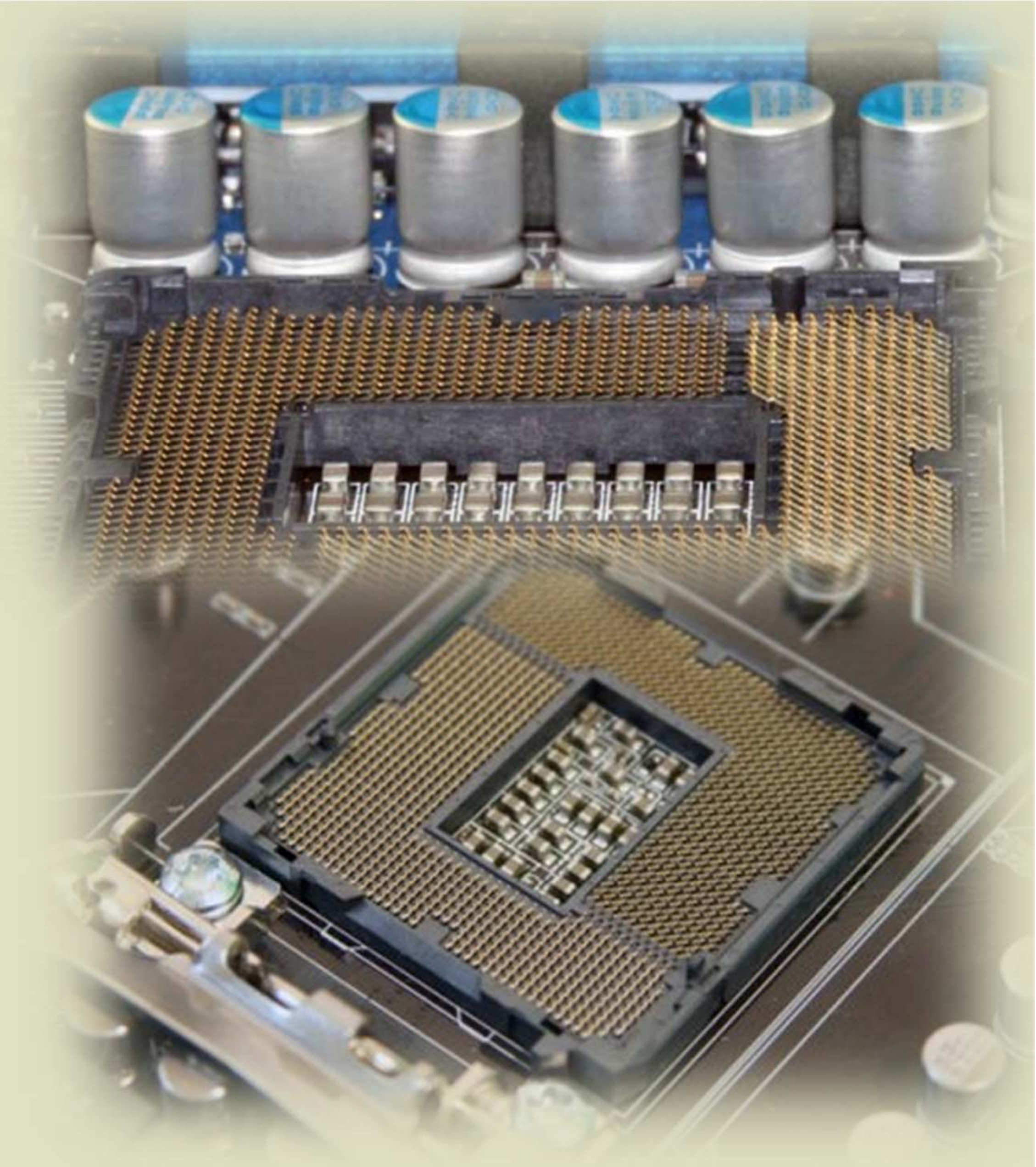
- Problem statement
- Description of the second level interconnect (SLI)
- Current desktop LGA socket and potential socket options
- Test board modifications
- Socket's performance comparison
- Summary

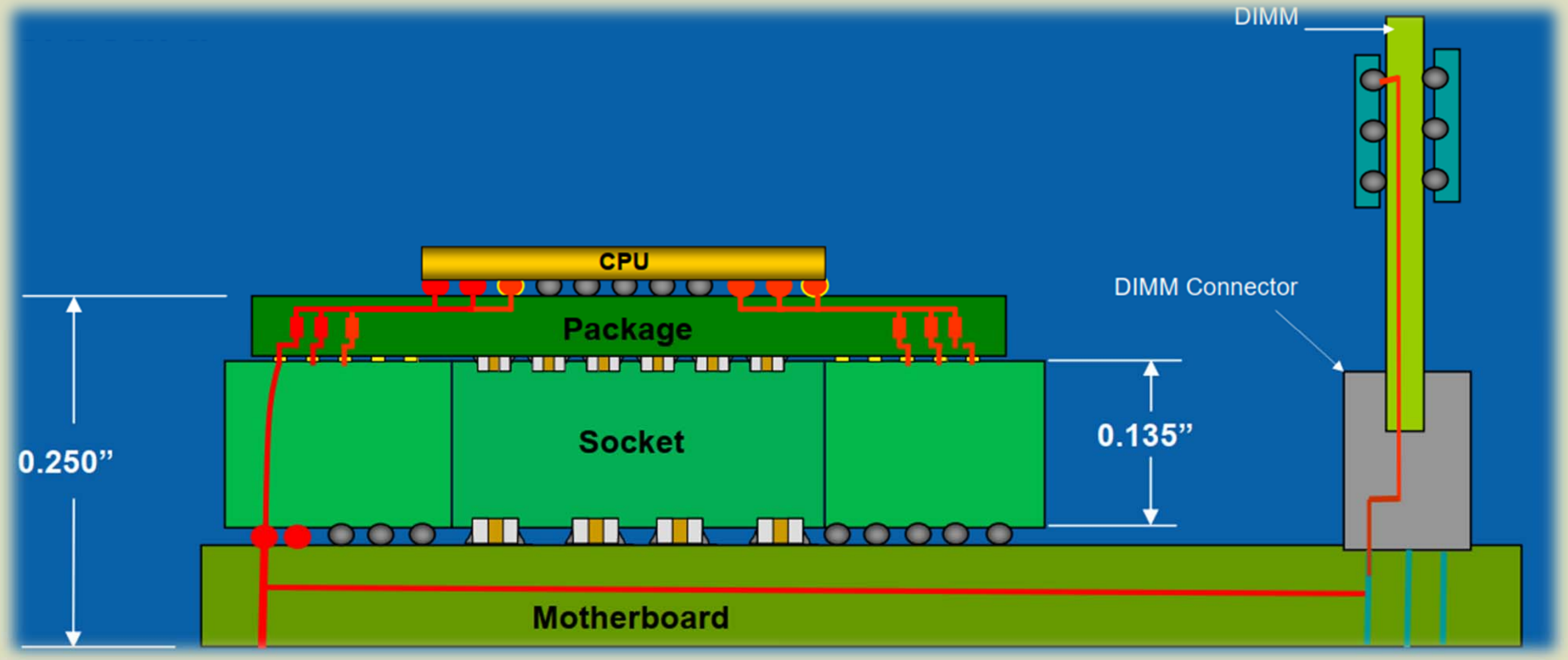
Problem Statement

- Current OEM LGA socket technology is based on cantilever pins that is ~ 3.00mm in height
- The height of the cantilever pins has led to concerns about the sockets' electrical performance on future products, especially for high frequency memory access.



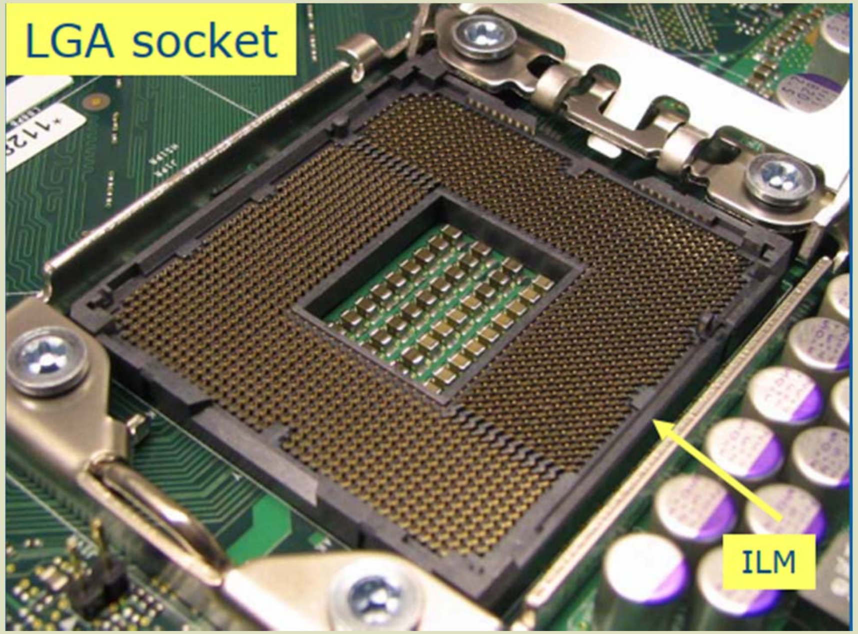
Second Leve Interconnect (SLI)

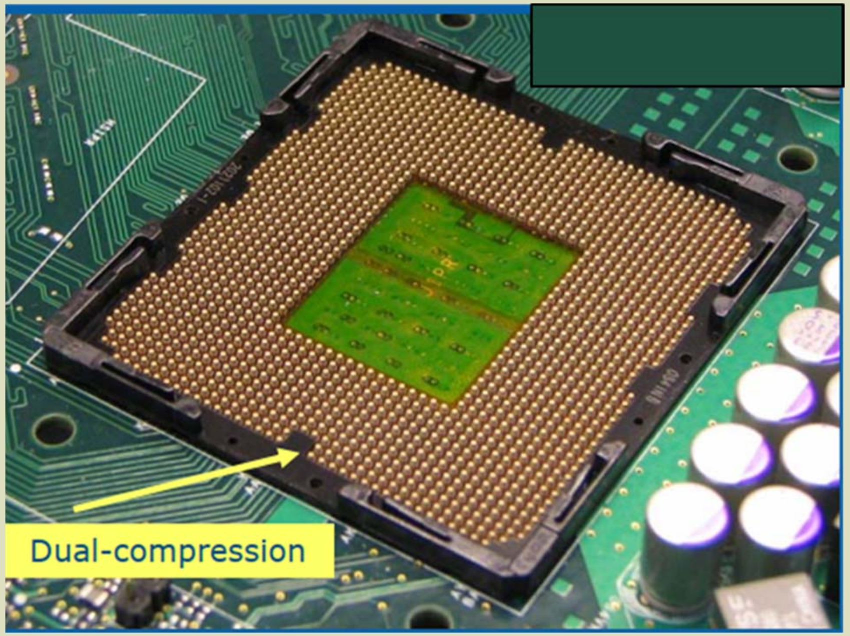
- SLI Components
  - Package
  - Socket
  - Motherboard

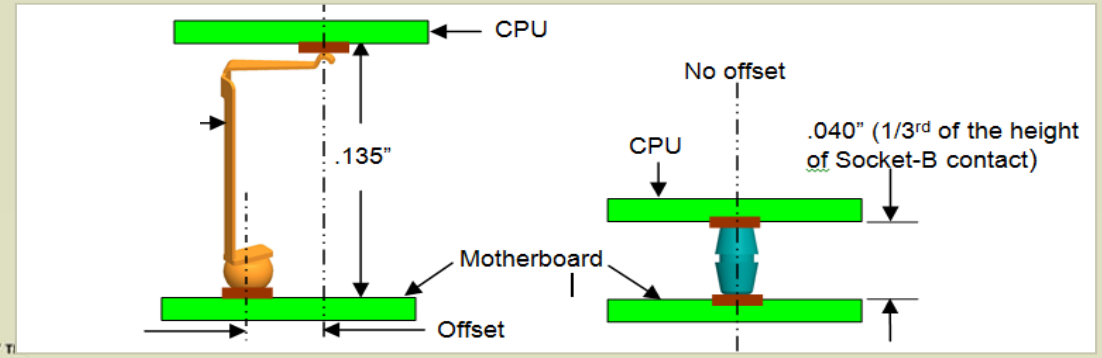


The socket occupies about 50% of the total vertical SLI components stack height

Socket Comparison

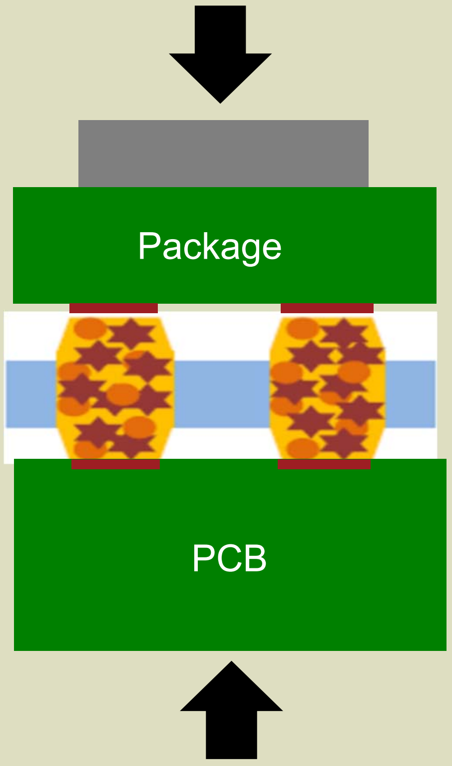


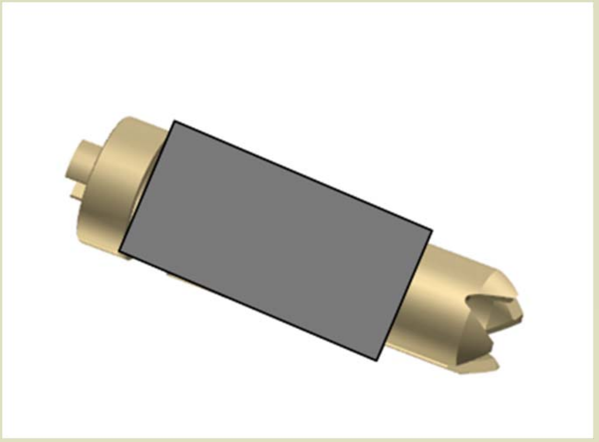




Elastomer and Sogo-pin

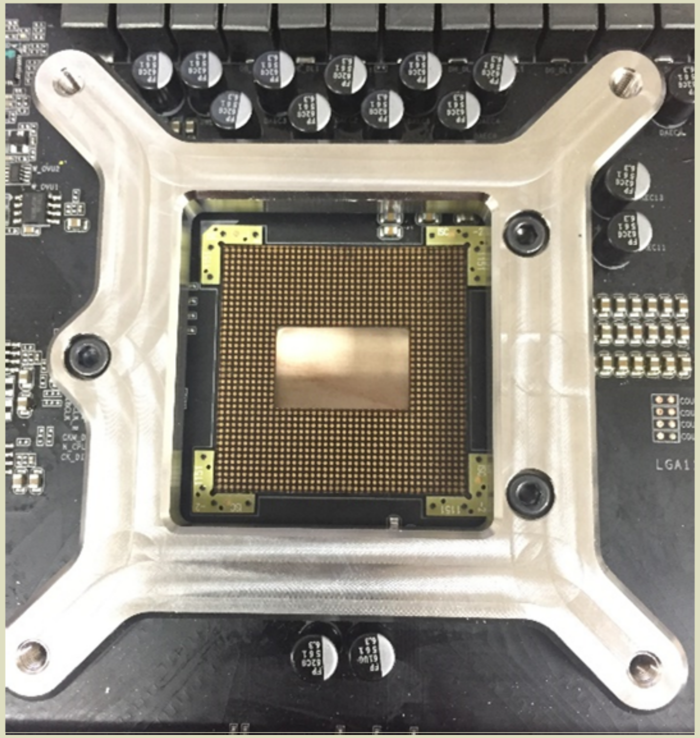
- Dual compression type sockets
- Elastomer pin consists of metal partials suspended within a silicon rubber body
- Single piece stamped and rolled pin (Sogo-pin) is an economic metal pin option

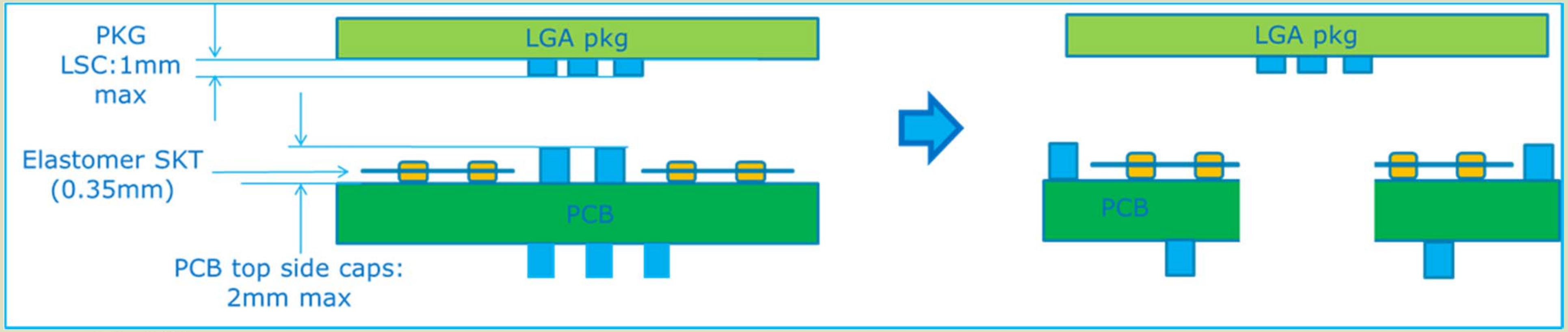




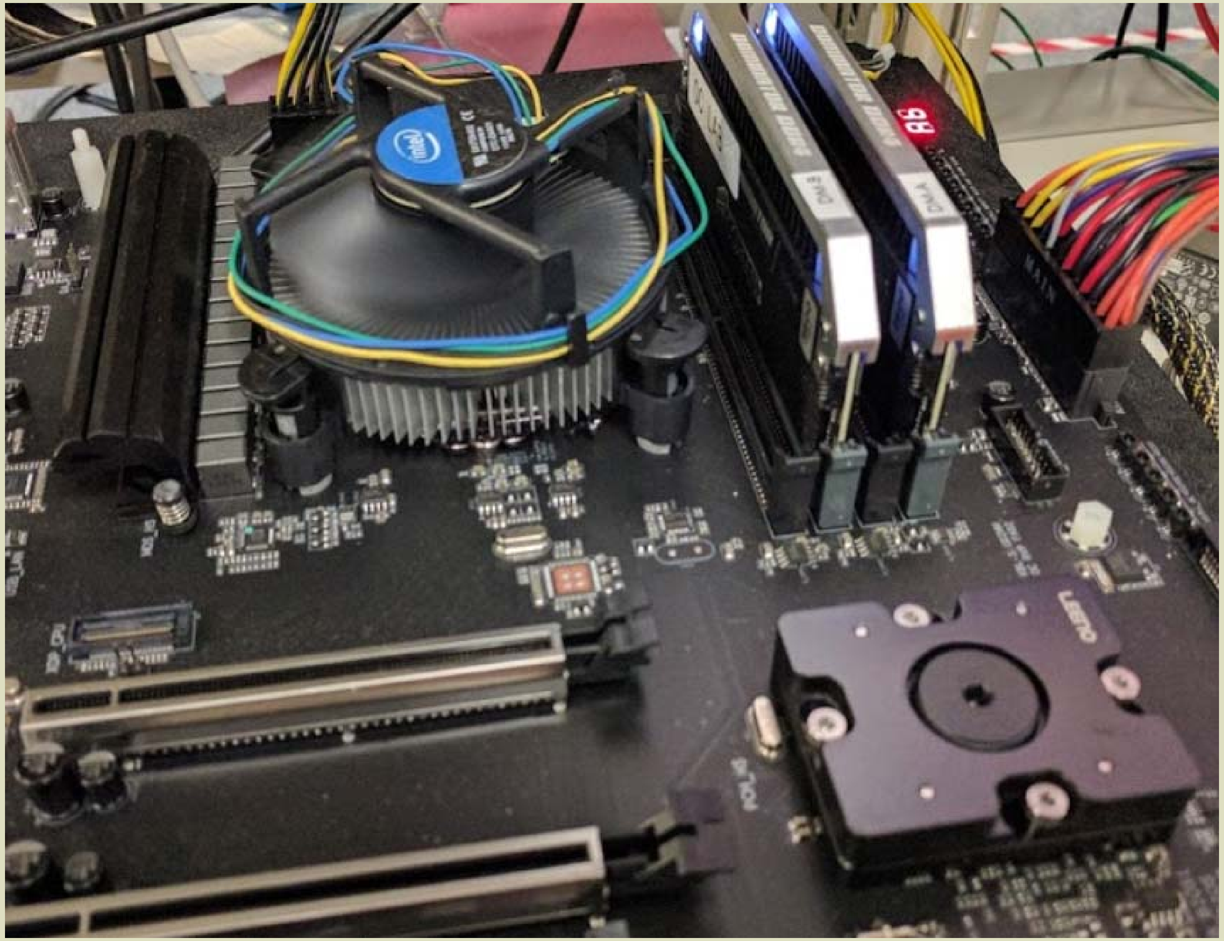
Test Board Modifications

- Package/PCB offset removal
- A hole was cut in the PCB and caps were moved to the secondary side

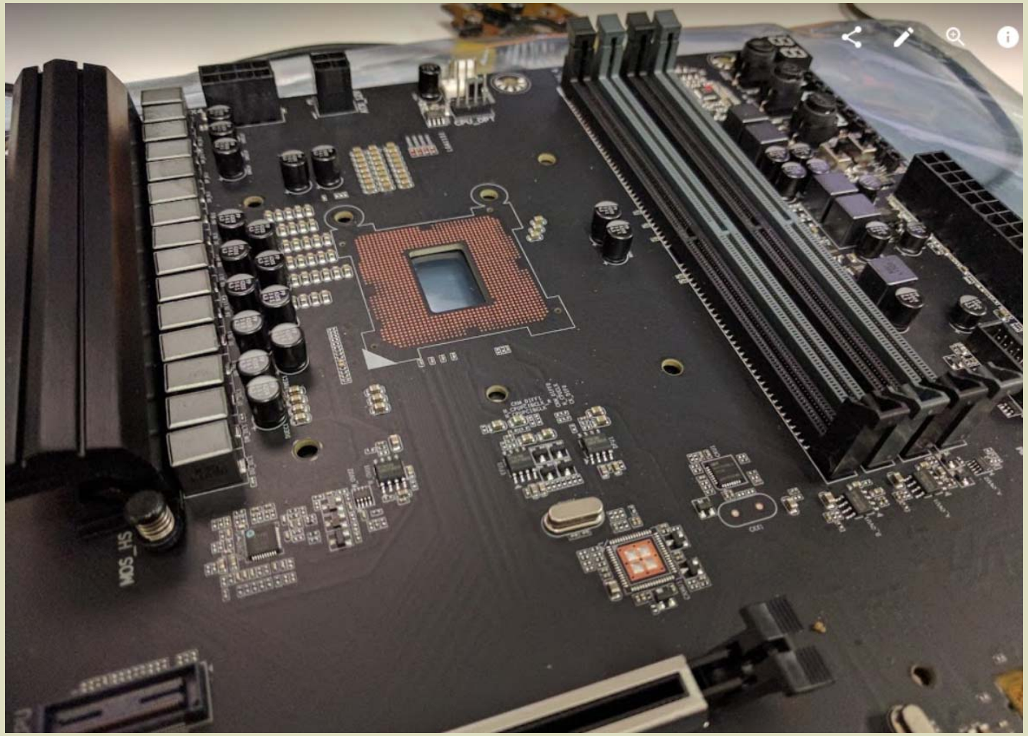


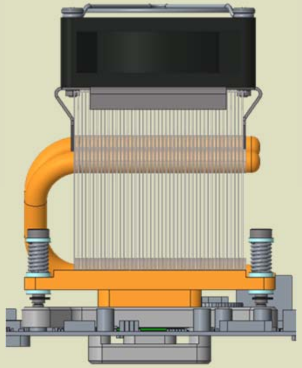


Is this the Real Life…



Is this just Fantasy…





LGA Socket Technology Qualification Scope

- Functional Testing
  - Quantify the added advantage relative to current baseline
  - Platform was modified to overcome interference challenges caused by the lower socket profile

- Reliability Testing
  - A full suite of reliability testing is planned
  - Following Intel and the industry standards such as those by Electronic Components Industry Association (ECIA)
  - Some results may be shared in future events

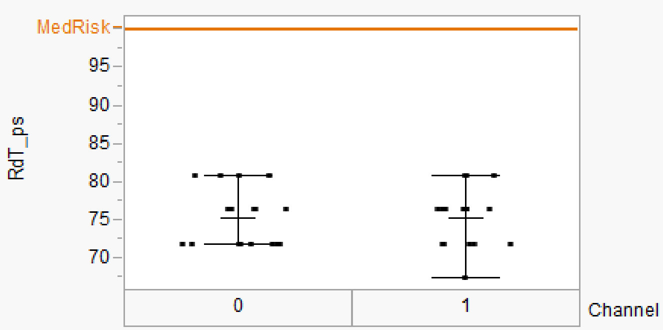
Baseline RMT (LGA only)

- Boards functional @3467MT/s
- DQ measurements are repeatable
  - Std dev is low enough
  - RdV std dev little higher, OK
- Cmd T/V are not repeatable

- *Note: EV Risk table →
- Timing tick = UI/64 = ~4.5ps
- RdV/CmdV tick = Vref/192 = ~3.
- WrV tick = ~7.8mV

Low Risk	>=120ps/mV
Med Risk	120< x >=100ps/mV
High Risk	<100ps/mV

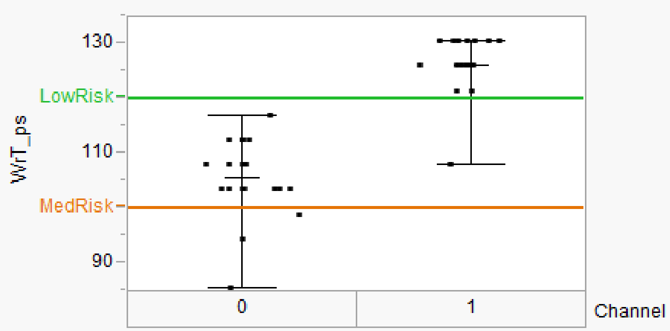
Variability Chart for RdT_ps



Variability Summary for RdT_ps

	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%	Mini
RdT_ps	75.34615	3.681665	0.589538	74.1527	76.53961	
Channel[0]	75.375	3.828133	0.855997	73.58338	77.16662	
Channel[1]	75.31579	3.625567	0.831762	73.56832	77.06326	

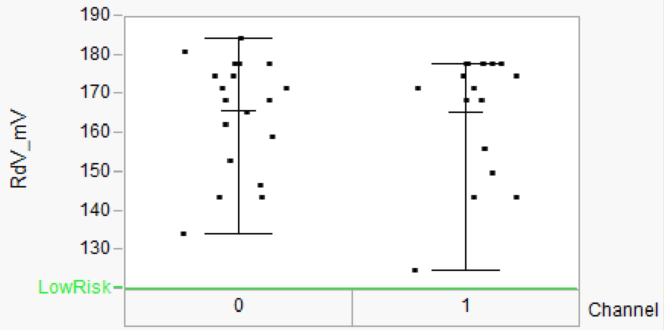
Variability Chart for WrT_ps



Variability Summary for WrT_ps

	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%	Mini
WrT_ps	115.6154	12.17821	1.950074	111.6677	119.5631	
Channel[0]	105.525	7.073812	1.581752	102.2144	108.8356	
Channel[1]	126.2368	5.297715	1.215379	123.6834	128.7903	

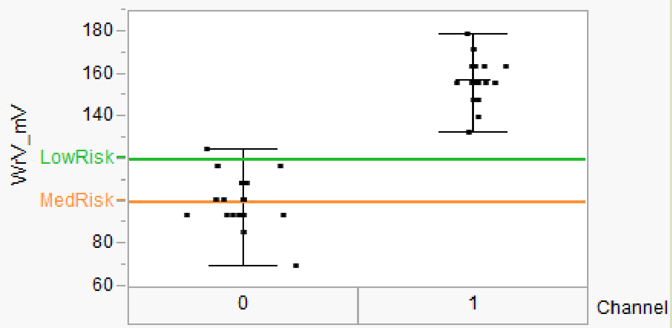
Variability Chart for RdV_mV



Variability Summary for RdV_mV

	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%	Mini
RdV_mV	165.7853	14.5157	2.324372	161.0798	170.4907	
Channel[0]	165.9375	14.47761	3.237292	159.1618	172.7132	134
Channel[1]	165.625	14.95073	3.429933	158.419	172.831	

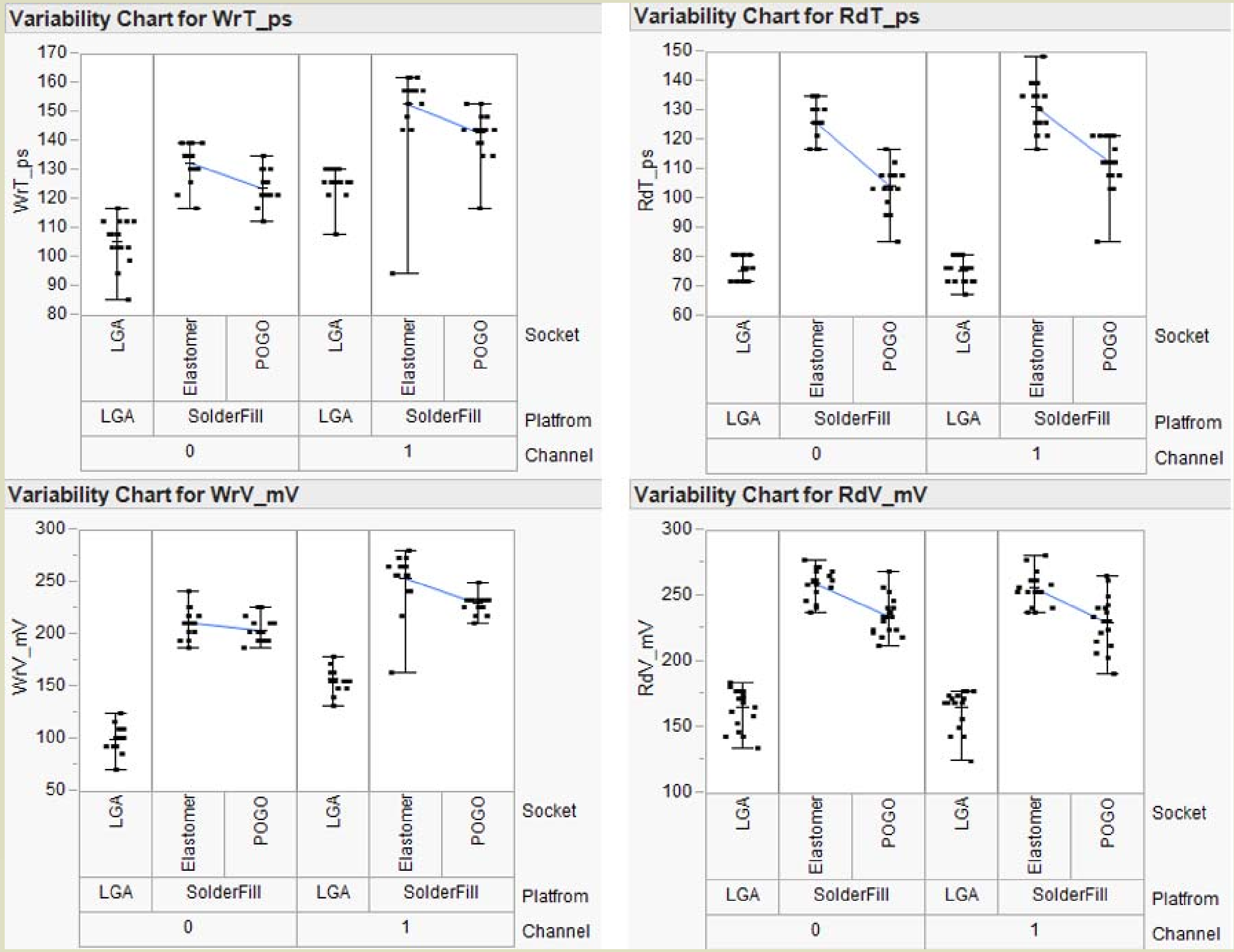
Variability Chart for WrV_mV



Variability Summary for WrV_mV

	Mean	Std Dev	Std Err Mean	Lower 95%	Upper 95%	Mini
WrV_mV	128.4	31.03774	4.970015	118.3387	138.4613	
Channel[0]	100.62	12.37177	2.766411	94.82983	106.4102	
Channel[1]	157.6421	10.58649	2.428706	152.5396	162.7446	

Memory Performance Results



Elastomer socket results provide the greatest amount of margin

Mean value improvement

Board	Socket	Channel	WrT_ps	WrV_mV	RdT_ps	RdV_mV
LGA	LGA	0	105	100	75	165
SolderFill	Elastomer	0	132	211	126	259
SolderFill	SOGO	0	123	204	104	234
LGA	LGA	1	126	157	75	165
SolderFill	Elastomer	1	152	253	131	256
SolderFill	SOGO	1	142	229	112	229

EV's eye margin risk limits: >120 ps/mV (Low), >100 ps/mV (Medium)

Conclusion and Next Steps

- Dual compression sockets seems promising, once speed pin advantage over regular LGA socket was achieved.
- Low profile Elastomer socket requires board cavity and caps to move to secondary side → Drives new design approach for PI/PD
- Elastomer material reliability in harsh environments for overclocking (exposure to N2, Dry Ice, Oil submersion) is still to be better understood
- Cost and ramp of supplier ecosystem to meet HVM requirements
- OEM & End user acceptance – handling and assembly

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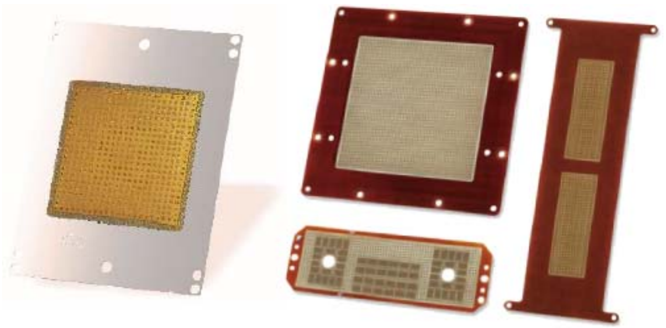
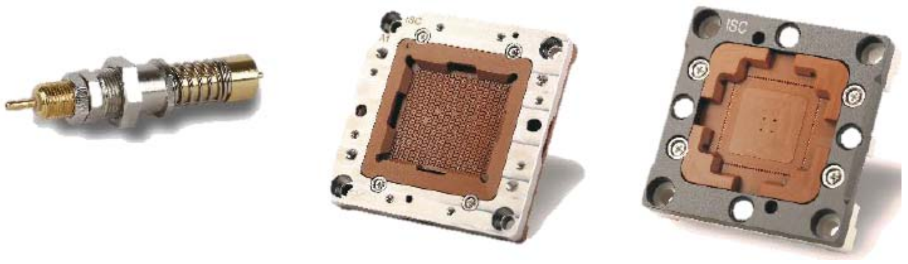


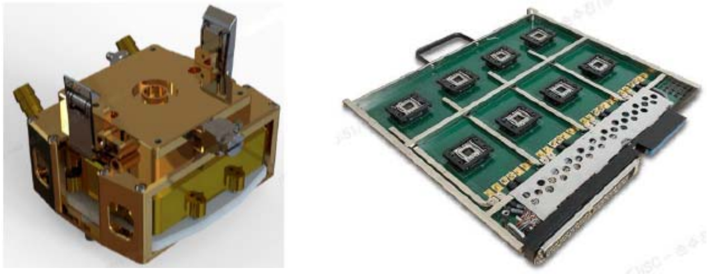
POGO SOCKET SOLUTIONS

- Excellent gap control & long lifespan
- High bandwidth & low contact resistance



THERMAL CONTROL UNIT

- Extreme active temperature control
- Safety auto shut-down temperature monitoring of the device & thermal control unit
- Full FEA analysis & Price competitiveness



BURN-IN SOLUTIONS

- Direct inserting on the board without soldering
- Higher performance BIB solution

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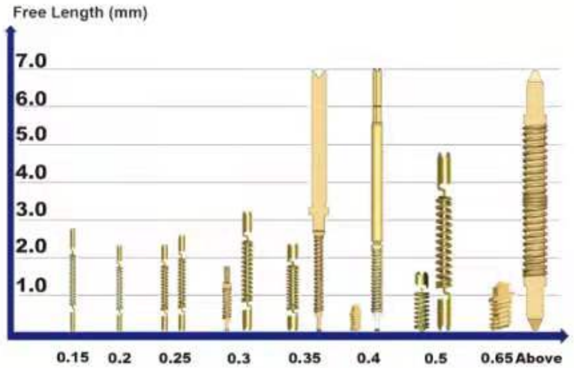
IWIN Co., Ltd. The test probe for high signal integrity at extremely high speed test

Spring probe by stamping



250 kinds of spring probe pin

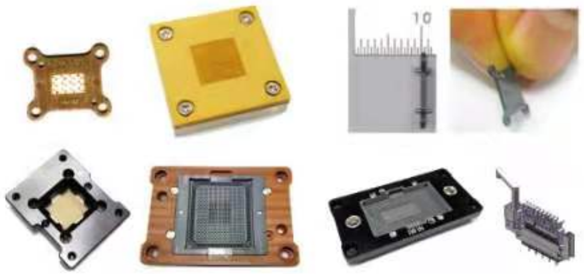
300 kinds of test socket (44,000 Pin count socket possible)

One piece spring probe

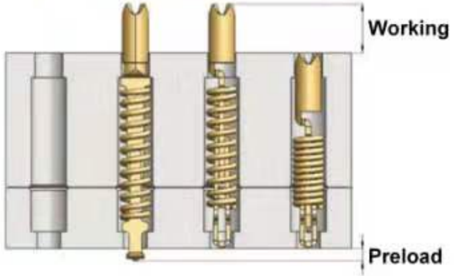
Three piece spring probe

High speed product → 0.63mm free length spring probe pin available

Finest Pitch → 0.15mm Pitch



Spring probe by stamping

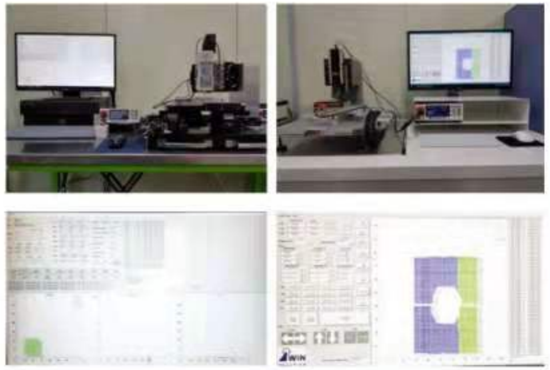


Patented

Pitch(mm)	Free Length(mm)	Current Carrying(Amps)
0.15/0.2/0.25	2.17~	0.5~
0.3	1.5~	1.5~
0.35	2.08~	1.8~
0.4	0.8~	2.5~
0.5	1.5~	3.0~
0.65	1.13~	9.0~
0.8	3.14~	3.0~

Automation

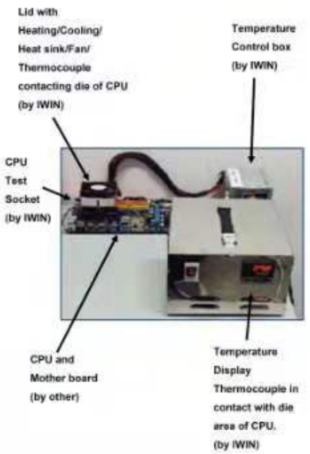
Pin assembly and Quality control



Top Figure: Socket CRES, Force, Stroke test
Bottom Figure: Data displayed

Top Figure: Socket CRES test
Bottom Figure: Data display 5,903 pins socket

Socket and Lid



Pin assembly

(Fully automated machines)

- Stamped piece parts attached to a reel fed into the assembly machine

- Assembled pins can be attached to a reel, or, supply in separate for socket assembly.

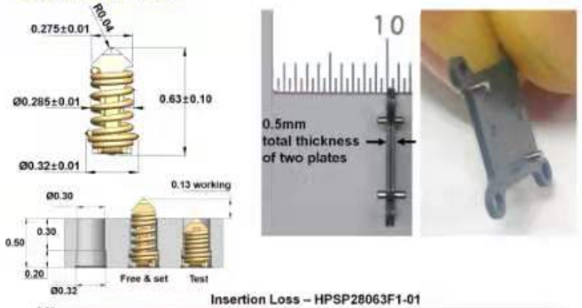
Spring probe pins for High speed

Extremely short spring probes by stamping

One piece spring probe

Three piece spring probe

Design approach



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