Modeling Measurement of High Bandwidth Device

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Texas Instruments

Virtual Event ● May 3 - 7, 2021

Agenda

- Pre-silicon Simulation[sim]
- Post silicon Measurement
- 2mm Trace Layout simulation data vs Network Analyzer [NA] measurement data
- Pre and Post Data correlation
- Summary

Information about measurement set up in general

- USB2.0 MUX switch
- Have multiple input pairs and output pairs
- User can decide which input and output to be connected by sending command through I2C
- For purpose of this presentation, study was done on below input and output pair
  - RP [positive input] to TP [positive output]
  - RN [negative input] to TN [negative output]

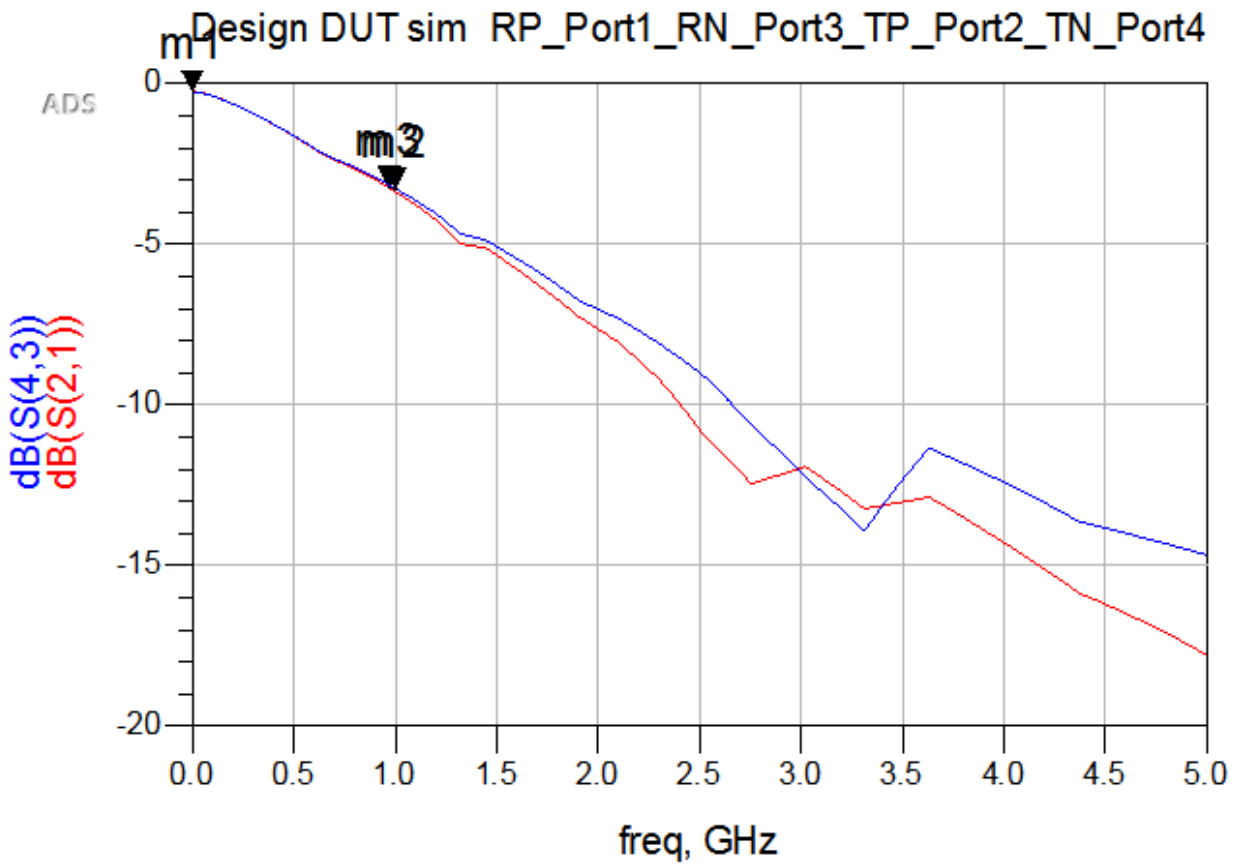
- Network analyzer[NA] is used to measure the DUT along with Advance Design System software [ADS] to extrapolate measurement data vs Simulation result.

Design DUT SIM (data from Designer)

m1
freq=300.0kHz
dB(S(4,3))=-0.264

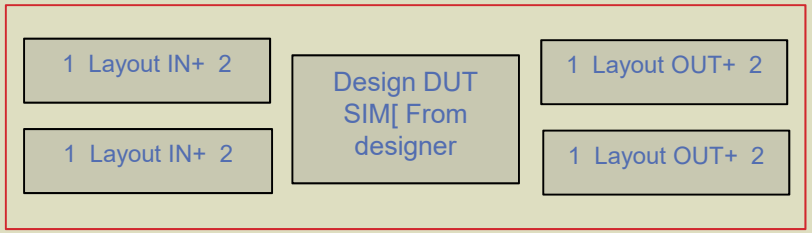
m2
freq=1.000GHz
dB(S(4,3))=-3.282

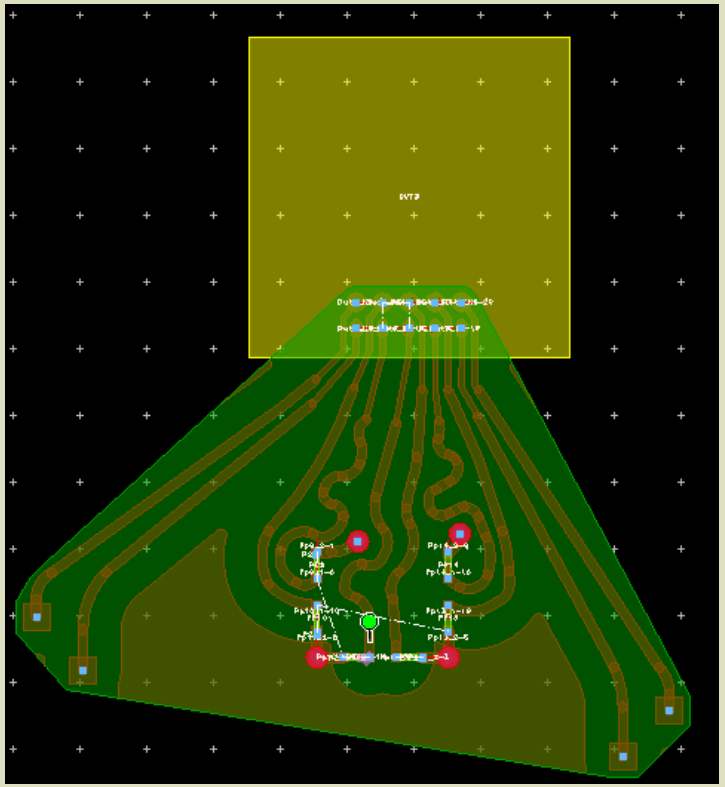
m3
freq=970.2MHz
dB(S(2,1))=-3.269



Generate S2P files from board Layout

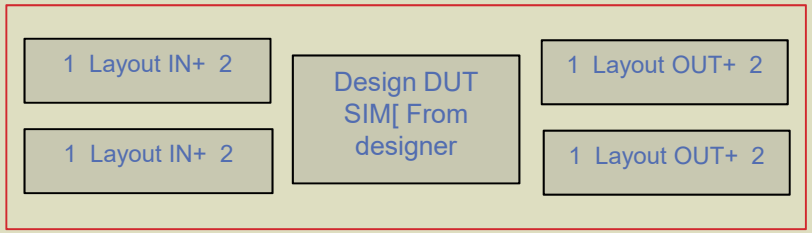
1. Get S2P file for each path from Layout. It is critical to follow below structure to get correct port assignment for layout Simulation.



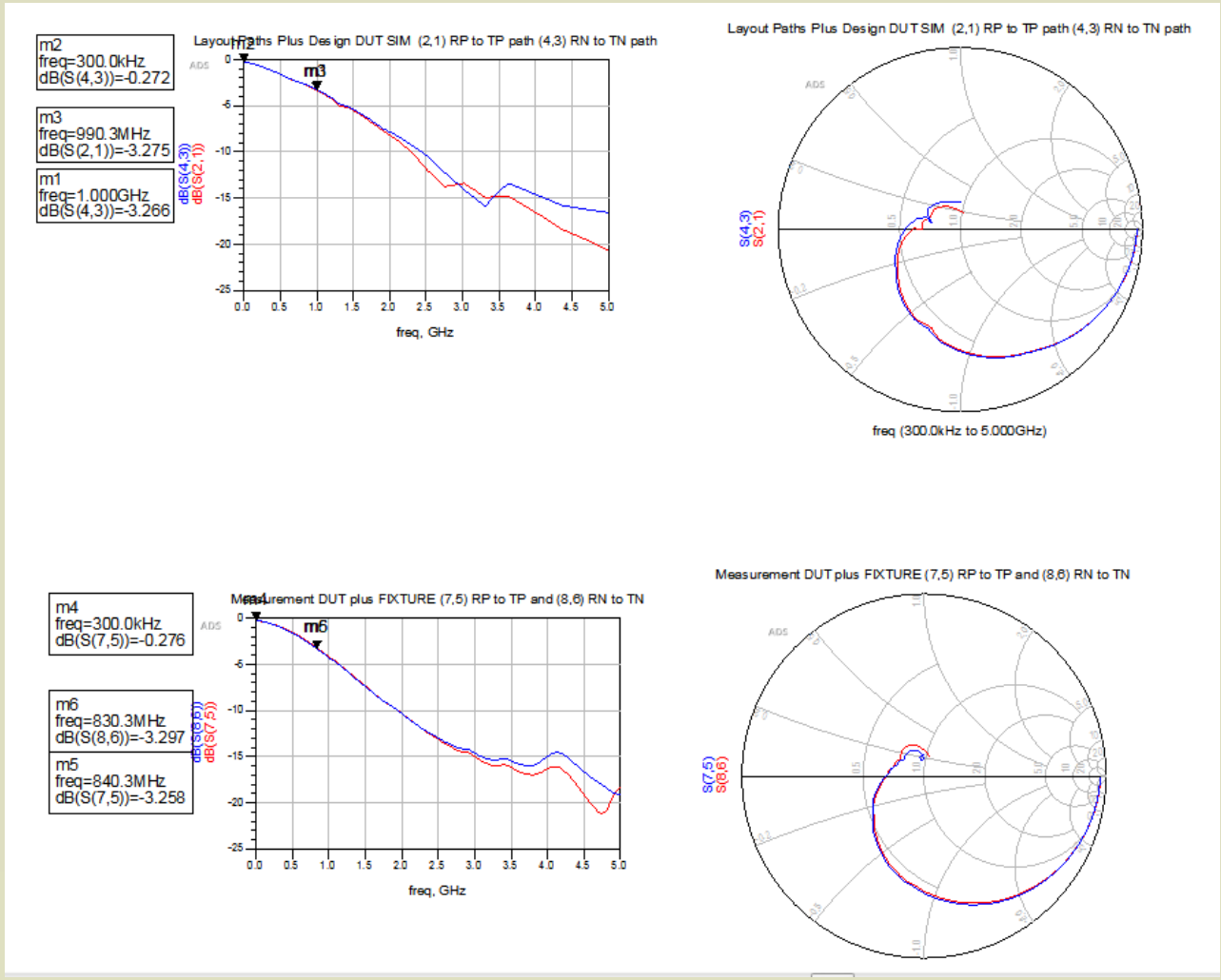


2. S2P file for each all 4 paths will be created from ADS
   I. Layout IN+.S2P
   II. Layout IN-.S2P
   III. Layout OUT+.S2P
   IV. Layout OUT-.S2P

Simulation of layout trace with DUT model



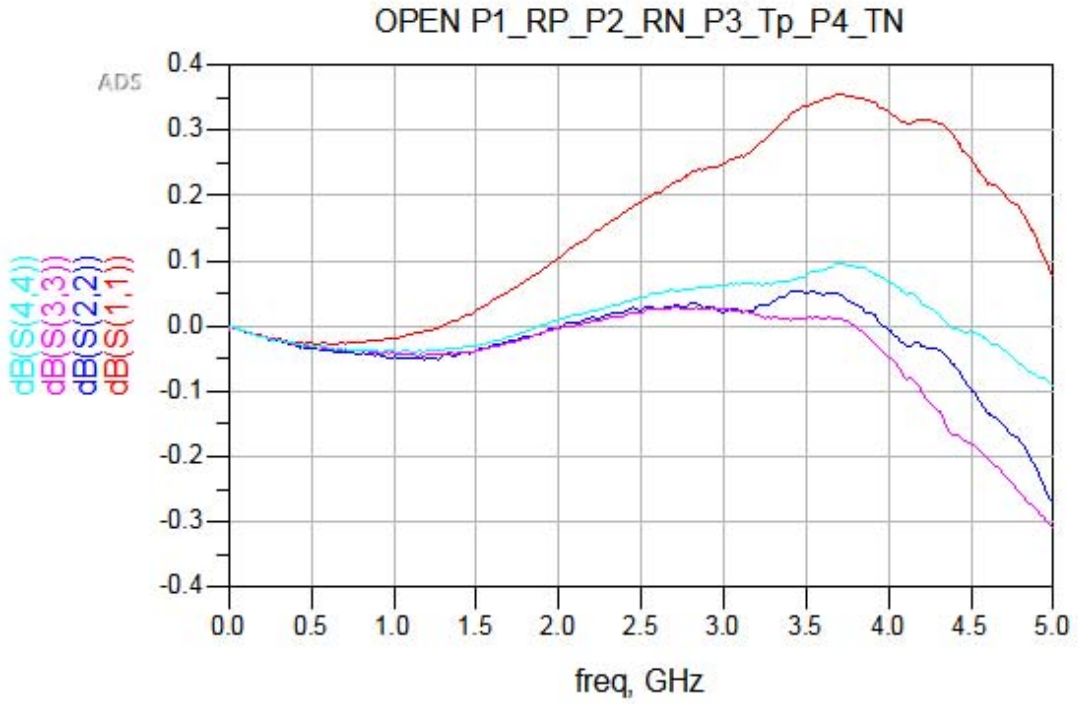
Do not see any effect of adding layout traces to Design DUT SIM. The same as Design DUT sim without traces

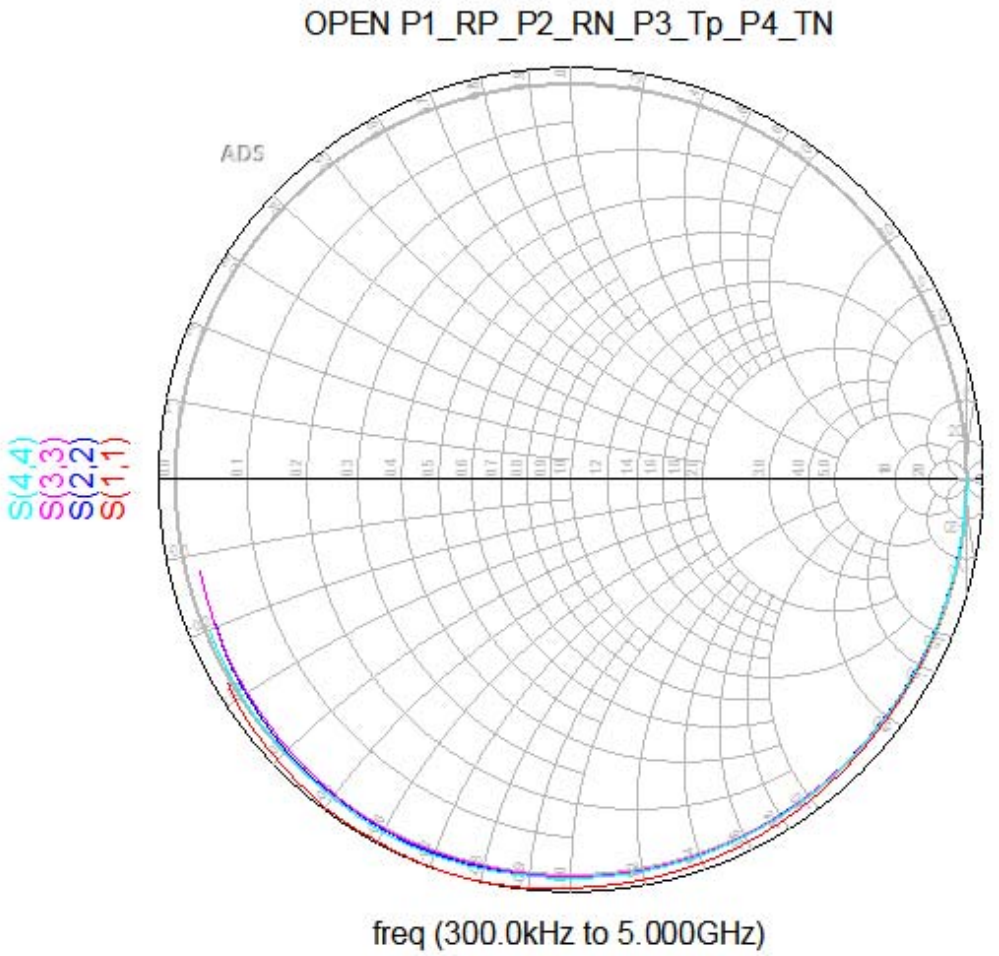


The De-Embedding Steps, Summarized

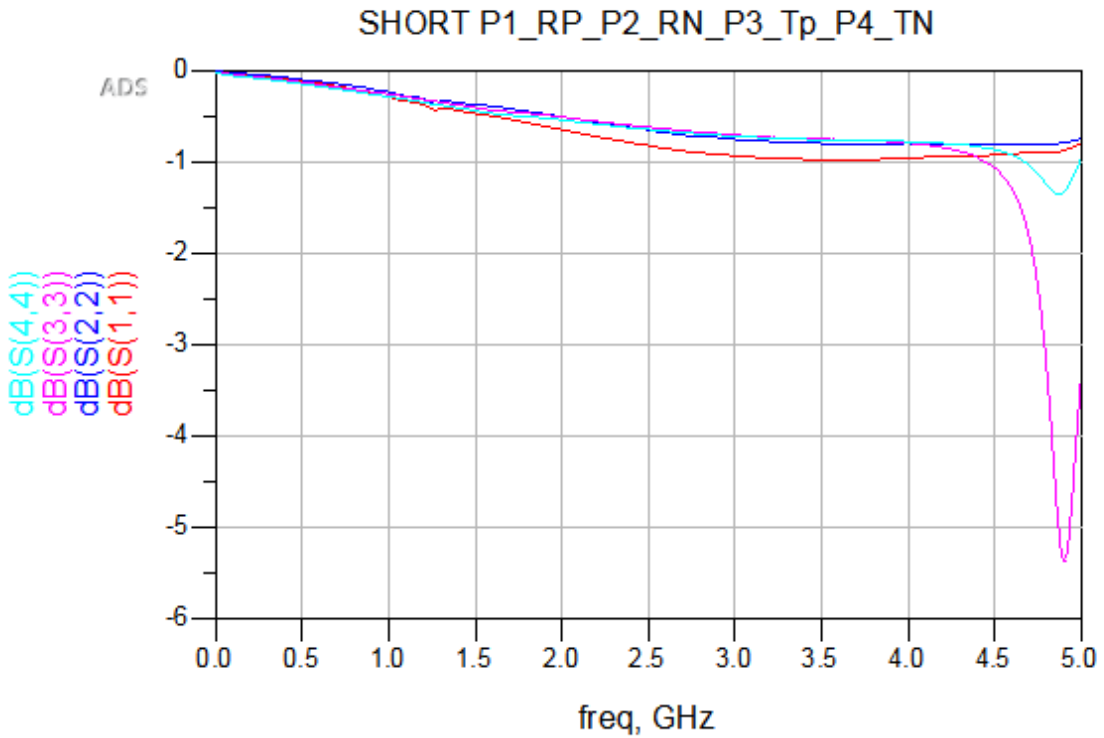
1. Build three PCB fixtures with DUT, open, and short.
2. Measure S-parameters of the open, short, and DUT using your network analyzer.
3. Convert S-parameters to Z-parameters and remove the series parasitic by subtracting:
   a) Z parameters of the short from Z parameter of embedded DUT
   b) Z parameters of the short from Z parameter of open
4. Convert Z-parameters from step 3a and 3b above to Y-parameters and remove the parallel parasitic by subtracting Y-open from Y-DUT (Y3a – Y3b).
5. Convert Y-parameter from step 4 above to S-parameters.

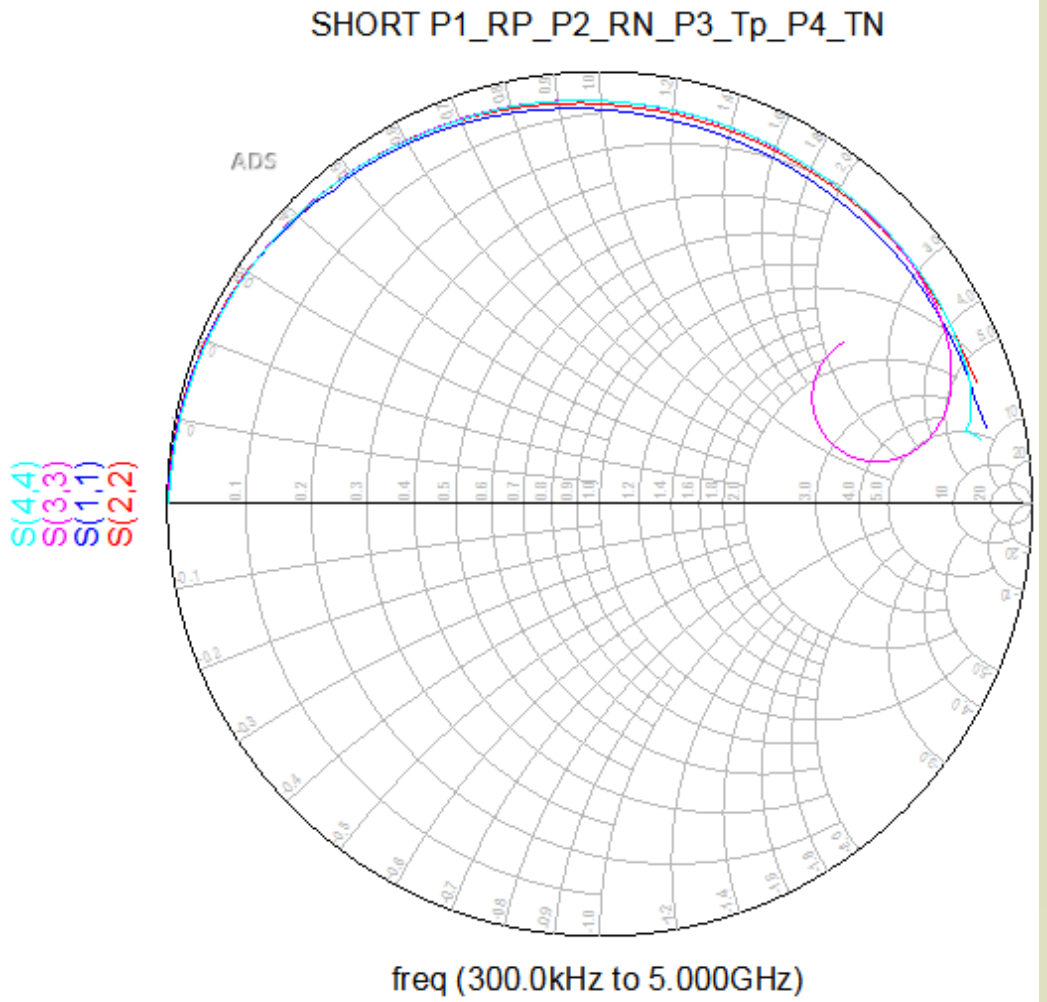
Simulation results for Measured OPEN RP, RN, TP and TN



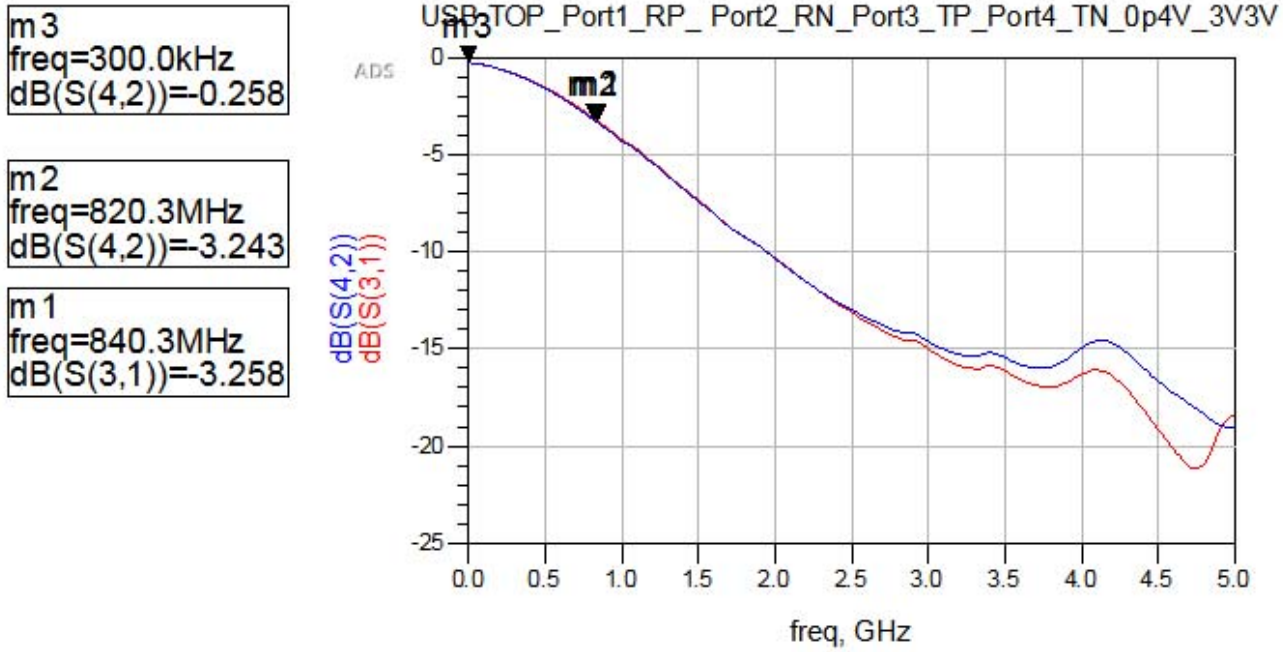


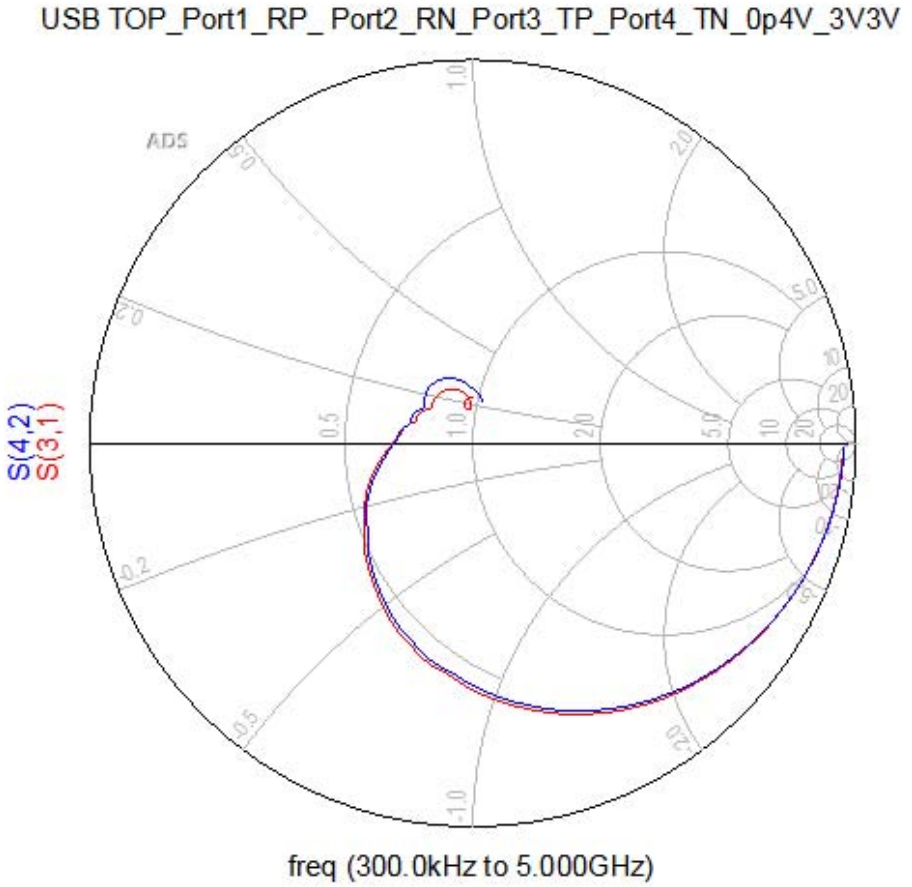
Simulation Results for Measured SHORT RP, RN, TP and TN





Measured DUT+FIXTURE





Step3

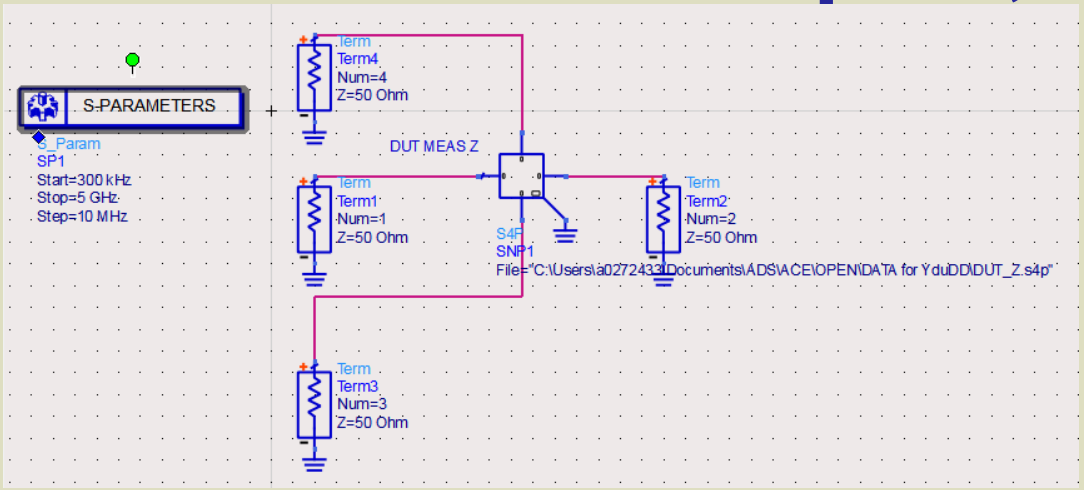
Convert S-parameters to Z-parameters and remove the series parasitic by subtracting:

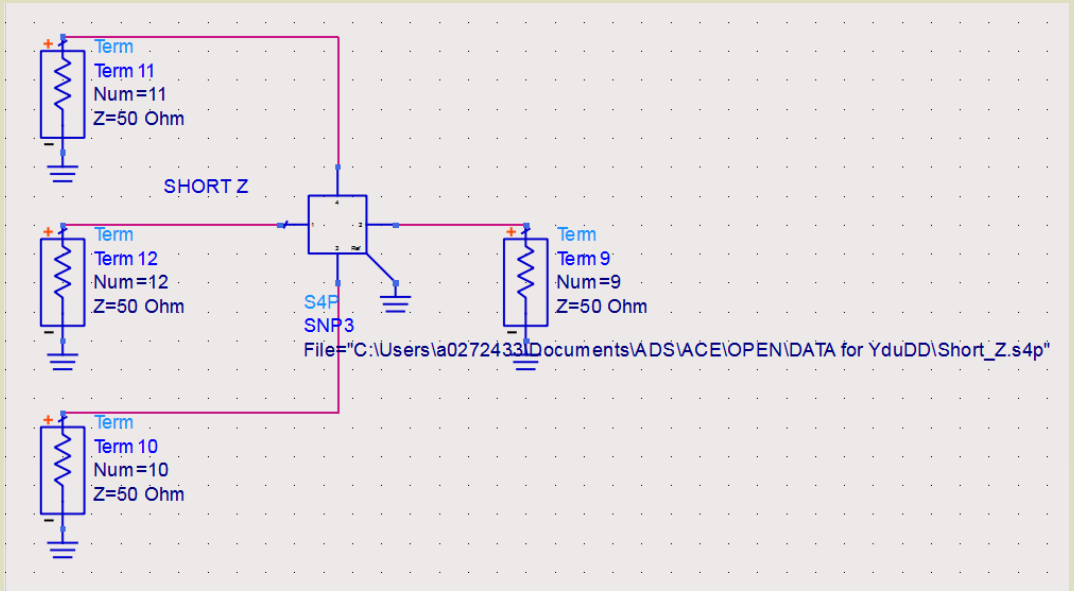
a) Z parameters of the short from Z parameter of embedded DUT
b) Z parameters of the short from Z parameter of open

ADS, import Measured Short, Open , DUT+ Fixture measurement and change the format to Z.

a) Zsh = Short measurement
b) Zop = Open measurement
c) Zdu = DUT + Fixture measurement
d) ZduD = Zdu – Zsh
e) ZopD = Zop - Zsh

Step 3a, ZduD = Zdu - Zsh





ZduD

Eqn ZduD11=(Z(1,1))-(Z(12,12))
Eqn ZduD12=(Z(1,2))-(Z(12,9))
Eqn ZduD13=(Z(1,3))-(Z(12,10))
Eqn ZduD14=(Z(1,4))-(Z(12,11))

Eqn ZduD21=(Z(2,1))-(Z(9,12))
Eqn ZduD22=(Z(2,2))-(Z(9,9))
Eqn ZduD23=(Z(2,3))-(Z(9,10))
Eqn ZduD24=(Z(2,4))-(Z(9,11))

Eqn ZduD31=(Z(3,1))-(Z(10,12))
Eqn ZduD32=(Z(3,2))-(Z(10,9))
Eqn ZduD33=(Z(3,3))-(Z(10,10))
Eqn ZduD34=(Z(3,4))-(Z(10,11))

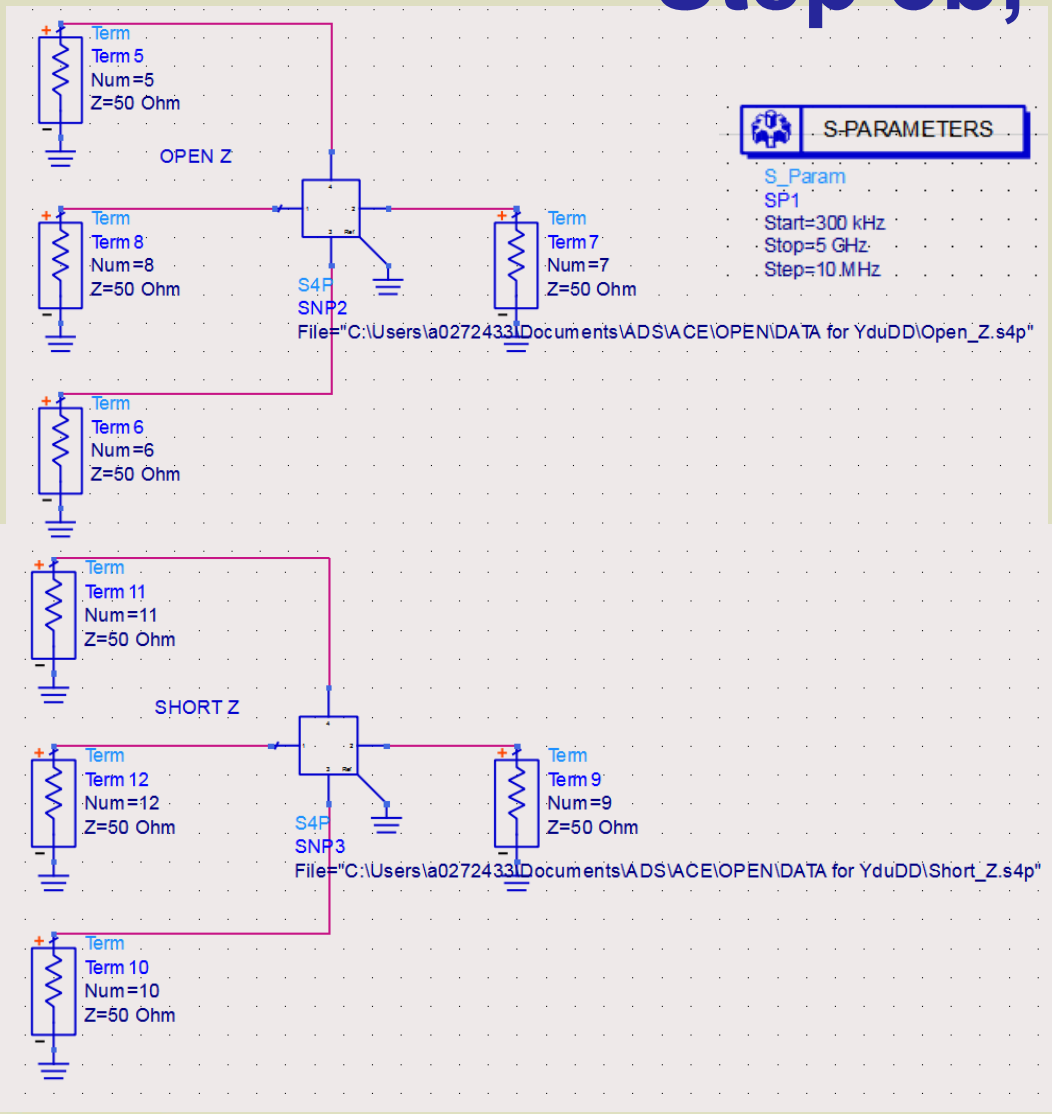
Eqn ZduD41=(Z(4,1))-(Z(11,12))
Eqn ZduD42=(Z(4,2))-(Z(11,9))
Eqn ZduD43=(Z(4,3))-(Z(11,10))
Eqn ZduD44=(Z(4,4))-(Z(11,11))

Eqn Zdiff={{ZduD11,ZduD12,ZduD13,ZduD14},{ZduD21,ZduD22,ZduD23,ZduD24},{ZduD31,ZduD32,ZduD33,ZduD34},{ZduD41,ZduD42,ZduD43,ZduD44}}

Eqn ZduD = write_snp("ZduD.s4p", Zdiff, "ZduD-parameter simulation data", "Hz", "RI", 50)

write_snp will default data into # Hz S RI R 1
So after file is written, change the format header to # Hz Z RI R 1 to use file as Z data format

Step 3b, ZopD = Zop - Zsh



ZopD

```
ZopD11=(Z(8,8))-(Z(12,12))
ZopD12=(Z(8,7))-(Z(12,9))
ZopD13=(Z(8,6))-(Z(12,10))
ZopD14=(Z(8,5))-(Z(12,11))

ZopD21=(Z(7,8))-(Z(9,12))
ZopD22=(Z(7,7))-(Z(9,9))
ZopD23=(Z(7,6))-(Z(9,10))
ZopD24=(Z(7,5))-(Z(9,11))

ZopD31=(Z(6,8))-(Z(10,12))
ZopD32=(Z(6,7))-(Z(10,9))
ZopD33=(Z(6,6))-(Z(10,10))
ZopD34=(Z(6,5))-(Z(10,11))

ZopD41=(Z(5,8))-(Z(11,12))
ZopD42=(Z(5,7))-(Z(11,9))
ZopD43=(Z(5,6))-(Z(11,10))
ZopD44=(Z(5,5))-(Z(11,11))

ZopDDiff={{ZopD11,ZopD12,ZopD13,ZopD14},{ZopD21,ZopD22,ZopD23,ZopD24},{ZopD31,ZopD32,ZopD33,ZopD34},{ZopD41,ZopD42,ZopD43,ZopD44}}

ZopDDiffFILE = write_snp("ZopD.s4p", ZopDDiff, "ZopD-parameter simulation data", "Hz", "RI", 50)
```

write_snp will default data into # Hz S RI R 1
So after file is written, change the format header to # Hz Z RI R 1 to use file as Z data format

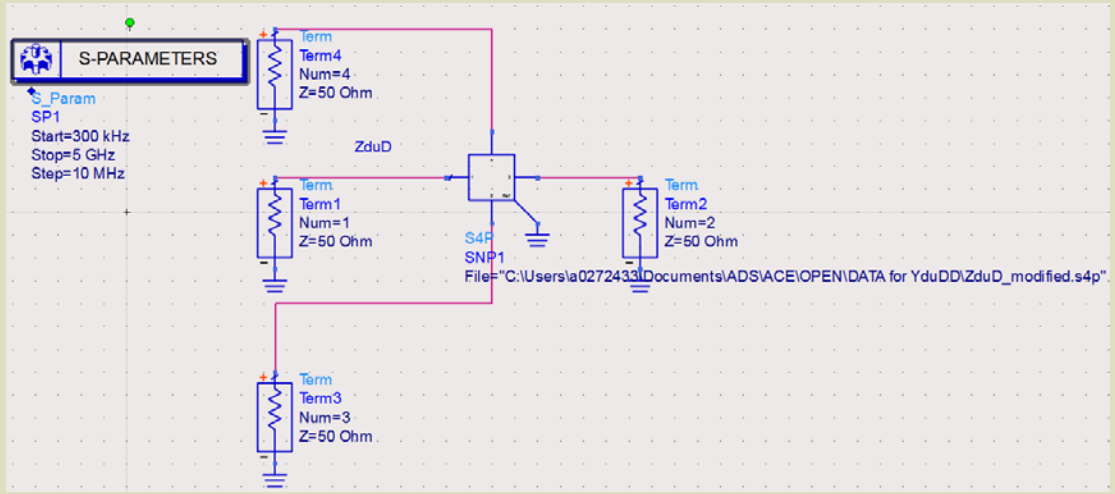
Step4

Convert Z-parameters from step 3a and 3b above to Y-parameters and remove the parallel parasitic by subtracting Y-open from Y-DUT (Y3a – Y3b).

- YduDD= YduD-YopD

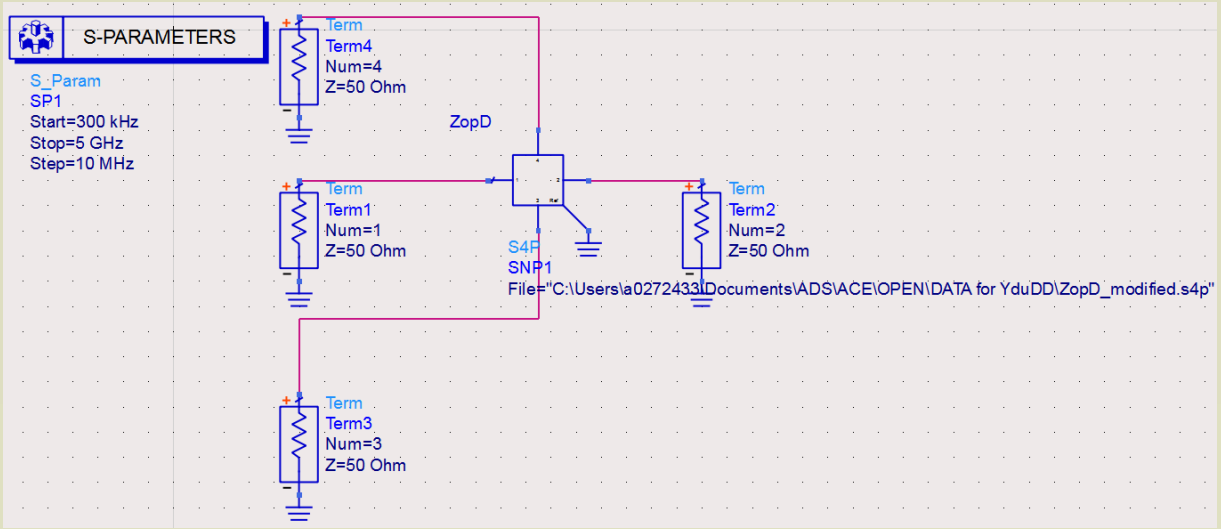
Convert ZduD, ZopD to Y in ADS

- ADS, import modified ZduD and ZopD and change the format to Y.



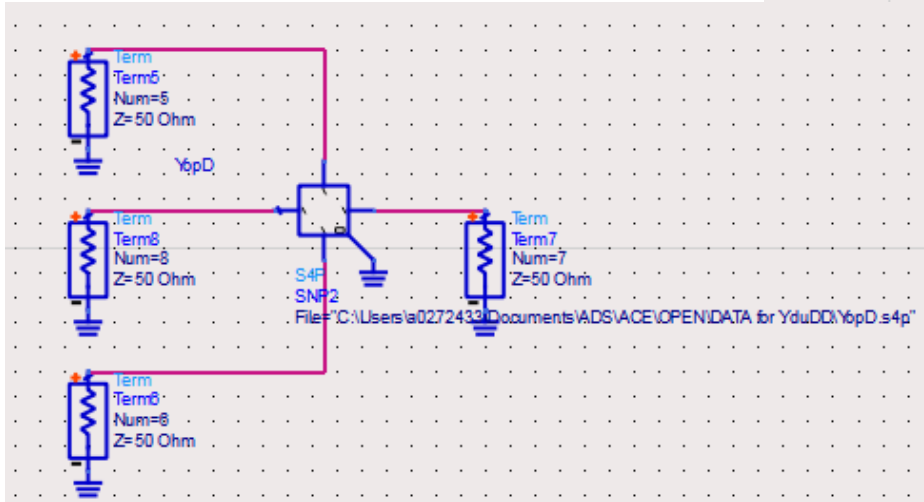
ZduD ⟹ YduD

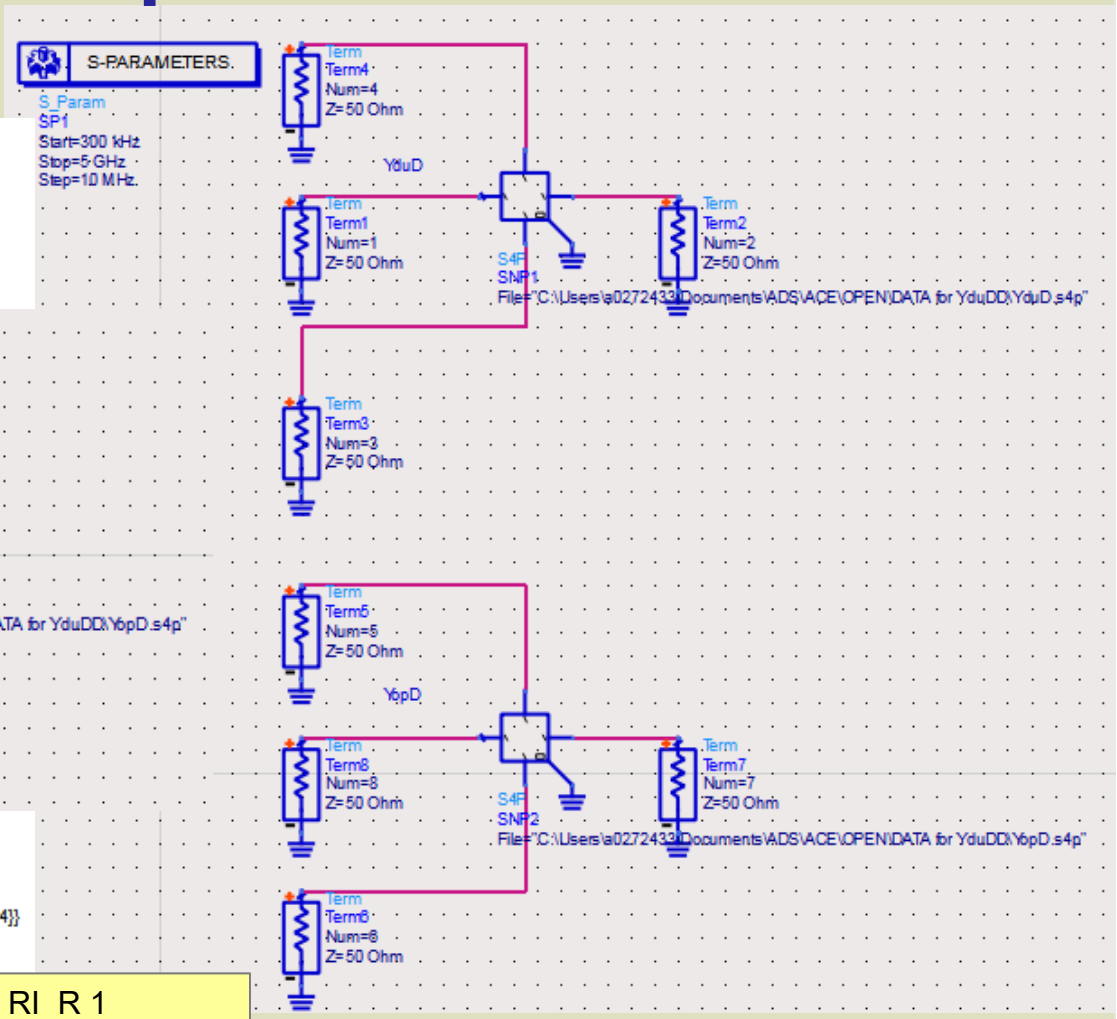
ZopD ⟹ YopD



YduDD= YduD-YopD

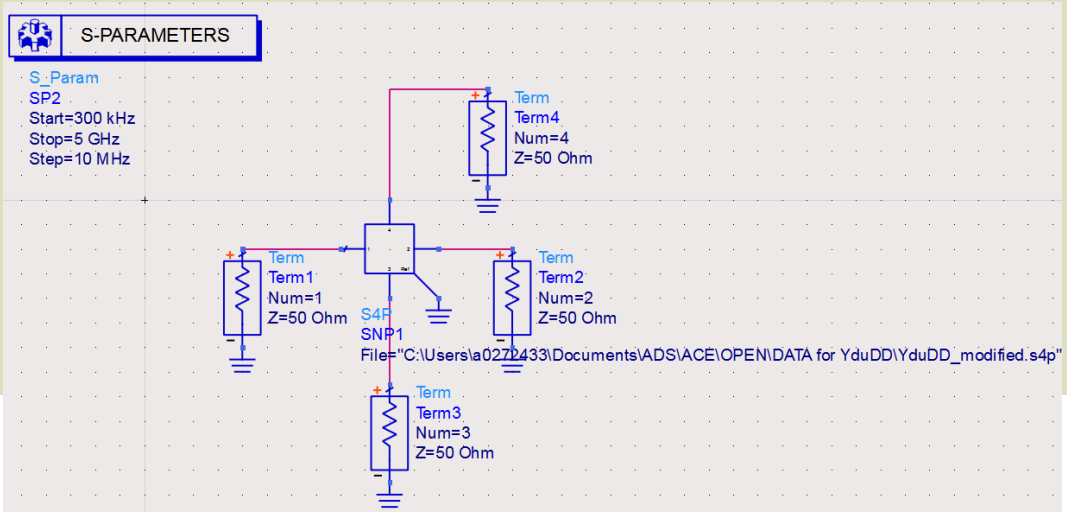
```
Eqn YduDD11=(Y(1,1))-(Y(8,8))
Eqn YduDD12=(Y(1,2))-(Y(8,7))
Eqn YduDD13=(Y(1,3))-(Y(8,6))
Eqn YduDD14=(Y(1,4))-(Y(8,5))

Eqn YduDD21=(Y(2,1))-(Y(7,8))
Eqn YduDD22=(Y(2,2))-(Y(7,7))
Eqn YduDD23=(Y(2,3))-(Y(7,6))
Eqn YduDD24=(Y(2,4))-(Y(7,5))

Eqn YduDD31=(Y(3,1))-(Y(6,8))
Eqn YduDD32=(Y(3,2))-(Y(6,7))
Eqn YduDD33=(Y(3,3))-(Y(6,6))
Eqn YduDD34=(Y(3,4))-(Y(6,5))

Eqn YduDD41=(Y(4,1))-(Y(5,8))
Eqn YduDD42=(Y(4,2))-(Y(5,7))
Eqn YduDD43=(Y(4,3))-(Y(5,6))
Eqn YduDD44=(Y(4,4))-(Y(5,5))

Eqn YduDD={{YduDD11,YduDD12,YduDD13,YduDD14},{YduDD21,YduDD22,YduDD23,YduDD24},{YduDD31,YduDD32,YduDD33,YduDD34},{YduDD41,YduDD42,YduDD43,YduDD44}}

Eqn YduDDFILE = write_snp("YduDD.s4p", YduDD, "YduDD-parameter simulation data", "Hz", "RI", 50)
```





write_snp will default data into # Hz S RI R 1
So after file is written, change the format header to # Hz Y RI R 1 to use file as Y data format

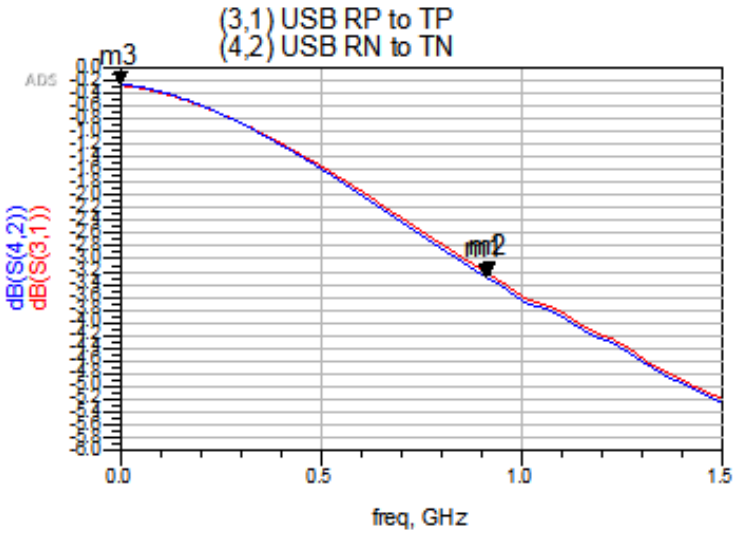
Step 5, YduDD to SduDD

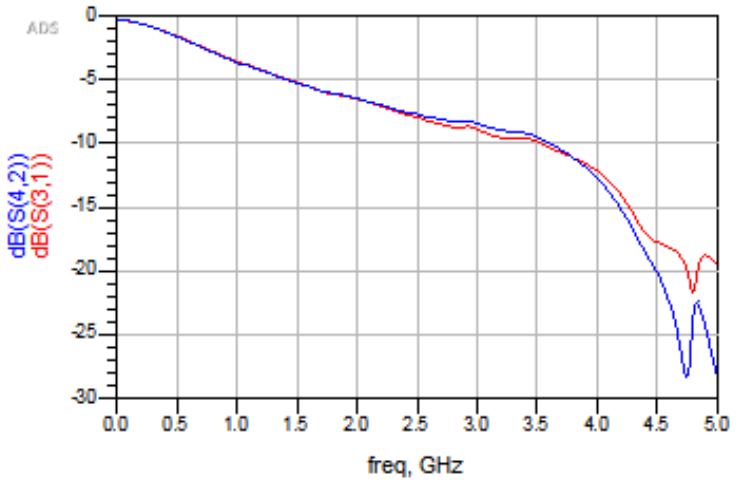


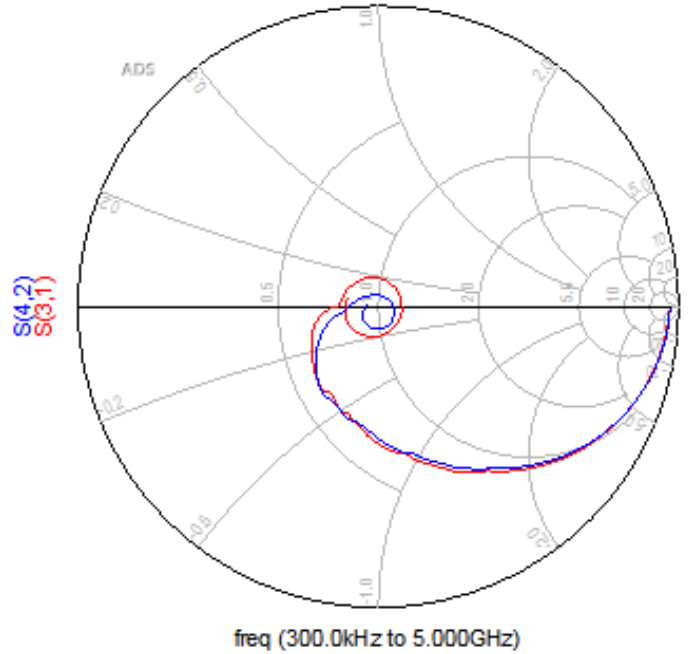
m1
freq=910.3MHz
dB(S(4,2))=-3.279

m2
freq=920.3MHz
dB(S(3,1))=-3.239

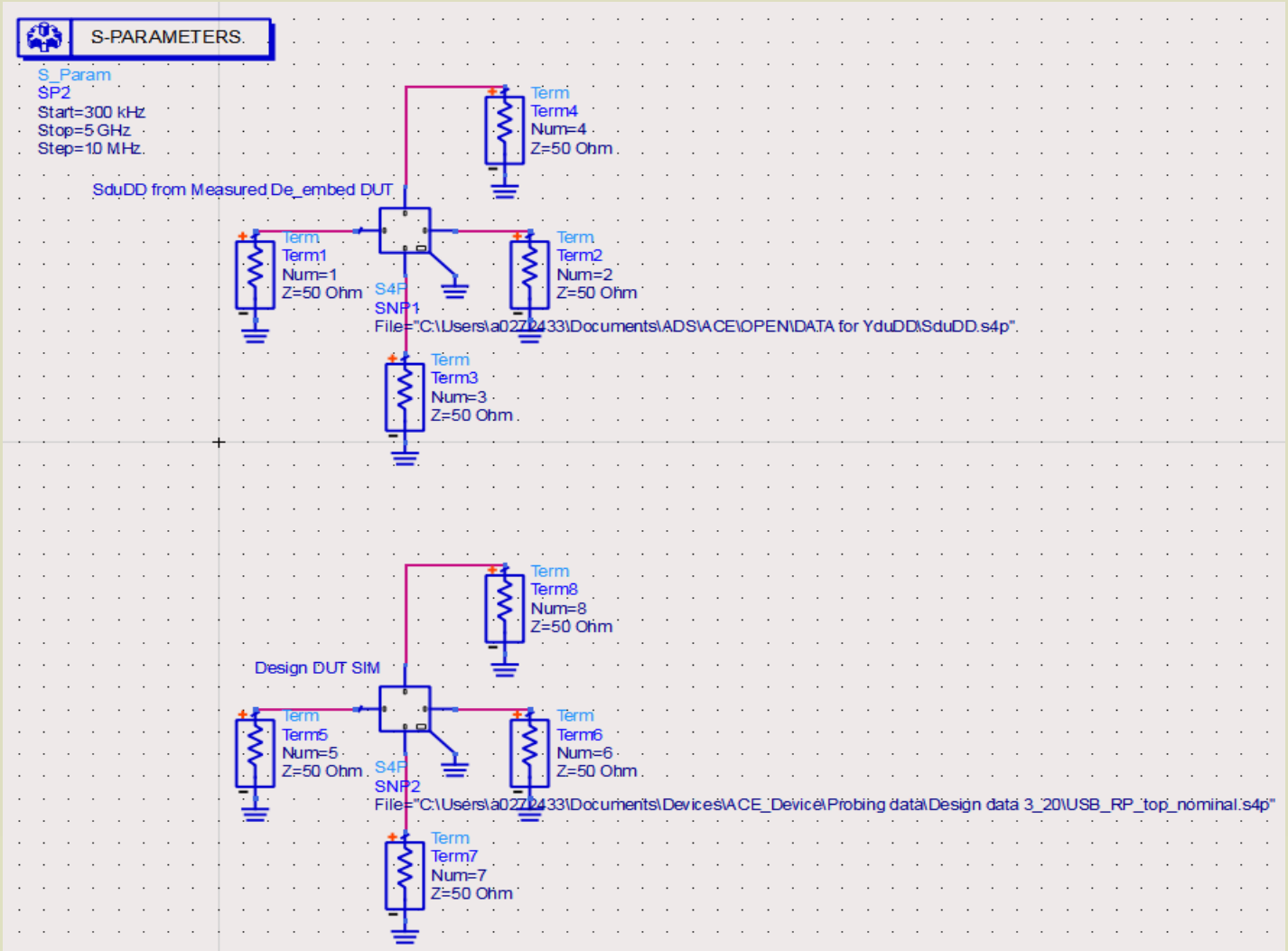
m3
freq=300.0kHz
dB(S(4,2))=-0.247





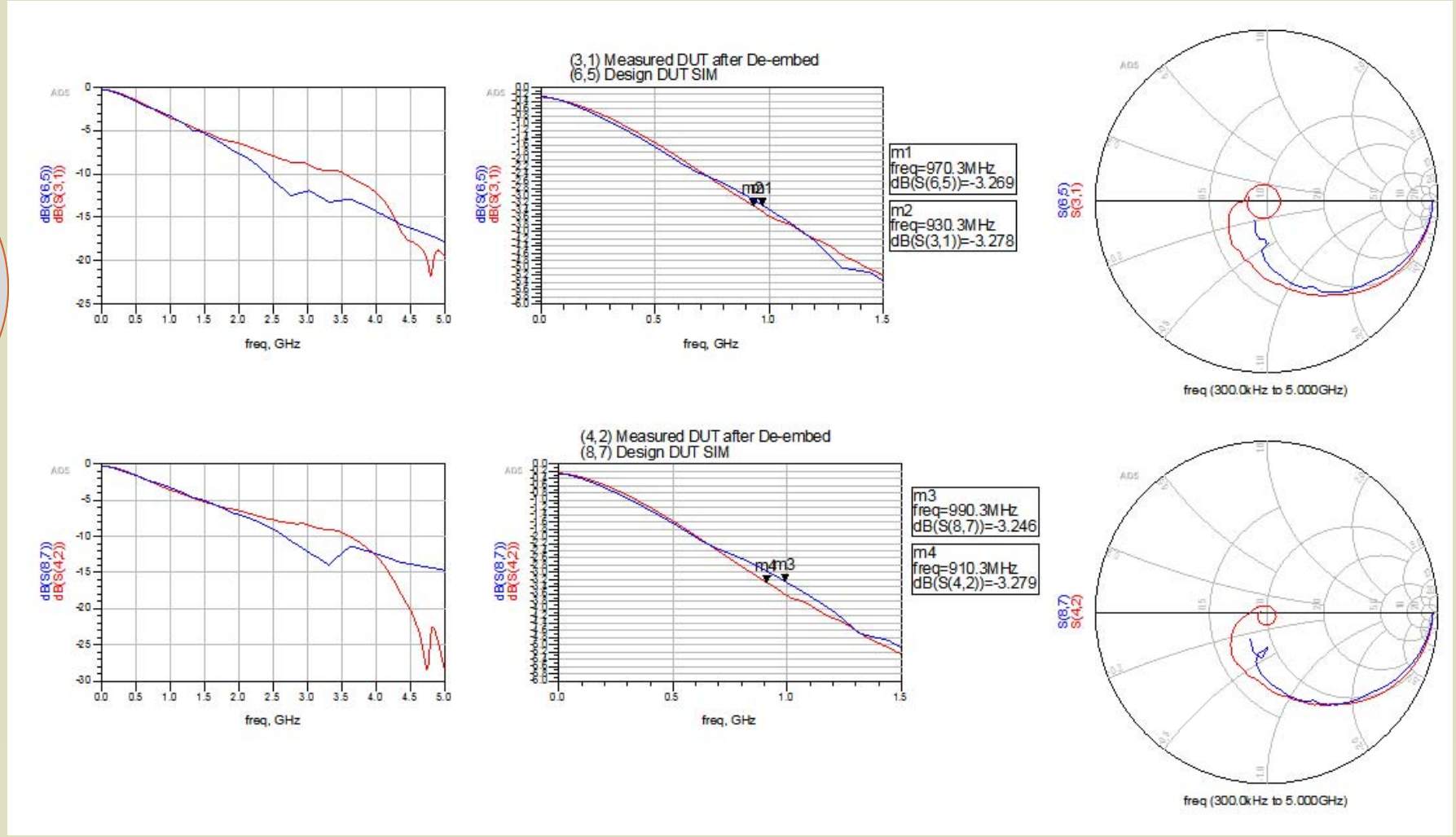


Measured DUT after De_Embedding vs Design DUT SIM

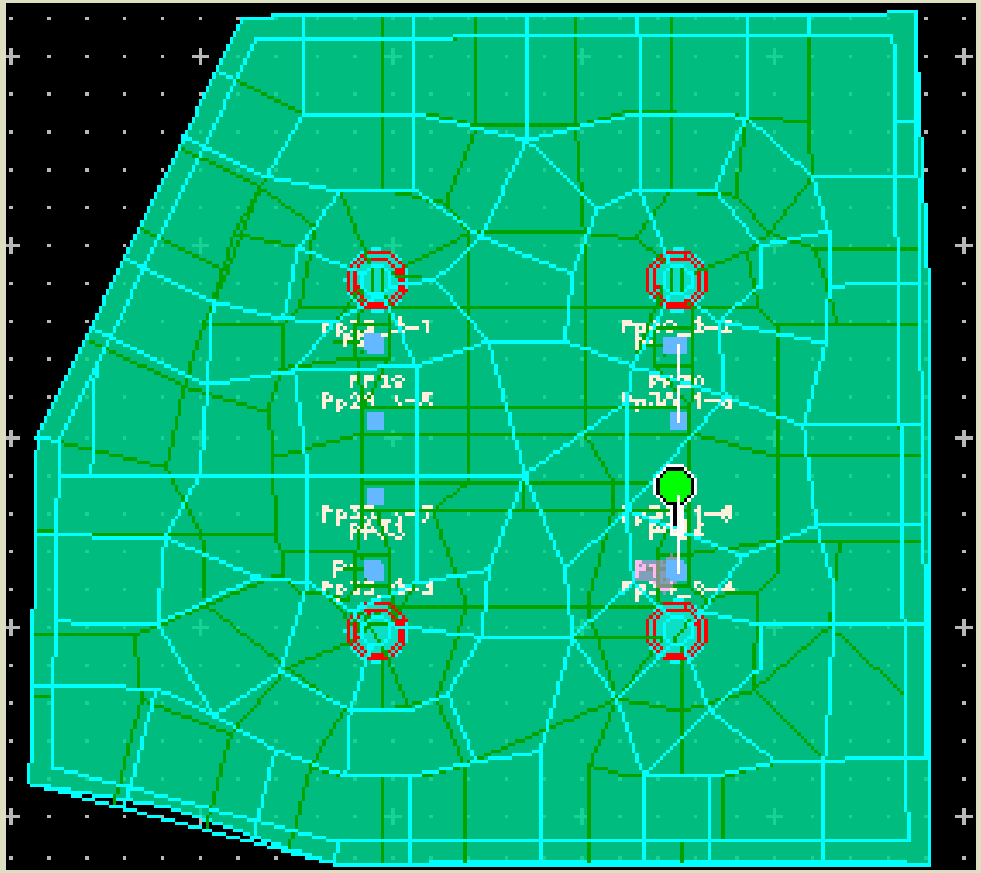


Measured DUT after De_Embed vs Design DUT SIM

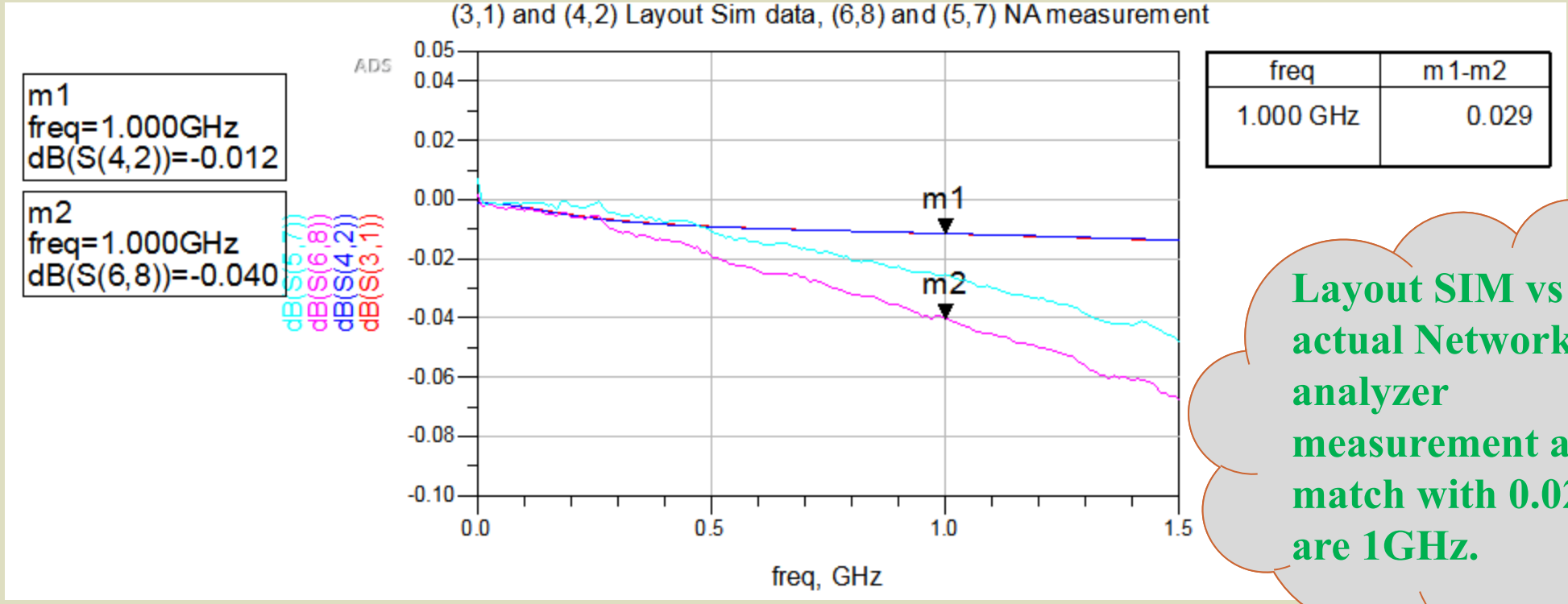
We still have unaccounted lost of Δ40 MHz in RP-TP path and Δ80 MHz in RN-TN path. Where that coming from?



Layout Simulation thru path mesh

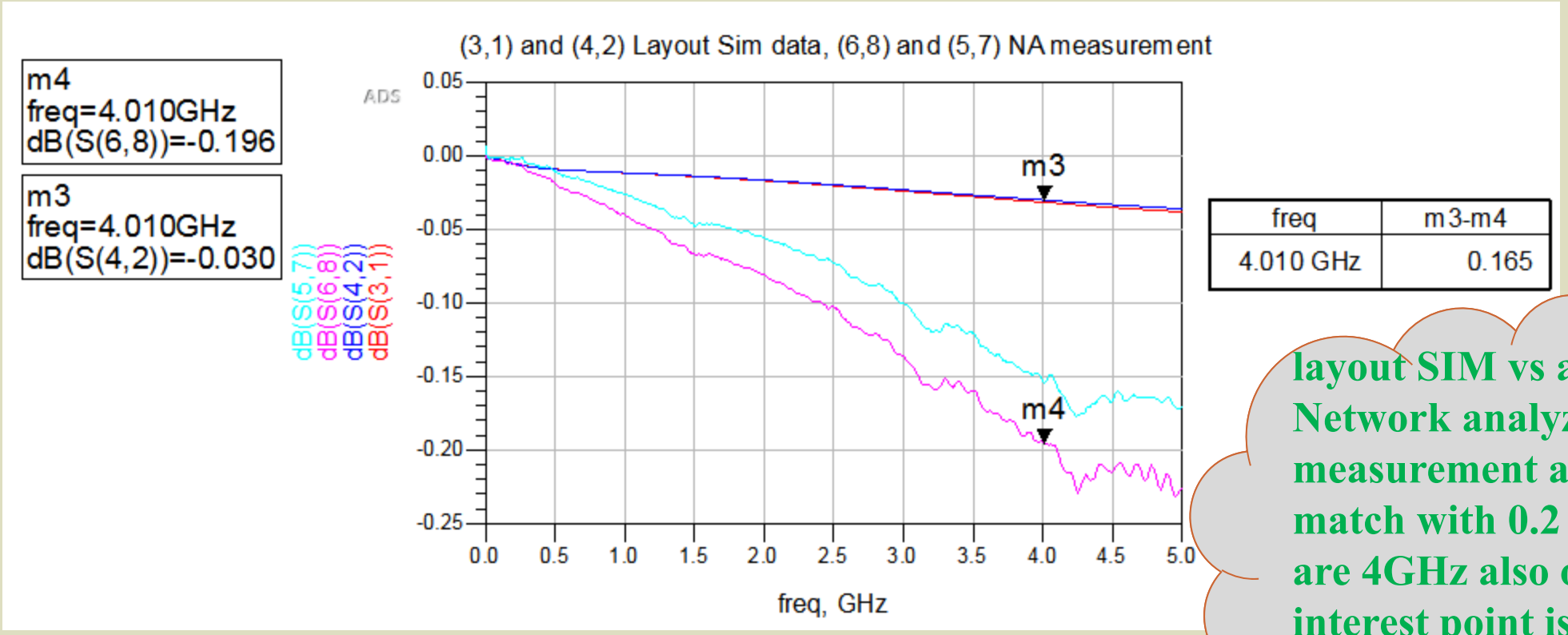


Comparison up to 1 GHz Layout Vs Measured thru path



Layout SIM vs actual Network analyzer measurement are match with 0.02 dB are 1GHz.

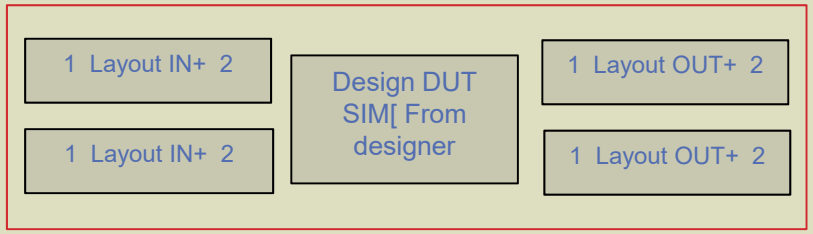
Comparison up to 5 GHz Layout Vs Measured thru path



freq	m3-m4
4.010 GHz	0.165

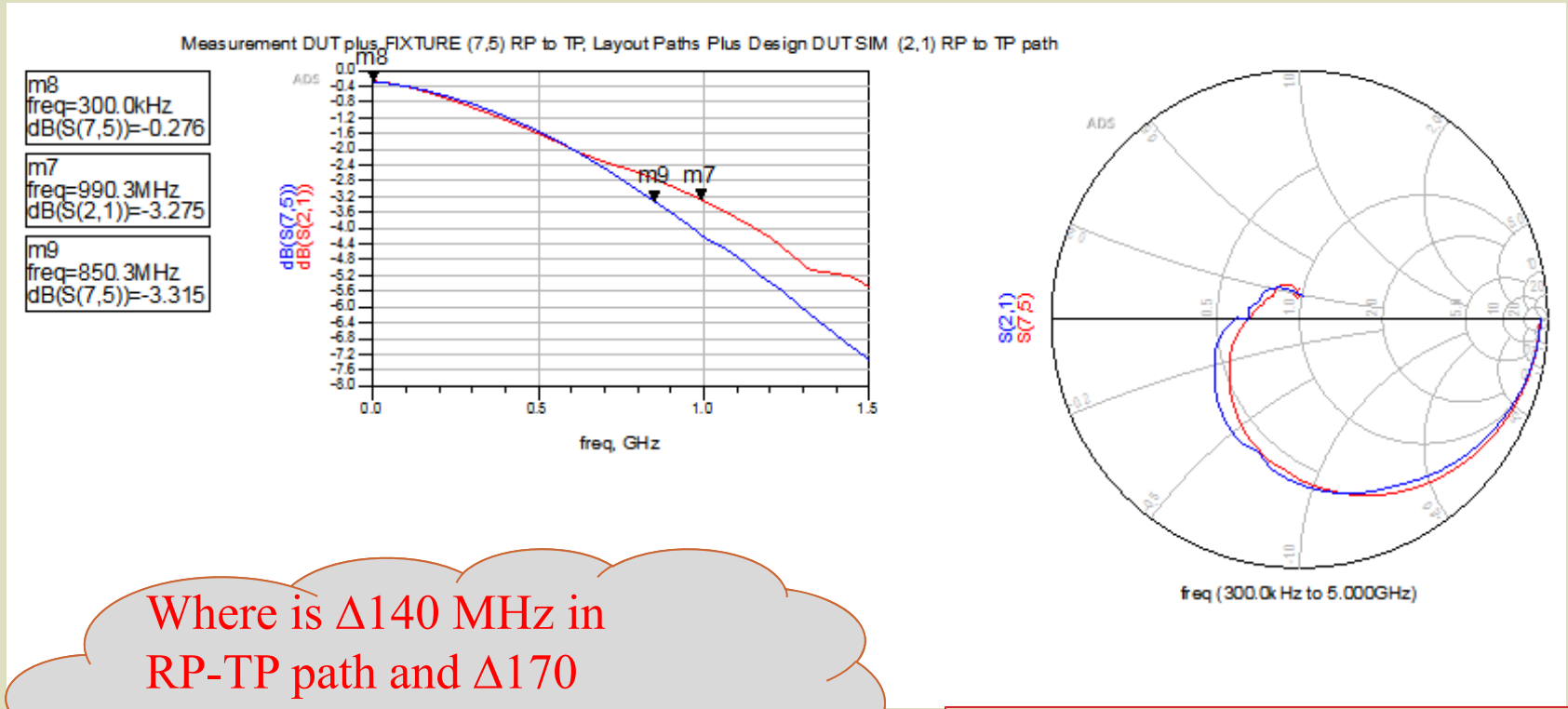
layout SIM vs actual Network analyzer measurement are match with 0.2 dB are 4GHz also our interest point is at 850MHz.

Layout Paths Plus Design DUT SIM vs Measurement DUT+ Fixture



VS

RP to TP



Where is Δ140 MHz in RP-TP path and Δ170 MHz in RN-TN path coming from ????

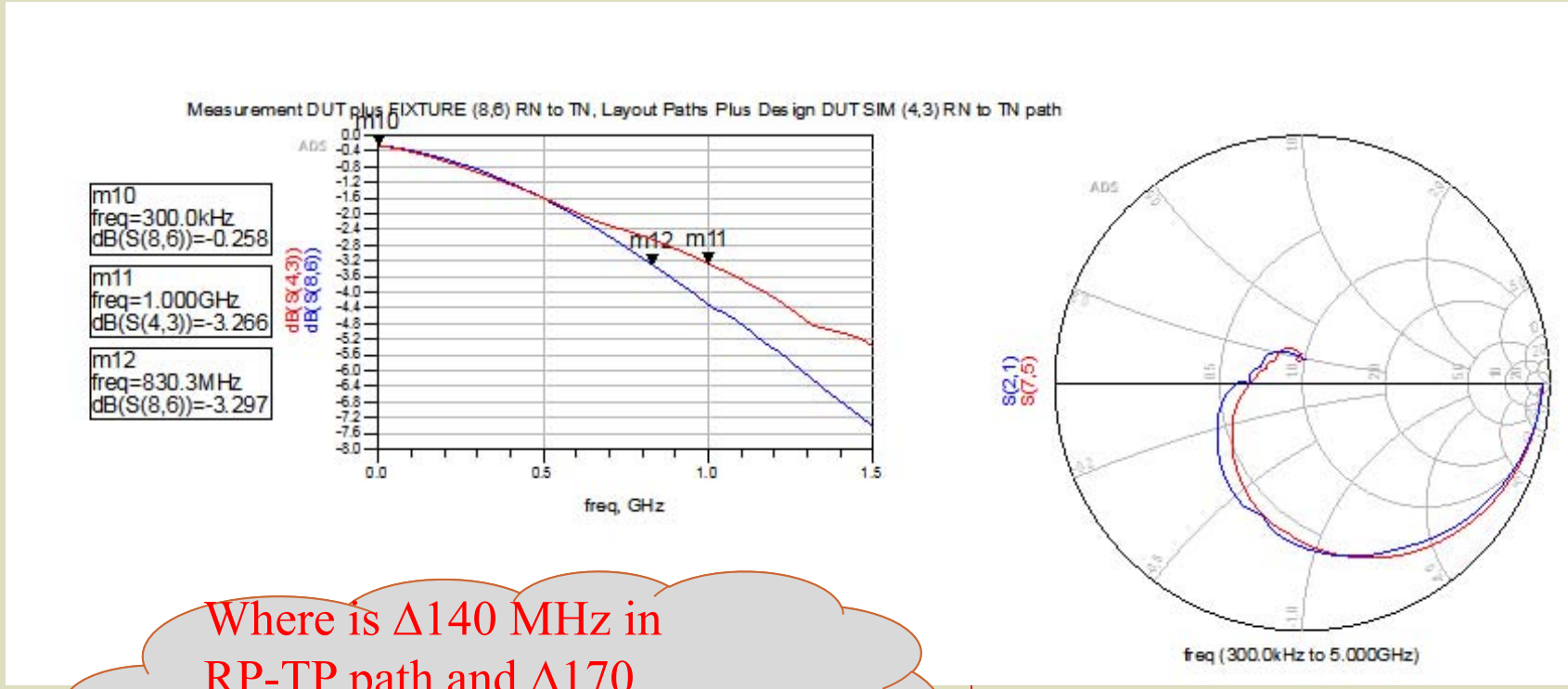
Red is Pre silicon data

- Layout Paths Simulation data of the traces plus Design DUT Sim

Blue is post silicon measurement data

- Using NA, measured FIXTURE + DUT measurement

RN to TN



Where is Δ140 MHz in RP-TP path and Δ170 MHz in RN-TN path coming from ????

Red is Pre silicon data

- Layout Paths Simulation data of the traces plus Design DUT Sim

Blue is post silicon measurement data

- Using NA, measured FIXTURE + DUT measurement

Summary

After taken care of loss due to the trace, we are still seeing 70MHz lost which are un-accounted for.
Next step: investigate on Packaging model of DUT

Experiment	3dB Frequency
Design SIM DUT	990 MHz
Probe Measured DUT + Trace	850 MHz
Design SIM DUT + EM trace	990 MHz
Probe Measured De-embed DUT + Probe Measured Trace	920 MHz

70MHz corresponds to 350fF of extra Cap on each side [input & output].

1. Design DUT [data from Designer]
2. Layout Trace + Design DUT
3. Network Analyzer Probe Data

m1
freq=970.3MHz
dB(S(2,1))=-3.269

Design DUT
(2,1) TP
(4,3) TN

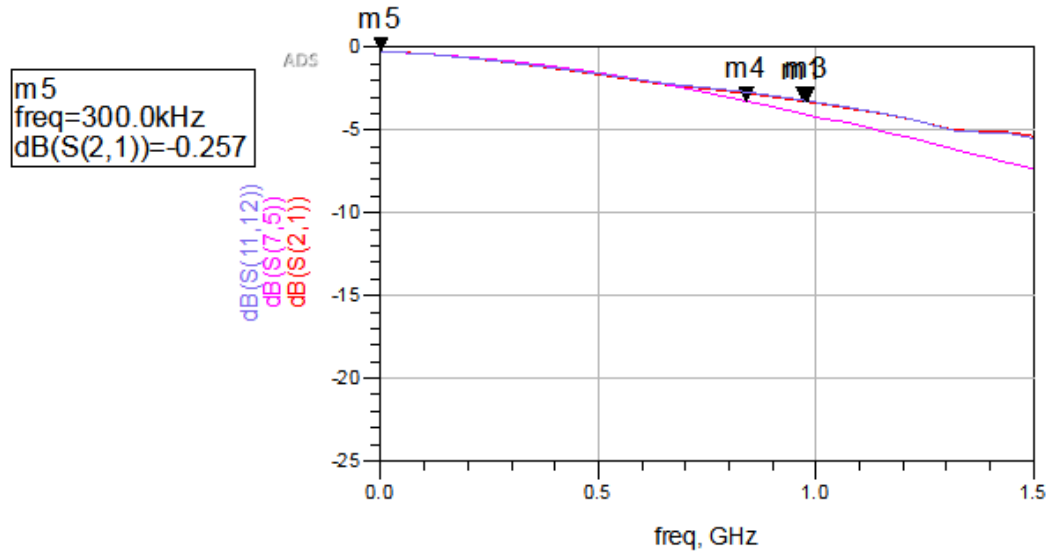
m3
freq=980.3MHz
dB(S(11,12))=-3.235

Layout Trace +Design DUT data
(11,12) TP
(9,10) TN

m4
freq=840.3MHz
dB(S(7,5))=-3.258

Probe Data
(7,5) TP
(8,6) TN

m5
freq=300.0kHz
dB(S(2,1))=-0.257



References

- CMOS RF Modeling, Characterization and Applications by M.Jamal Deen, Tor A. Fjeldly
- How to Characterize Surface Mount RF Devices application note by Agilent Technologies

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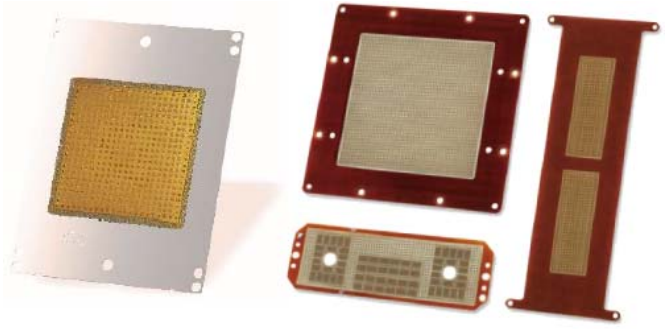
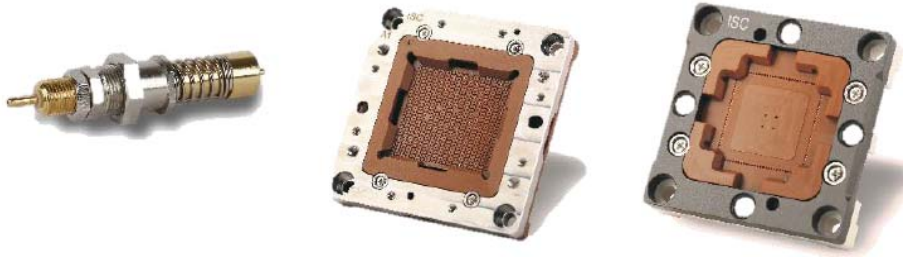


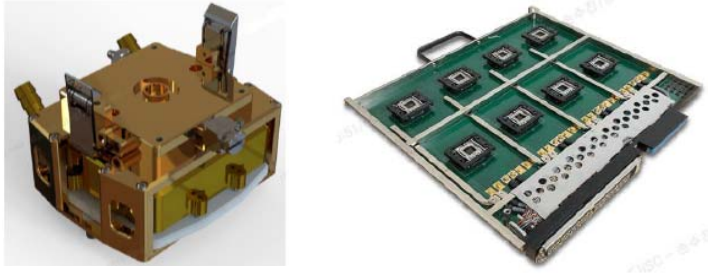
POGO SOCKET SOLUTIONS

- Excellent gap control & long lifespan
- High bandwidth & low contact resistance



THERMAL CONTROL UNIT

- Extreme active temperature control
- Safety auto shut-down temperature monitoring of the device & thermal control unit
- Full FEA analysis & Price competitiveness



BURN-IN SOLUTIONS

- Direct inserting on the board without soldering
- Higher performance BIB solution

CONTACT
ISC CO., LTD

ISC HQ
Seong-nam, Korea

ISC International
Silicon-valley, CA

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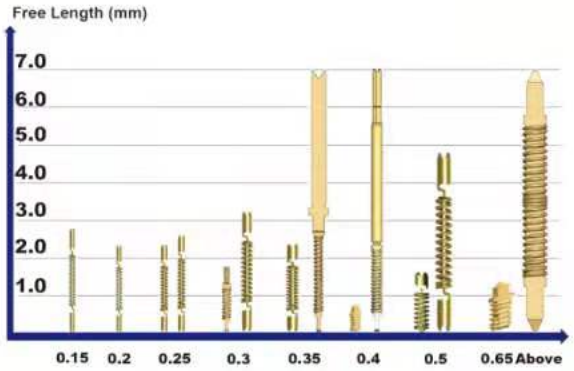
IWIN Co., Ltd. The test probe for high signal integrity at extremely high speed test

Spring probe by stamping



250 kinds of spring probe pin

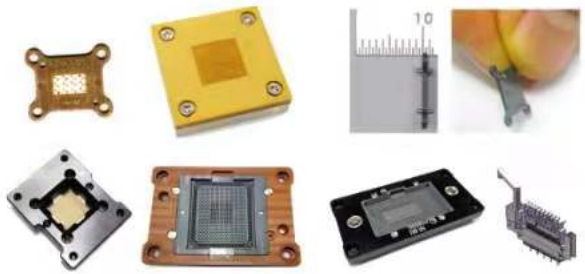
300 kinds of test socket (44,000 Pin count socket possible)

One piece spring probe

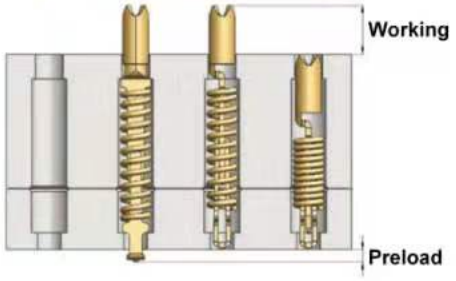
Three piece spring probe

High speed product → 0.63mm free length spring probe pin available

Finest Pitch → 0.15mm Pitch



Spring probe by stamping

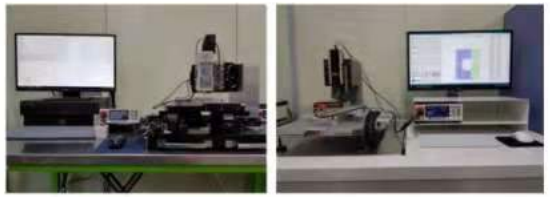


Patented

Pitch(mm)	Free Length(mm)	Current Carrying(Amps)
0.15/0.2/0.25	2.17~	0.5~
0.3	1.5~	1.5~
0.35	2.08~	1.8~
0.4	0.8~	2.5~
0.5	1.5~	3.0~
0.65	1.13~	9.0~
0.8	3.14~	3.0~

Automation

Pin assembly and Quality control



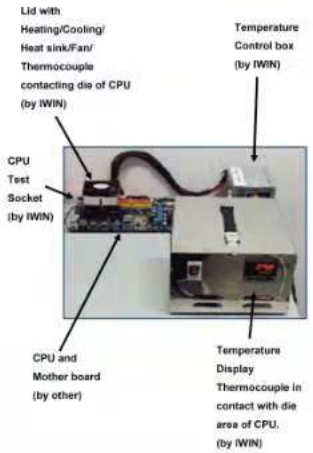
Top Figure: Socket CRES, Force, Stroke test

Bottom Figure: Data displayed

Top Figure: Socket CRES test

Bottom Figure: Data display 5,903 pins socket

Socket and Lid



Pin assembly

(Fully automated machines)

- Stamped piece parts attached to a reel fed into the assembly machine

- Assembled pins can be attached to a reel, or, supply in separate for socket assembly.

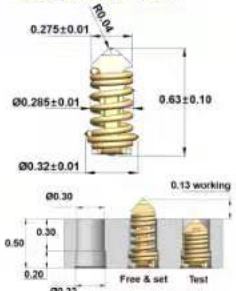
Spring probe pins for High speed

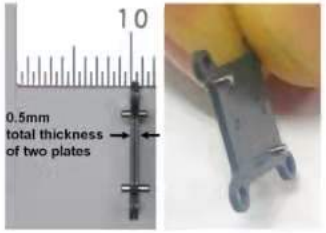
Extremely short spring probes by stamping

One piece spring probe

Three piece spring probe

Design approach





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High Performance Probe solution

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