#### VIRTUAL EVENT

# TestConX

Presentation Archive May 3-7, 2021

TestConX.org

© 2021 TestConX- Image: tonda / iStock

## Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

#### Xiao-Ming Gao Intel Corporation



Virtual Event • May 3 - 7, 2021



## Agenda

- Overview of PAM4 in high-speed interfaces
- Challenges of PAM4 IP validation
- Advantages of coax via PAM4 interposer
- Design of PAM4 interposer
- Manufacturing process
- Summary



## **Overview of PAM4 in High-Speed Interfaces**

- Platform channel bandwidth bottleneck
- Transition from NRZ to PAM4
- 4-level modulation and bandwidth efficient
- Sensitive to noise and crosstalk
- Employ FEC to improve BER performance

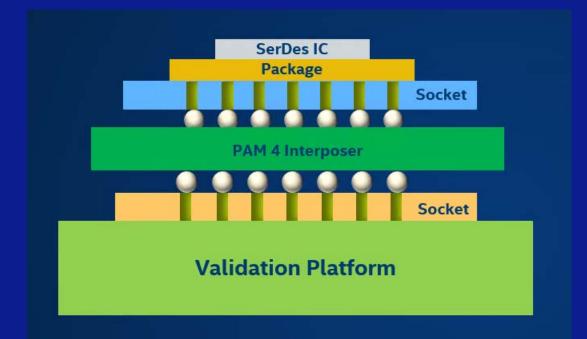


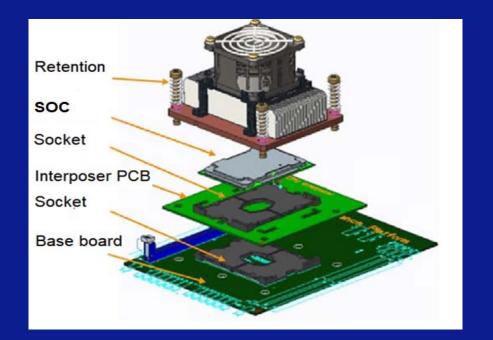
## **Challenges of PAM4 IP Validation**

- Very high data rate up to 100 Gb/s and beyond
- Crosstalk isolation is critical to IP electrical performance
- PAM4 IP providers use different package ball map
- New platform design for each IP validation
- Low return on investment and slow time to market



#### **PAM4 Interposer Usage Model**







Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

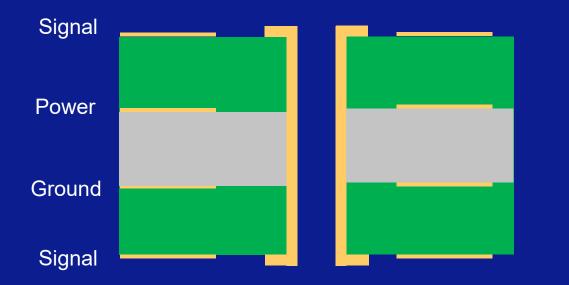
5

#### **Advantages of Coax Via PAM4 Interposer**

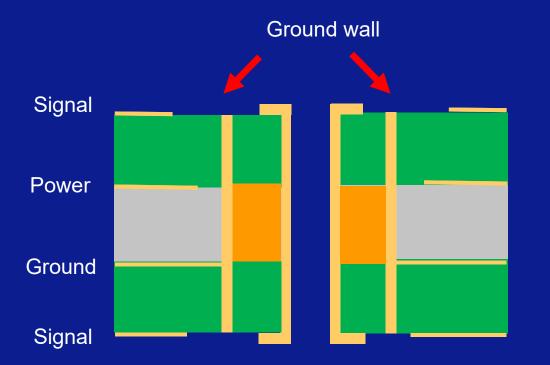
- Reuse of baseboard platform
- Reduce development cost and speed up time to market
- Excellent crosstalk isolation
- Measurements can be done on interposer
- More accurate validation of PAM4 IP electrical parameters



#### **Coax ground via construction**



#### Standard via



#### Coax via with ground wall



Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

202

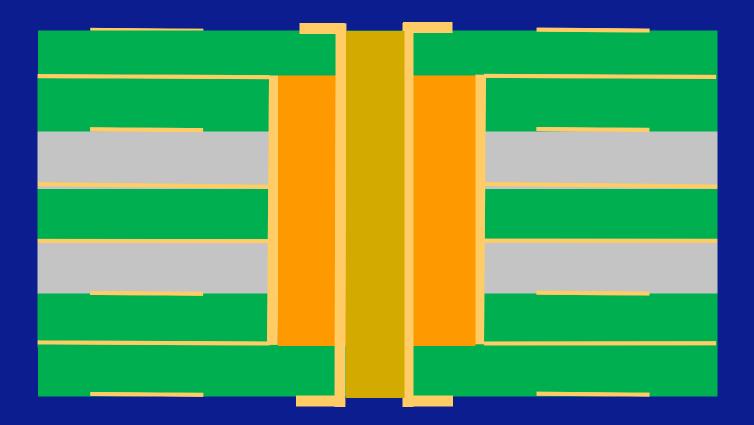
- Coax ground via internal layer construction process

   First step is to drill the larger outer via
   Second step is to plate this larger through hole via
   Third step is to fill the hole with dielectric material

  Construct the top and bottom layer with traces
- Add the top and bottom layers to internal layers and press together
- Drill the inner via from top to bottom layers
- Plate inner through hole via



#### **Manufacturing Process Demonstration**





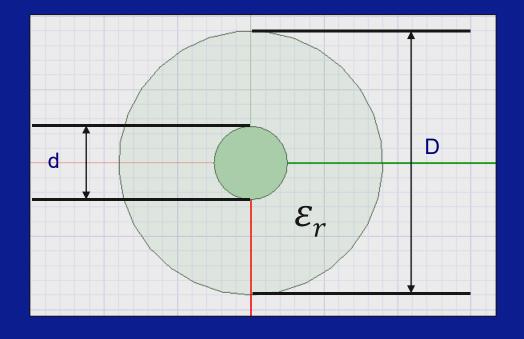
Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

#### **Benefits of Coax Via Ground Wall**

- Minimize impedance discontinuities
- Reduce noise and crosstalk from nearby signals
- Improve EMI
- Save space compared with adding extra ground vias



#### Coax via impedance estimate



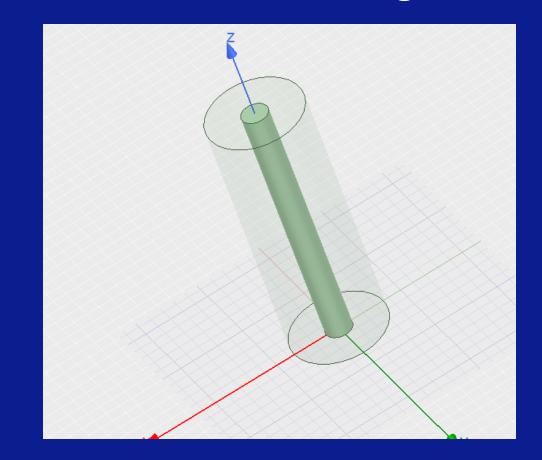
$$Z_0 = \frac{138 * \log_{10}(D/d)}{\sqrt{\varepsilon_r}}$$

- Z<sub>0</sub>: Characteristic impedance
- D: Outer conductor diameter
- d: Inner conductor diameter
- $\mathcal{E}_r$ : Relative permittivity of the dielectric



Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

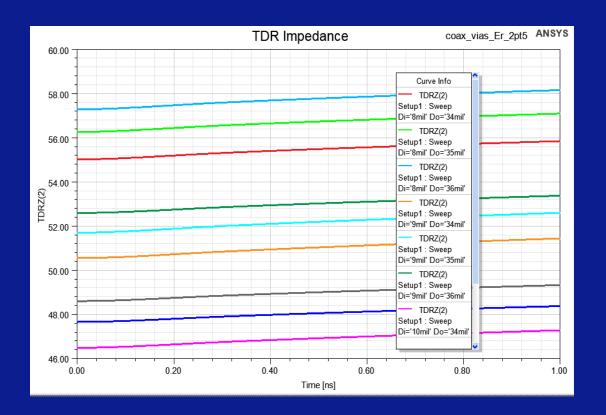
#### **Design of PAM4 Interposer** Coax via dielectric filing material 3D EM modeling



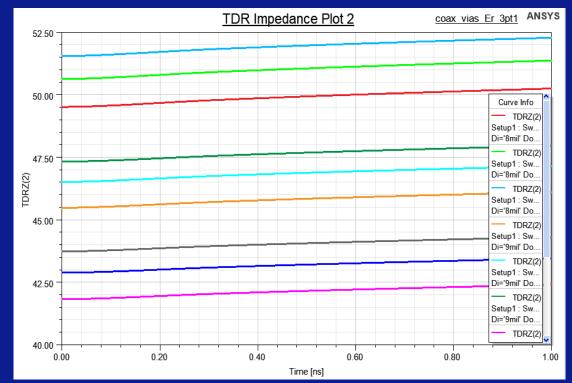
Optimize the outer conductor diameter D, inner conductor diameter d, and dielectric  $\mathcal{E}_r$  to meet target characteristic impedance  $Z_0$ 



Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation



 $\mathcal{E}_{\gamma}$ =2.5



 $\mathcal{E}_{\gamma}$ =3.1

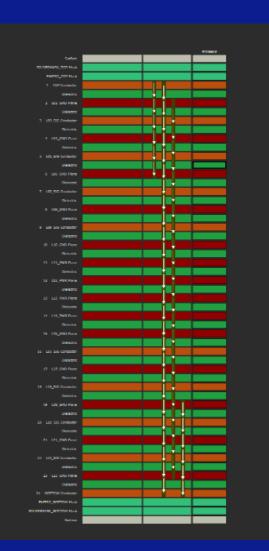


Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

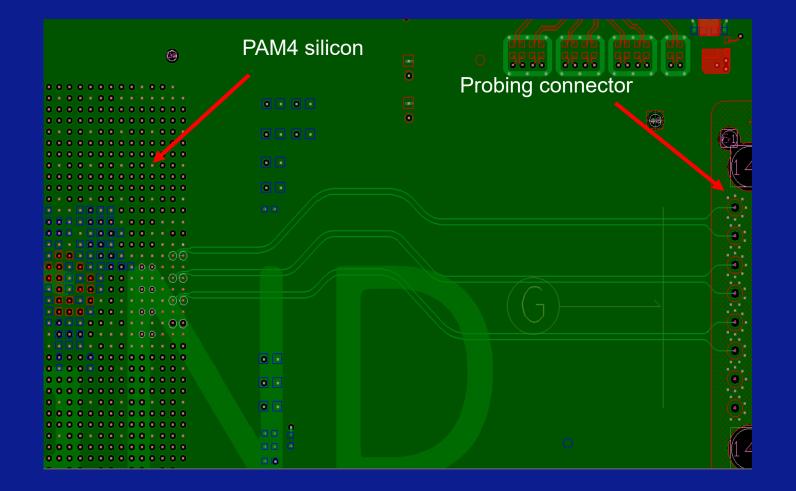
13 202

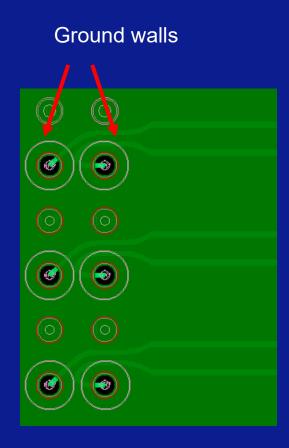
Objects			Types 🕨	
	Name	Layer	Layer Function	
		Surface		
	SOLDERMASK_TOP	Mask	Solder Mask	
	ENEPIG_TOP	Mask	Coating Conductive	
1	тор	Conductor	Conductor	
		Dielectric	Dielectric Prepreg	
2	L02_GND	Plane	Plane	
		Dielectric	Dielectric Core	
3	L03_SIG	Conductor	Conductor	
		Dielectric	Dielectric Prepreg	
4	L04_GND	Plane	Plane	
		Dielectric	Dielectric Core	
5	L05_SIG	Conductor	Conductor	
		Dielectric	Dielectric Prepreg	
6	L06_GND	Plane	Plane	
		Dielectric	Dielectric Prepreg	
7	L07_SIG	Conductor	Conductor	
		Dielectric	Dielectric Core	
8	L08_GND	Plane	Plane	
		Dielectric	Dielectric Prepreg	
9	L09_SIG	Conductor	Conductor	
		Dielectric	Dielectric Core	
10	L10_GND	Plane	Plane	
		Dielectric	Dielectric Prepreg	
11	L11_PWR	Plane	Plane	
		Dielectric	Dielectric Core	
12	L12_PWR	Plane	Plane	

Objects		Types 🕨	
	Name	Layer	Layer Function
		Dielectric	Dielectric Prepreg
13	L13_PWR	Plane	Plane
		Dielectric	Dielectric Core
14	L14_PWR	Plane	Plane
		Dielectric	Dielectric Prepreg
15	L15_GND	Plane	Plane
		Dielectric	Dielectric Core
16	L16_SIG	Conductor	Conductor
		Dielectric	Dielectric Prepreg
17	L17_GND	Plane	Plane
		Dielectric	Dielectric Core
18	L18_SIG	Conductor	Conductor
		Dielectric	Dielectric Prepreg
19	L19_GND	Plane	Plane
		Dielectric	Dielectric Prepreg
20	L20_SIG	Conductor	Conductor
		Dielectric	Dielectric Core
21	L21_GND	Plane	Plane
		Dielectric	Dielectric Prepreg
22	L22_SIG	Conductor	Conductor
		Dielectric	Dielectric Core
23	L23_GND	Plane	Plane
		Dielectric	Dielectric Prepreg
24	воттом	Conductor	Conductor
	ENEPIG_BOTTOM	Mask	Coating Conductive
	SOLDERMASK_BOTTOM	Mask	Solder Mask





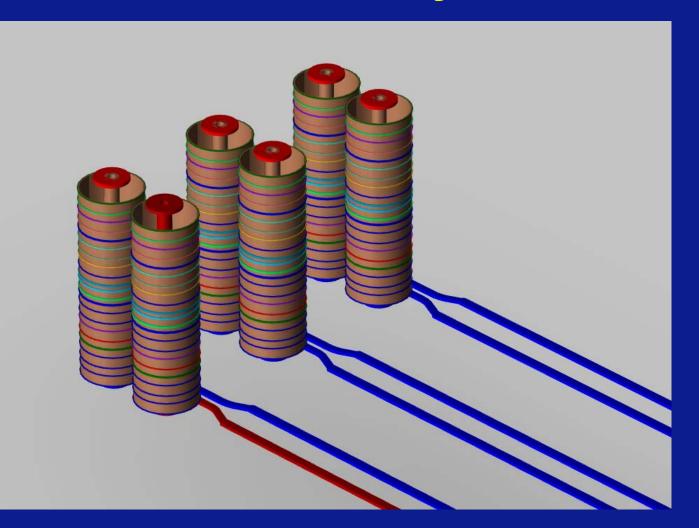






Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

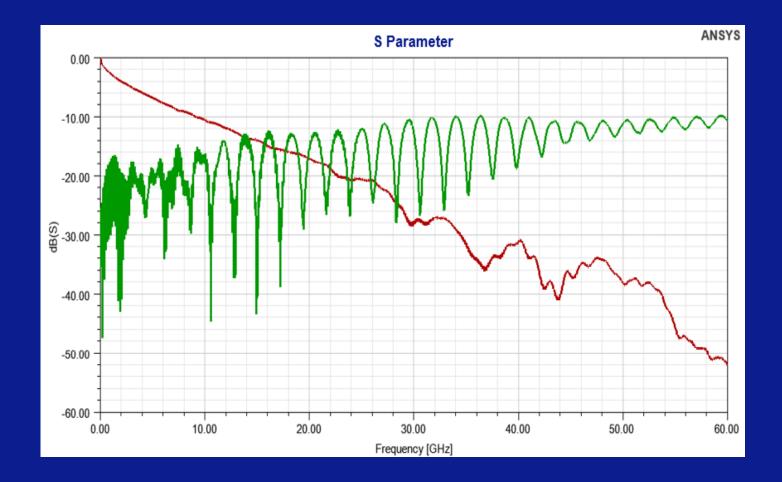
#### **Coax Via Differential Pairs Layout**





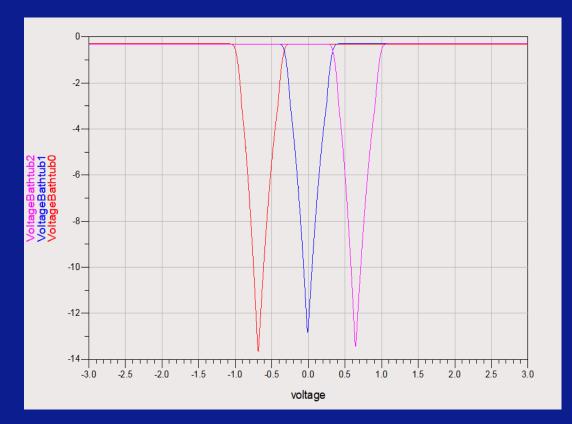
Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

## **Channel Modeling**

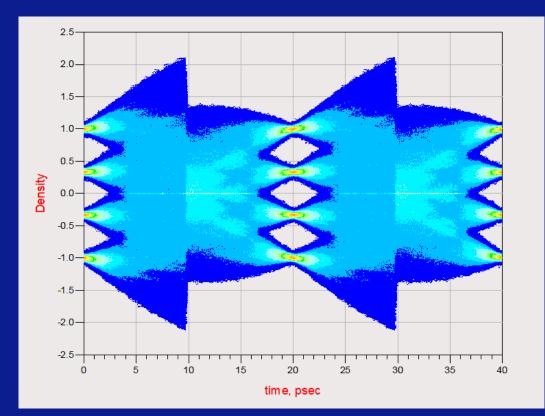


TestConX

#### **PAM4 Performance**



PAM4 bit error rate



Eye diagram of 100 Gb/s PAM4



Design and Analysis of a High-Performance PCB Interposer for 100G PAM4 Validation

18

## **Summary**

- High performance coax via PAM4 interposer
- Acceleration of PAM4 IP validation and time to market
- Good crosstalk isolation performance
- Compatible with current PCB manufacture process



## With Thanks to Our Sponsors!



## With Thanks to Our Sponsors!



## With Thanks to Our Sponsors!





## Cohu

The Market Leader in Test Interface Solutions for the Most Challenging Applications











Mobility

Precision Analog & Sensors

High End Digital

Automotive & Power



RF



#### **ELASTOMET SOCKET & INTERPOSERS**

- High performance and competitive price
- High speed & RF device capability
- Various customized design to meet challenge requirement

#### **POGO SOCKET SOLUTIONS**

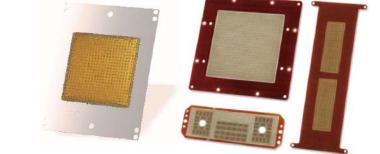
- Excellent gap control & long lifespan
- High bandwidth & low contact resistance

#### THERMAL CONTROL UNIT

- Extreme active temperature control
- Safety auto shut-down temperature monitoring of the device & thermal control unit
- Full FEA analysis & Price competitiveness

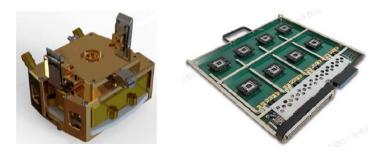
#### **BURN-IN SOLUTIONS**

- Direct inserting on the board without soldering
- Higher performance BIB solution







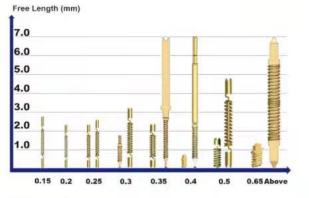


CONTACT ISC CO., LTD **ISC HQ** Seong-nam, Korea **ISC International** Silicon-valley, CA Tel: +82-31-777-7675 / Fax: +82-31-777-7699 Email: <u>sales@isc21.kr</u> / Web: <u>www.isc21.kr</u>

#### WIN IWIN Co., Ltd.

#### The test probe for high signal integrity at extremely high speed test

#### Spring probe by stamping



250 kinds of spring probe pin

300 kinds of test socket (44,000 Pin count socket possible)

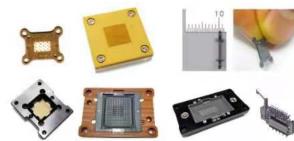
One piece spring probe

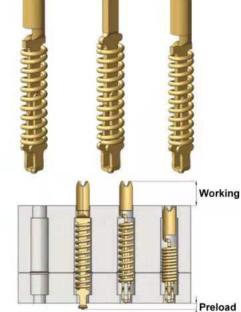
Three piece spring probe

High speed product → 0.63mm free length

spring probe pin available

Finest Pitch → 0.15mm Pitch





Spring probe by stamping

		Patented	
Pitch(mm)	Free Length(mm)	Current Carrying(Amps)	
0.15/0.2/0.25	2.17~	0.5~	
0.3	1.5~	1.5~	
0.35	2.08~	1.8~	
0.4	0.8~	2.5~	
0.5	1.5~	3.0~	
0.65	1.13~	9.0~	
0.8	3.14~	3.0~	

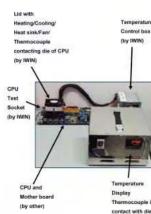
#### Automation Pin assembly and Quality control





Top Figure: Socket CRES, Force, Stroke test Bottom Figure: Data displayed

#### Socket and Lid



area of CPU.

(by IWIN)



Pin assembly (Fully automated machines)



- Stamped piece parts attached to a reel fed into the assembly machine

Assembled pins can be attached to a reel, or, supply in separate for socket assembly

#### Spring probe pins for High speed

Extremely short spring probes by stamping

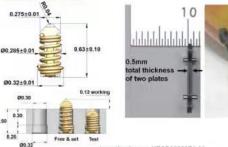




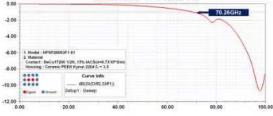
One piece spring prob **Design approach** 

0.50

Three piece spring probe







Return Loss - HPSP28063F1-01 0.00 -10.00 62.01GHz -20.00 -30.00 -40.00 -50.00 Curve Info dB(St(Dim),Dim)) -60.0 -70.00 0.00

#### SOLUTION

Copyright©2021 IWIN Co.,Ltd all right reserved Homepage. www.iwinsn.com Tel. +82-10-6417-7580 E-mail. aj@iwinsn.com

#### **High Performance Probe solution**

#### **COPYRIGHT NOTICE**

The presentation(s)/poster(s) in this publication comprise the proceedings of the 2021 TestConX Virtual Event. The content reflects the opinion of the authors and their respective companies. They are reproduced here as they were presented at the 2021 TestConX Virtual Event. The inclusion of the presentations/posters in this publication does not constitute an endorsement by TestConX or the workshop's sponsors.

There is NO copyright protection claimed on the presentation/poster content by TestConX. However, each presentation/poster is the work of the authors and their respective companies: as such, it is strongly encouraged that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author(s) or their companies.

"TestConX" and the TestConX logo are trademarks of TestConX. All rights reserved.

