VIRTUAL EVENT

TestConX

Presentation Archive May 3-7, 2021

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Dancing over Digital-Analog Dichotomy

"- Engendering Analog Signals from Digital Channels"

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Virtual Event • May 3 - 7, 2021





- Introduction
- Methodology
- Implementation and Validation
 - Analog signal generation
 - Digital stream capture
 - Filter circuit implementation
- Case Study
- Conclusion





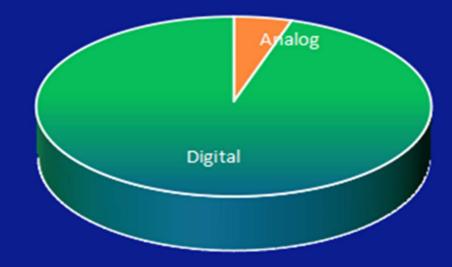
Why Testing Analog devices using Digital Channel?

 Acquiring analog instrument for minimal scope of analog resources in a SoC results in additional cost.



• Prelude of generation technique using pre-existing digital instrument.

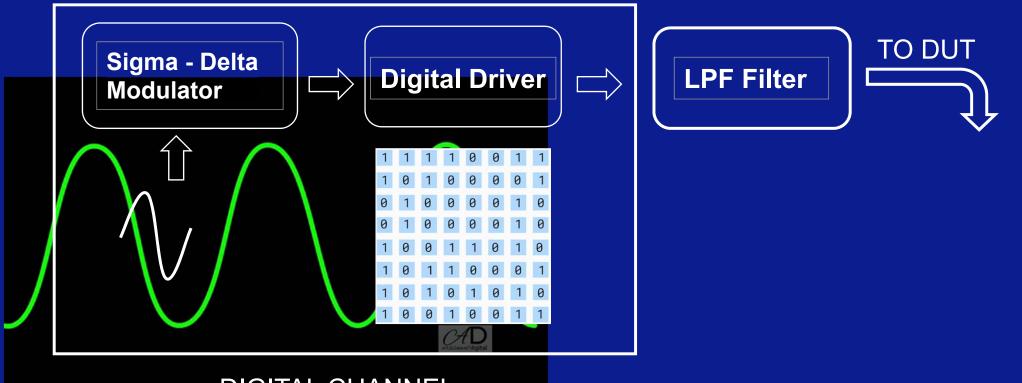
 Pulse Width Modulation Technique is independent of Tester platform; however the case study is implemented on Advantest 93K.







METHODOLOGY



DIGITAL CHANNEL





Generation of Digital Pulse Stream

• Sigma-Delta Modulation technique used for digital pulse generation.

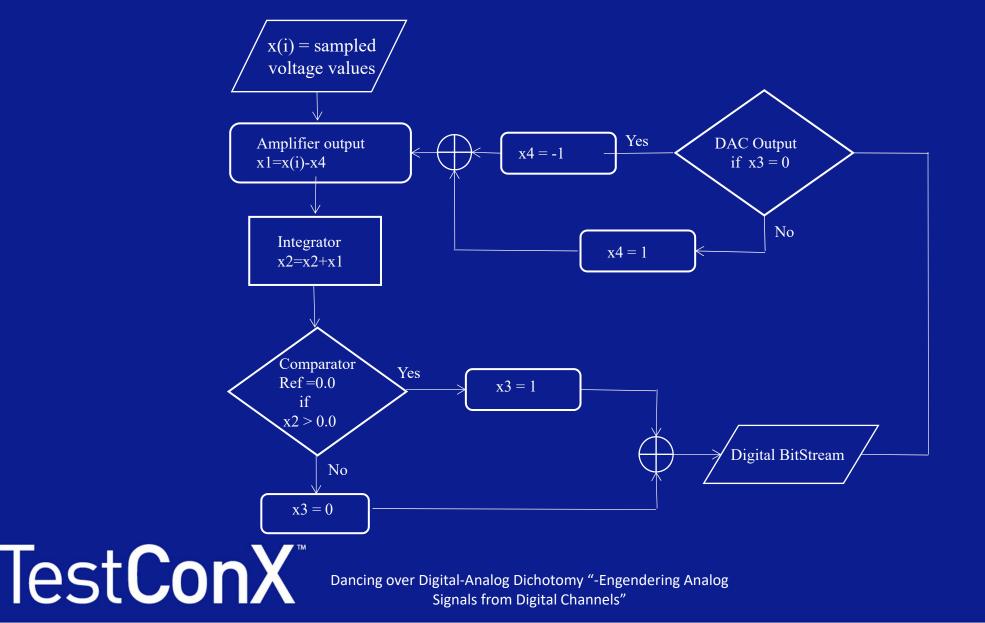
Why $\sum -\Delta$ modulation?

- High transmission efficiency ascertained by capturing the delta between consecutive samples.
- Oversampled input ensures reduction in noise power.
- Implements Noise Shaping function that pushes noise to high frequency.





FLOW CHART - \sum-\Delta MODULATOR



_° 2021

Generated Bit Stream

- Sine Wave : Fundamental freq (Fm) = 1KHz Sampling Freq (Fs) = 10KHz
- Intermediate calculation for equivalent bit stream generation.
- Engendered Bit Stream : 11101000101

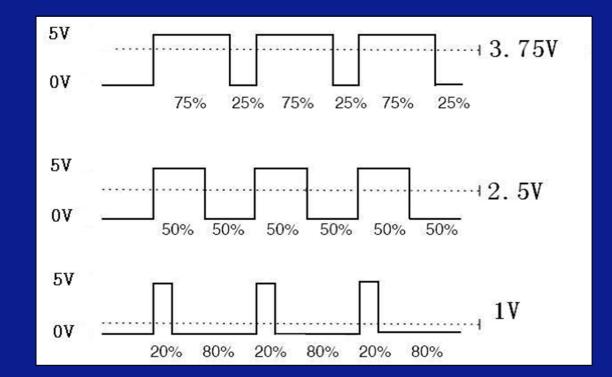
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X(i)	X1	X2	X3	X4
1.0000	0	1	1	1
0.9046	-0.0954	0.9046	1	1
0.6548	-0.3452	0.5594	1	1
0.3459	-0.6541	-0.0947	0	-1
0.0958	1.0958	0.0011	1	1
0	-1	-0.9989	0	-1
0.09493	1.09493	-0.90397	0	-1
0.34443	1.34443	-0.55954	0	-1
0.65329	1.65329	0.09375	1	1
0.90366	-0.09634	-0.00259	0	-1
0.99999	1.99999	0.9974	1	1

PWM

- Generated bitstream is given as X4 mode pattern to Digital channel.
- Variation in duty cycle of each period controls average output voltage.
- Higher the number of samples, more accurate the analog signal





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PWM Filter - Objectives

- Eliminates unwanted high-frequency signal components other than DC.
- Achieve the peak desired by the load circuit.
- Eliminate any DC offset.
- Minimize the analog signal ripple.

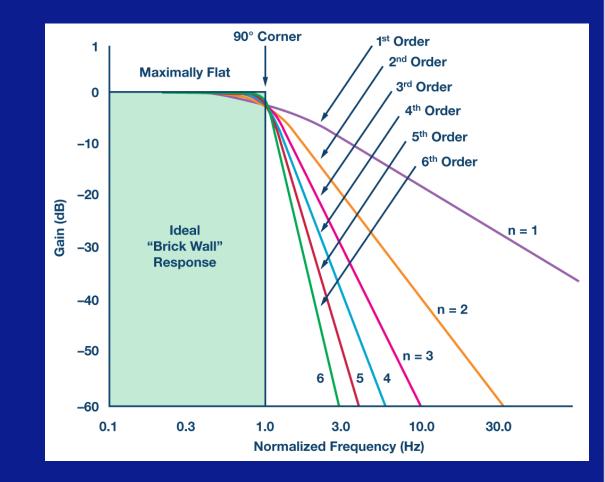




Filter Circuit Implementation

• Features of properly designed filter :

- Better level of attenuation and sharpness of cut-off frequency.
- Higher roll-off rate between Pass Band and Stop Band
- Assuring the correct quantizationnoise attenuation.





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Filter Recommendation

- Parameters considered for the filter :
 - Cut-off frequency
 - Order of the filter
 - Series resistance of filter
- Filter designs considerations for selecting cut-off frequency:

Waveform Type	Cut off frequency Selection (fco)	Filter Selection
Sinusoidal	< 1.5 x	Low Pass Filter
Cosine	< 1.5 x	Low Pass Filter
Ramp	Between 10 x and 100 x	Band Pass Filter



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Implementation

- Tester Platform
- Advantest 93k

- PS1600

- Instrument
- Order of modulator 1
- X-Mode 4
- LPF specs -

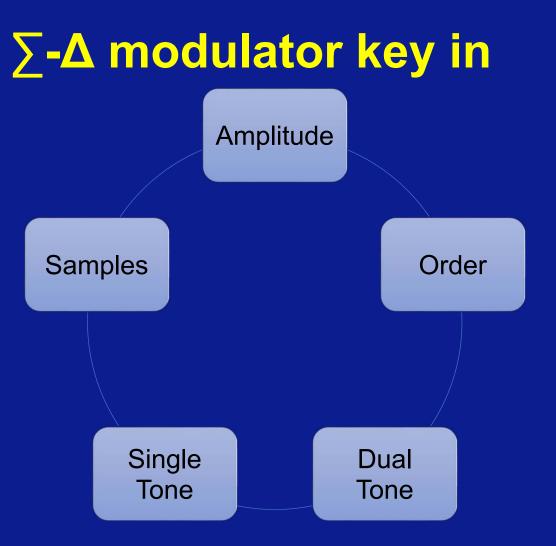
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Passive LC &7th order filter, with Fc = 1.3MHz & Zin = 6 ohm

Output Analog waveform (generated) -

Amplitude: 5VFm (Fundamental Freq): 1KHzFs (Sampling Freq): 5.5 MHz





 Formula for input cosine wave generation : x[i] = Amplitude *cos (2*pi*cycles/samples*i) +0.5;



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Test Conversion Details - vectors

- Generated Bit Stream saved in the mentioned location.
- User needs to copy to pattern file.
- Reference signal:

cycles = 3; samples = 65536

• Executed at frequency = 5.5MHz in X4 mode to obtain variation in duty cycle.

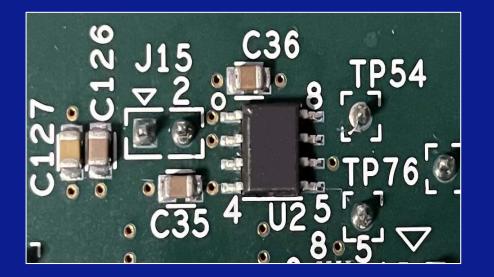
PWM_Patte				8 € \$	1.000.01.00	NG 7		
else et			-r - r					
Signal Size: 1,00	0 bytes		input (DVC)					
X-Mode Ar	ea							
Protocol				_				
Vector#	Instruction	Comment	L00	-				
137			1101	1				
138			1111					
139			0111					
140		1	1011					
141			1110					
142			1111					
143			0111					
144			1011					
145			1110					
146			1111					
147			0111					
148			1011					
149			1101					
150			1110					
151			1110					
152			1111					
153			0111					
154			1011					
155			1011					
156			1101					
157			1101					
158			1110					
159		1	1110					
160			1110					
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168			0111					

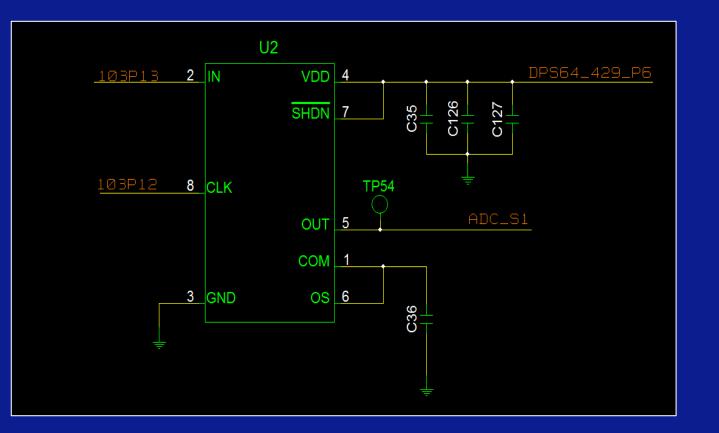




Circuit Implementation On - Board

• Board designed such that both the direct analog source and PWM converted analog source fed to input of ADC.









CASE STUDY

- A sampled study of two scenarios and corresponding comparison of signal parameters i.e., SNR and THD
 - i. Direct analog source input to the ADC device
 - ii. PWM converted analog source input to the same device
- Larger the SNR (Signal to Noise Ratio) specification, Better an instrument differentiates signal from the noise in measurements.
- THD (Total Harmonic Distortion) expresses the effect of high amplitude frequency components of a given signal frequency on the instrument.

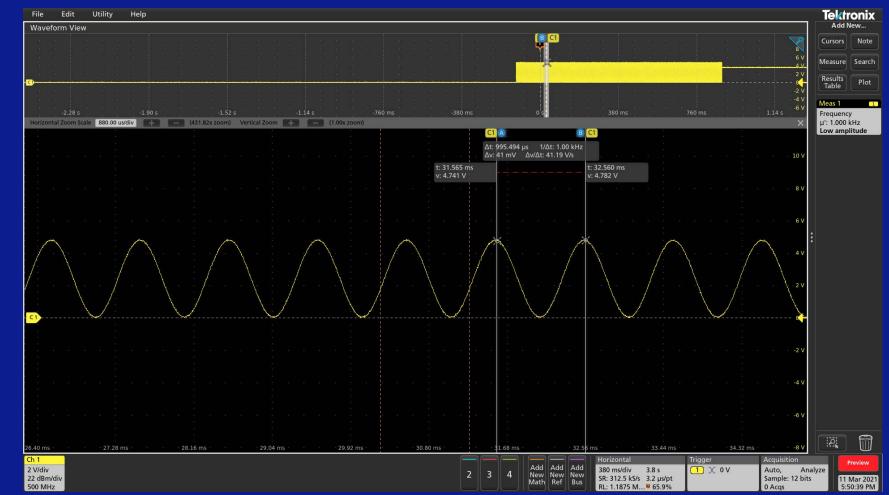




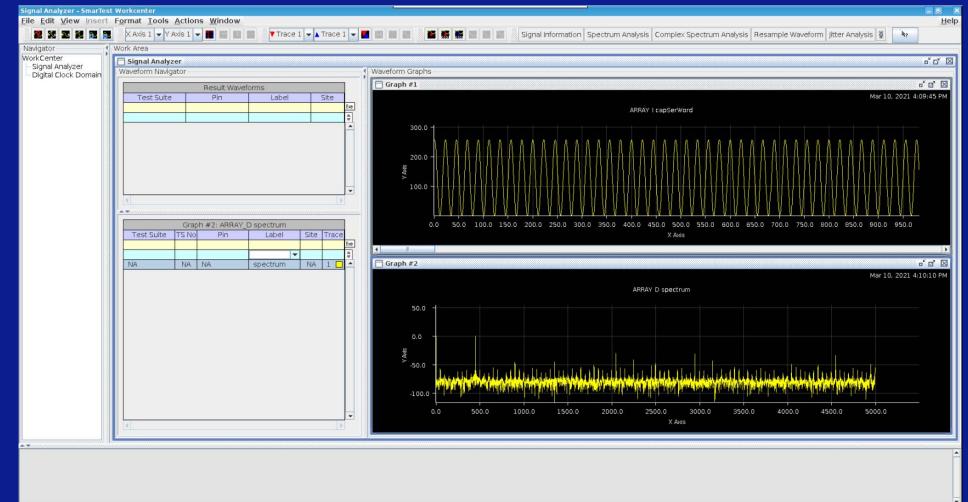
CASE STUDY 1 Direct analog source input from analog instrument

- Freq = 1KHz
- Amplitude = 5V
- Samples = 65536

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Output of ADC Device from Direct Analog Source



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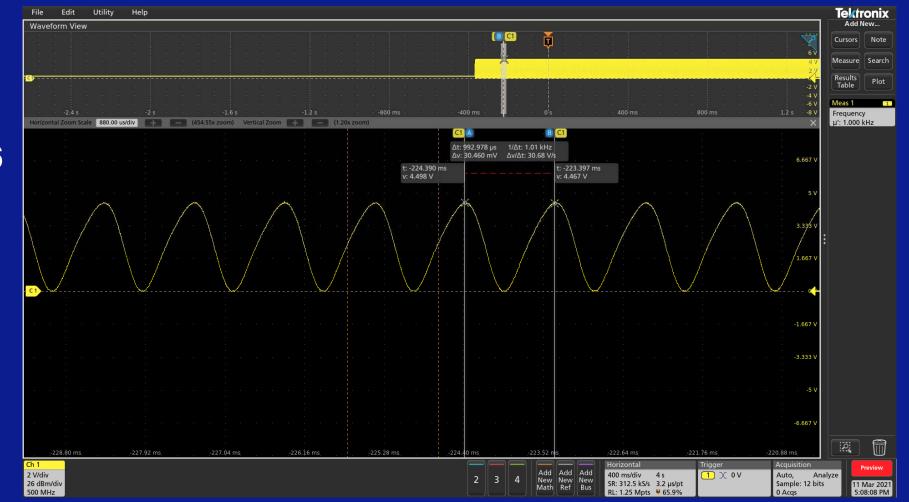
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E:0 W:0 F:0

CASE STUDY 2 Analog wave generated using PWM input

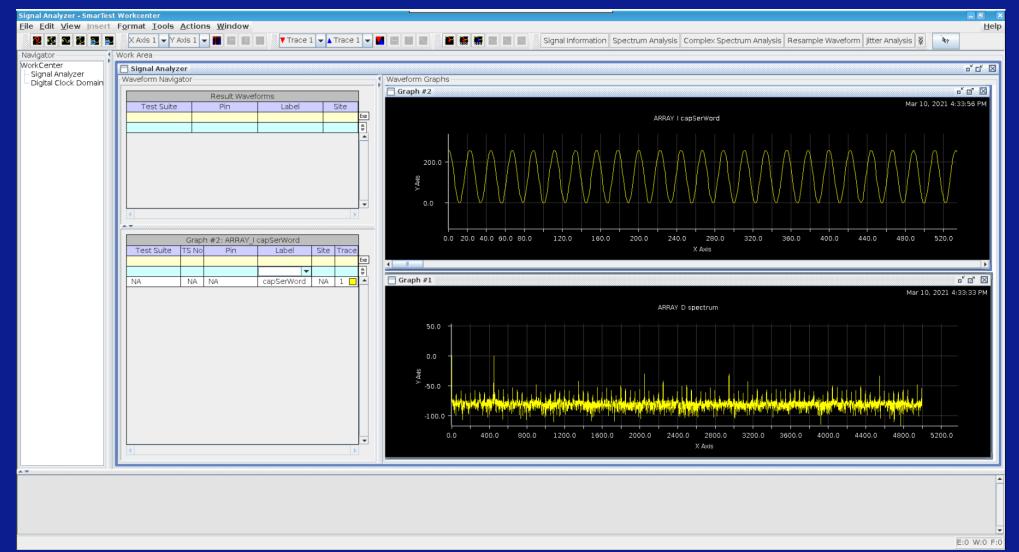
- Freq = 1KHz
- Amplitude = 5V
- Samples = 65536

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Output of ADC Device from PWM input



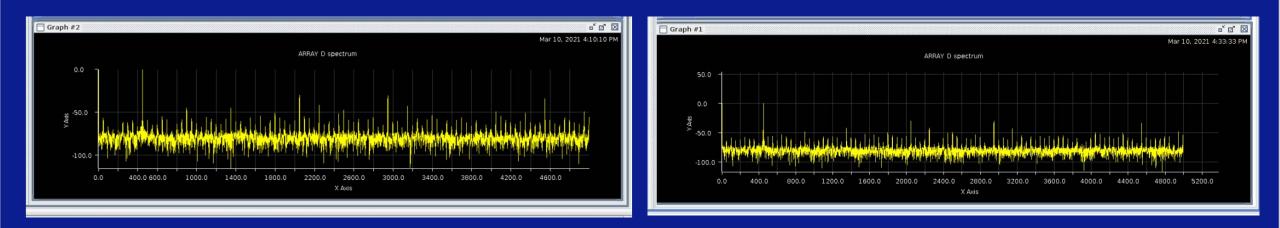
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Spectrum Comparison

Spectrum of Analog Instrument

Spectrum of PWM output



SNR = 65 dBTHD = -60 dB SNR = 63 dB THD = -58 dB

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CONCLUSION

• Implementation of this technique on tester platforms other than Advantest 93k and correlation of the results.

• Further scope for technique is to use on-board PLL after digital driver pin to exceed the limitation.





References

- Advantest Technical Document Center Topic No. 138518 "Enhancing Analog Signal Generation by Digital Channel Using Pulse Width Modulation".
- https://www.electronicdesign.com/technologies/analog/art icle/21798185/understanding-deltasigma-modulators





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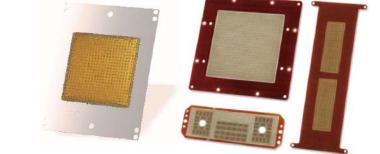
- Excellent gap control & long lifespan
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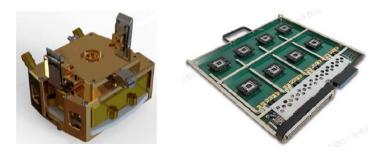
BURN-IN SOLUTIONS

- Direct inserting on the board without soldering
- Higher performance BIB solution







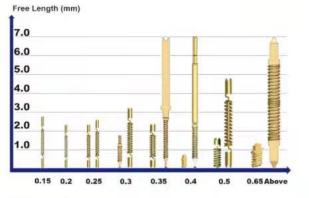


CONTACT ISC CO., LTD **ISC HQ** Seong-nam, Korea **ISC International** Silicon-valley, CA Tel: +82-31-777-7675 / Fax: +82-31-777-7699 Email: <u>sales@isc21.kr</u> / Web: <u>www.isc21.kr</u>

WIN IWIN Co., Ltd.

The test probe for high signal integrity at extremely high speed test

Spring probe by stamping



250 kinds of spring probe pin

300 kinds of test socket (44,000 Pin count socket possible)

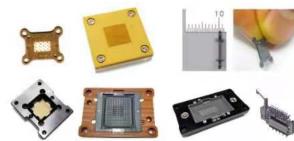
One piece spring probe

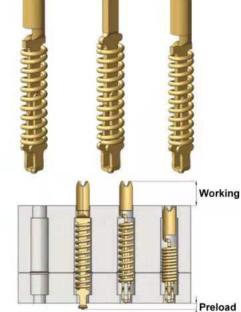
Three piece spring probe

High speed product → 0.63mm free length

spring probe pin available

Finest Pitch → 0.15mm Pitch





Spring probe by stamping

		Patented		
Pitch(mm)	Free Length(mm)	Current Carrying(Amps)		
0.15/0.2/0.25	2.17~	0.5~		
0.3	1.5~	1.5~		
0.35	2.08~	1.8~		
0.4	0.8~	2.5~		
0.5	1.5~	3.0~		
0.65	1.13~	9.0~		
0.8	3.14~	3.0~		

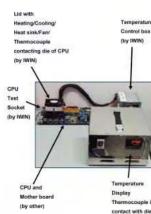
Automation Pin assembly and Quality control





Top Figure: Socket CRES, Force, Stroke test Bottom Figure: Data displayed

Socket and Lid



area of CPU.

(by IWIN)



Pin assembly (Fully automated machines)



- Stamped piece parts attached to a reel fed into the assembly machine

Assembled pins can be attached to a reel, or, supply in separate for socket assembly

Spring probe pins for High speed

Extremely short spring probes by stamping

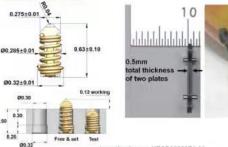




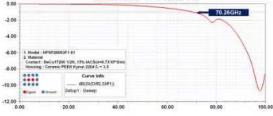
One piece spring prob **Design approach**

0.50

Three piece spring probe







Return Loss - HPSP28063F1-01 0.00 -10.00 62.01GHz -20.00 -30.00 -40.00 -50.00 Curve Info dB(St(Dim),Dim)) -60.00 -70.00 0.00

SOLUTION

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High Performance Probe solution

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