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Optimized PCBs for a 5G World

Don Thompson
R&D Altanova

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What are the New Challenges of 5G?

5G represents a significant jump in the frequencies normally seen on load boards. Not only that but the number of channels that must be tested for a given load board will drastically increase due to technologies like beam forming as well as increased site counts.

Frequency Rang 2:
24.25 GHz – 43.5 GHz

Beam-forming,
Multi band radios

High volume production

24.25-43.5 GHz load boards and probe cards

Tester microwave instrument resource sharing

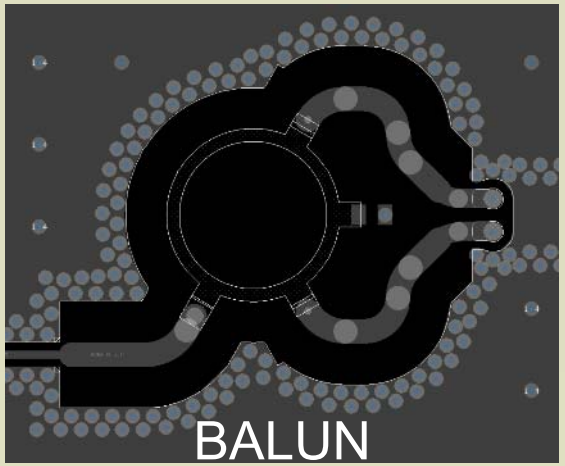
Massive increase in PCB and socket capabilities

What Does 5G Need in a Load Board?

In order to do reliable designs for 5G test systems we need the following:

1. A best practice guidebook for what trace structures and the PCB manufacturing guidelines
2. Reliable simulations correlated to measurements
3. A reliable design to fab process (repeatable and predictable performance)
4. Performance validation

Additionally, 5G requires filters, BALUNs, and other high quality trace structures



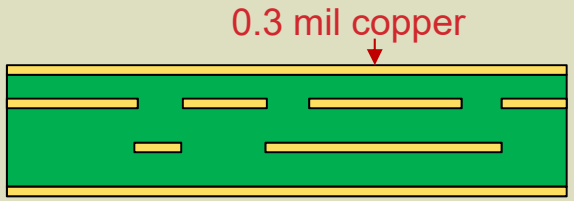
These high frequency structures must be right on the first try. There is no time for spinning the design to optimize the high frequency behavior

Defining Important Electrical Aspects of RF Transmission Lines

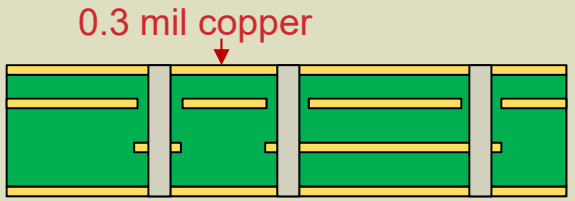
1. Insertion loss (IL) - How much TX energy arrives at RX
2. Return loss (RL) – How much TX energy returns to TX
3. Impedance – Same as RL but in time domain and from a pulse
4. Isolation – Signal to noise cause by other sources

Why Are Microstrips Hard? / How a PCB is made

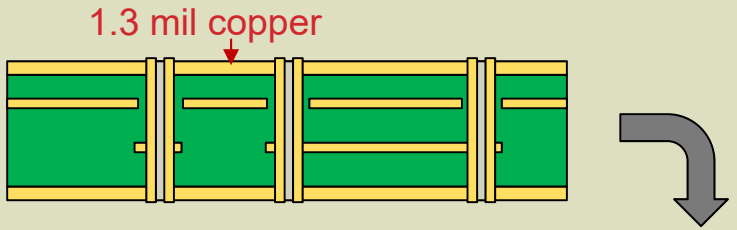
1. Laminate PCB



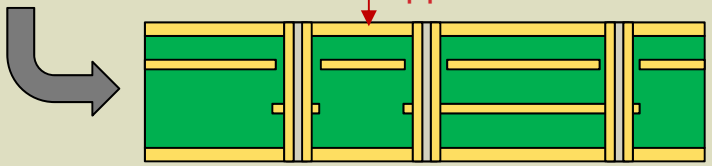
2. Drill Vias



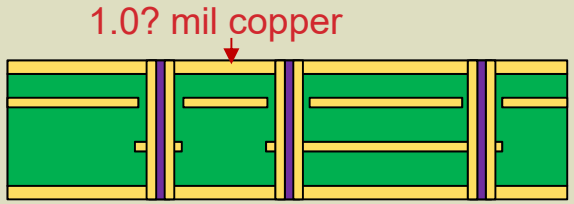
3. Plate Vias



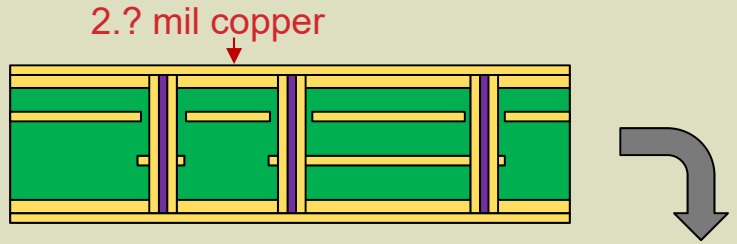
4. Planarize copper



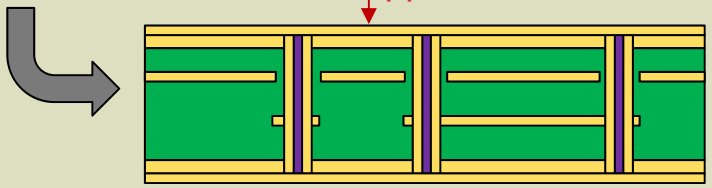
5. Fill Vias



6. Plate Over Fill



7. Planarize copper



The copper thickness on the surface of the PCB has a large tolerance because of these steps, so precise etching becomes very hard. That's why typical microstrip impedance tolerance on a thick PCB is only ±10%.

Microstrip Transmission Lines?

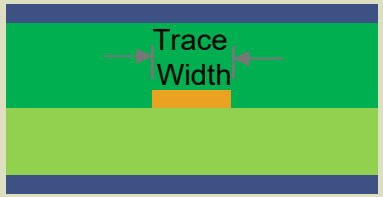
High frequency RF signals are typically on PCB surface layers because:

1. Vias are hard
2. Microstrip (surface) are lower loss than stripline (internal)
3. Vias are hard

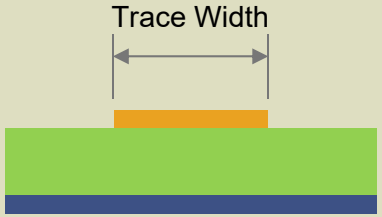
Therefore: this presentation will focus mostly on microstrip

Stripline vs. Microstrip vs. Coplanar Waveguide

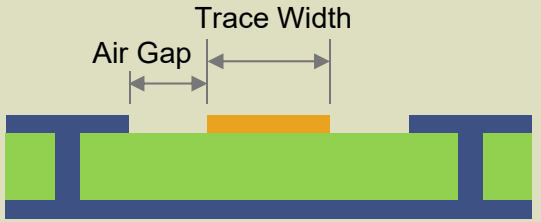
Stripline



Microstrip



CPW



- All trace structures have common impedance equations that have been empirically derived
- Typically stack-up defines the dielectric thickness. We will assume 5 mils dielectric thickness for most calculations.
- Dielectric is one of four categories: Crappy FR4, Mid-range, High-performance, & Teflon based
- Microstrip and CPW are on PCB exterior
  - Exterior copper is thicker due to via plating operations
  - Exterior copper tolerance control is much worse than interior copper
  - Exterior copper typically has lower impedance control due to worse tolerances
  - Microstrip and CPW have the significant 5G advantage of having no vias or no via stubs

Common Dielectric Loss Examples

	Dielectric Constant	Loss Tangent	Category
FR4	4.2	0.0200	Crappy but cheap
Nelco 4800-20	3.8	0.0070	Mid-Tier
Rogers 4003	3.4	0.0027	High-Performance
Tachyon 100G	3.0	0.0021	High-Performance
Meteorwave 8000	3.3	0.0016	High-Performance
Taconic EZ-IO-F	2.8	0.0015	Teflon Based
Rogers 3003	3	0.0010	Teflon Based

Determines trace width
Not super interesting

Determines loss

Dielectric Simulation Data – A Starting Point

Crappy FR4 < Mid-Tier < High-Performance

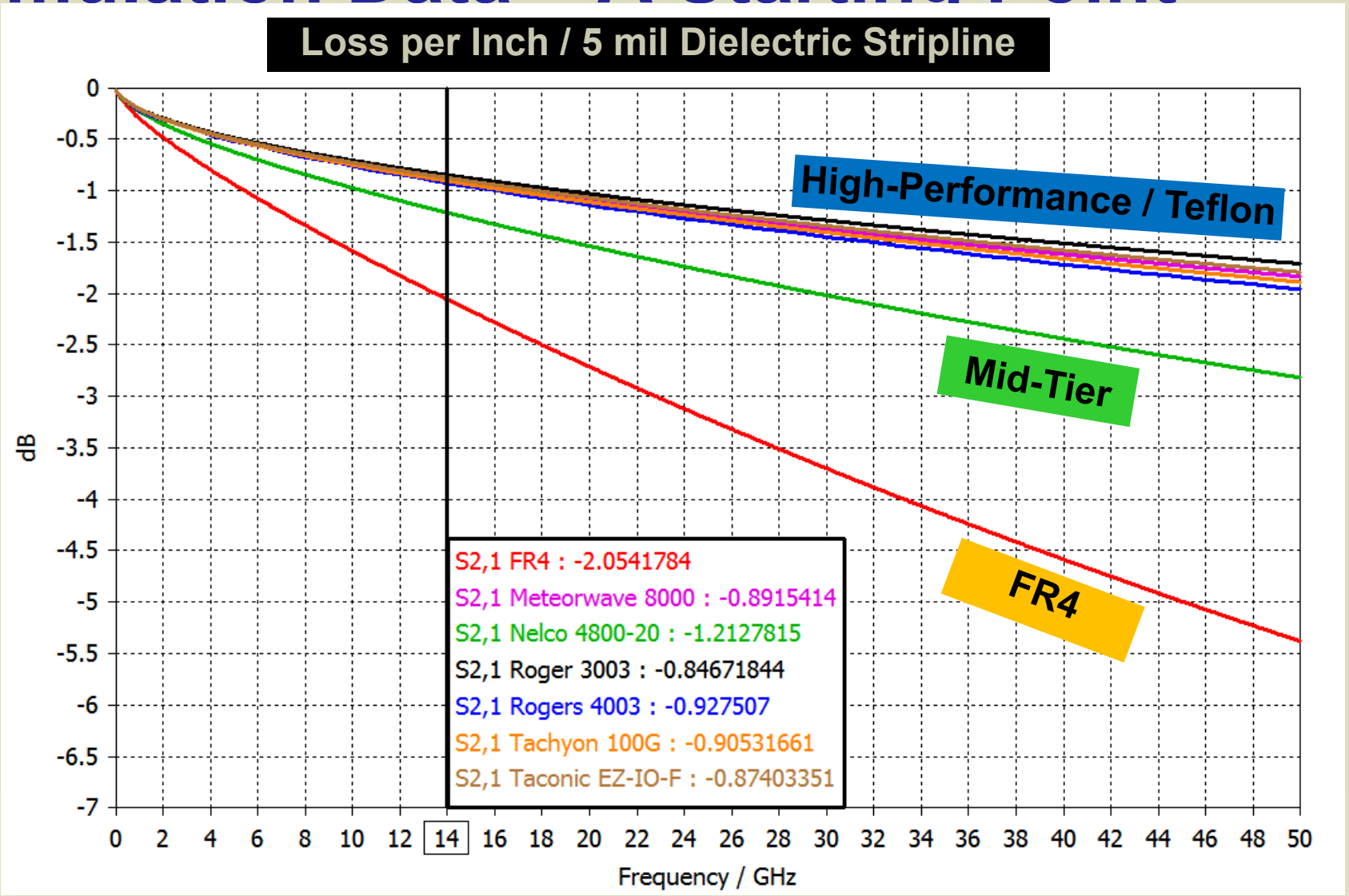
BUT

The difference between High-Performance and Teflon and each other is less than a 10% difference

<u>Conclusion</u>:

1.7” Mid-Tier = 1” FR4

2.3” High-Per = 1” FR4



Transmission Line Loss: Conventional Wisdom & What We Think We Know

General design & manufacturing:

- Microstrips are better than stripline
- Co-planer waveguide are better than microstrips
- Surface roughness has a significant impact on performance insertion loss (but how much?)
- Published dielectric loss-tangents are trustworthy (Simulation vs. Measurements)

Plating & Etch:

- Gold wrap should make microstrips & CPWs better
- Nickel may / should have a negative impact on performance
- Does ENEPIG provide any benefit?
- How do different etch processes affect performance? (three flavors)

Extras:

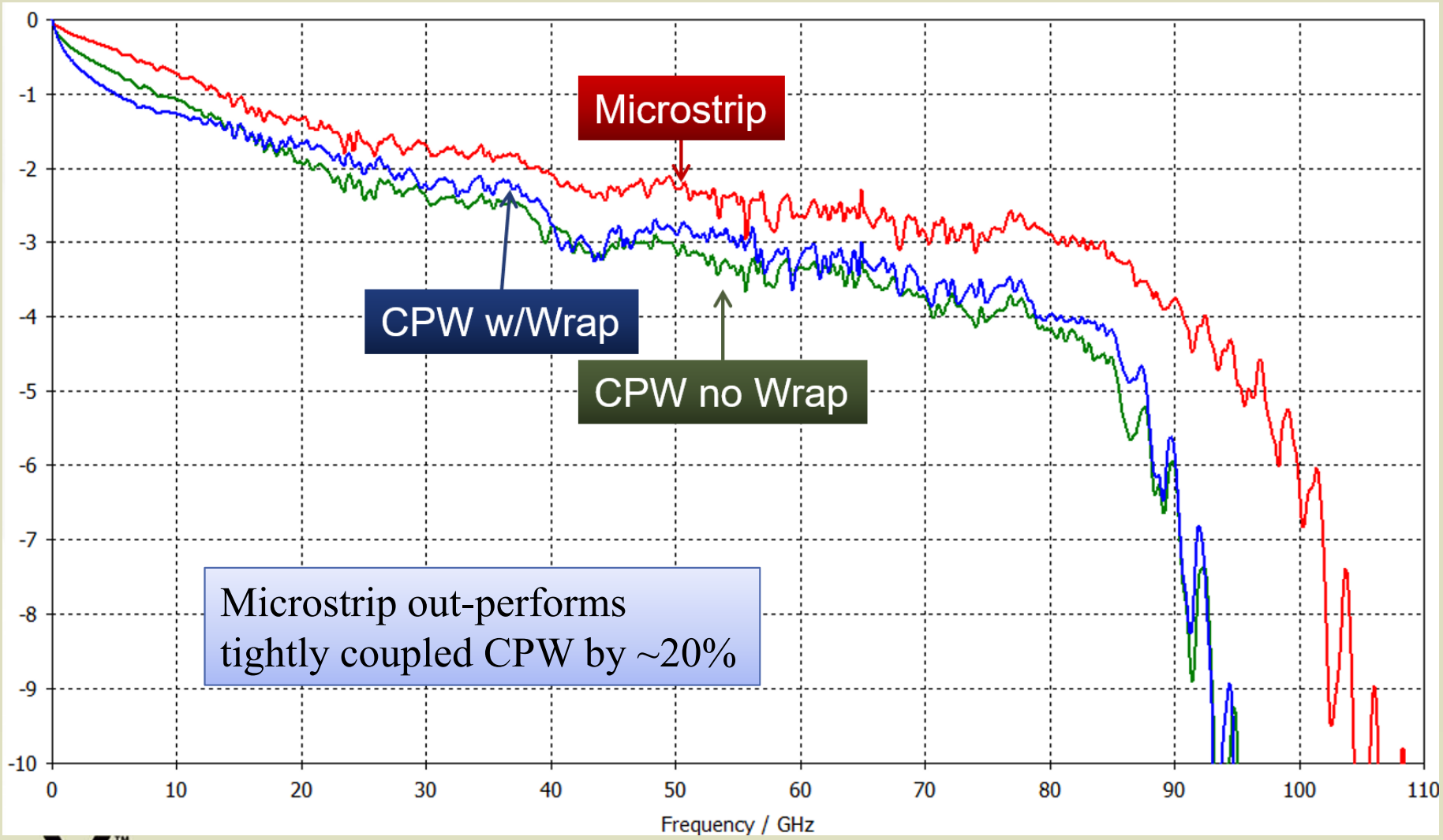
How much does the CPW dimensions affect the loss?

1st Round: Microstrip vs CPW

Microstrip:

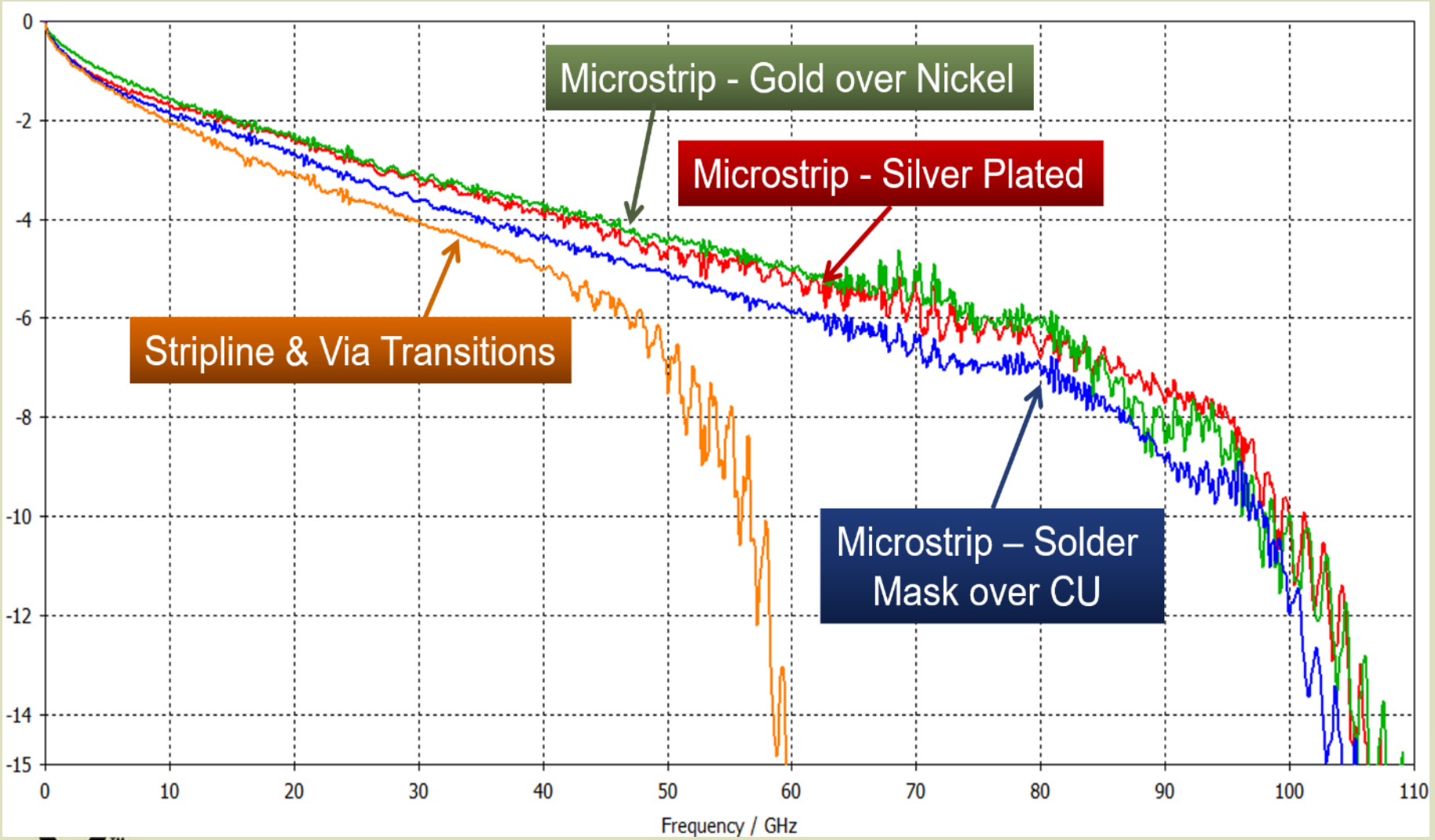
CPW:

Wrap = 10 µin gold around edges of microstrip

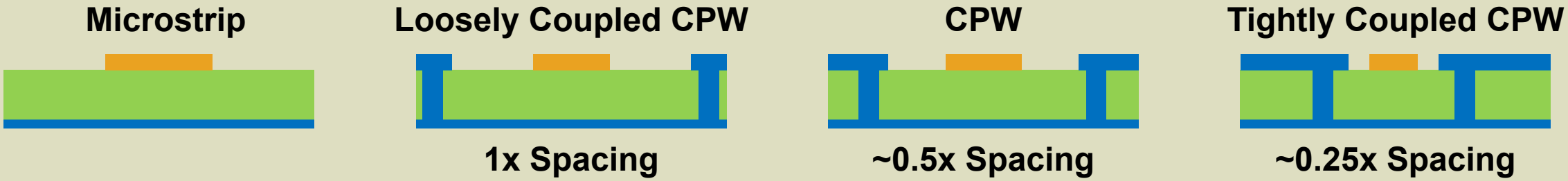


1st Round: Plating Variations

- Stripline's Via has fallout ~45 Ghz
- Silver plating provides no benefit
- Solder mask DK provides additional loss
- Simple Gold over Nickel is easiest and best performing



Transmission Line Loss



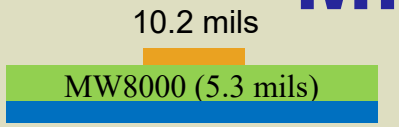
- "1x" spacing means the center conductor width equals the gap width
- Technically this is Grounded Co-Planar Waveguide, but it's also commonly referred to as CPW

Literature quotes:

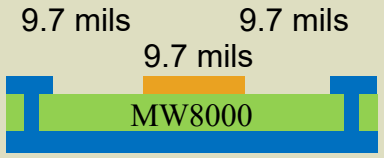
- *"PCB fabrication issues have less impact on microstrip circuits than GCPW circuits." -TRUE*
- *"Microstrip … suffers increased circuit losses into the millimeter-wave frequency range, making the circuit technology less efficient for use at frequencies of 30 GHz and beyond." - FALSE*

Microstrip vs CPW Measurements

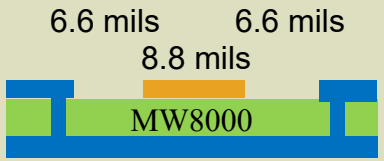
Micro-strip



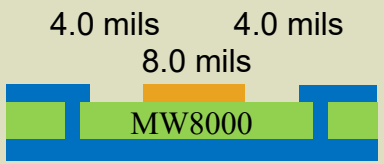
CPW 1X



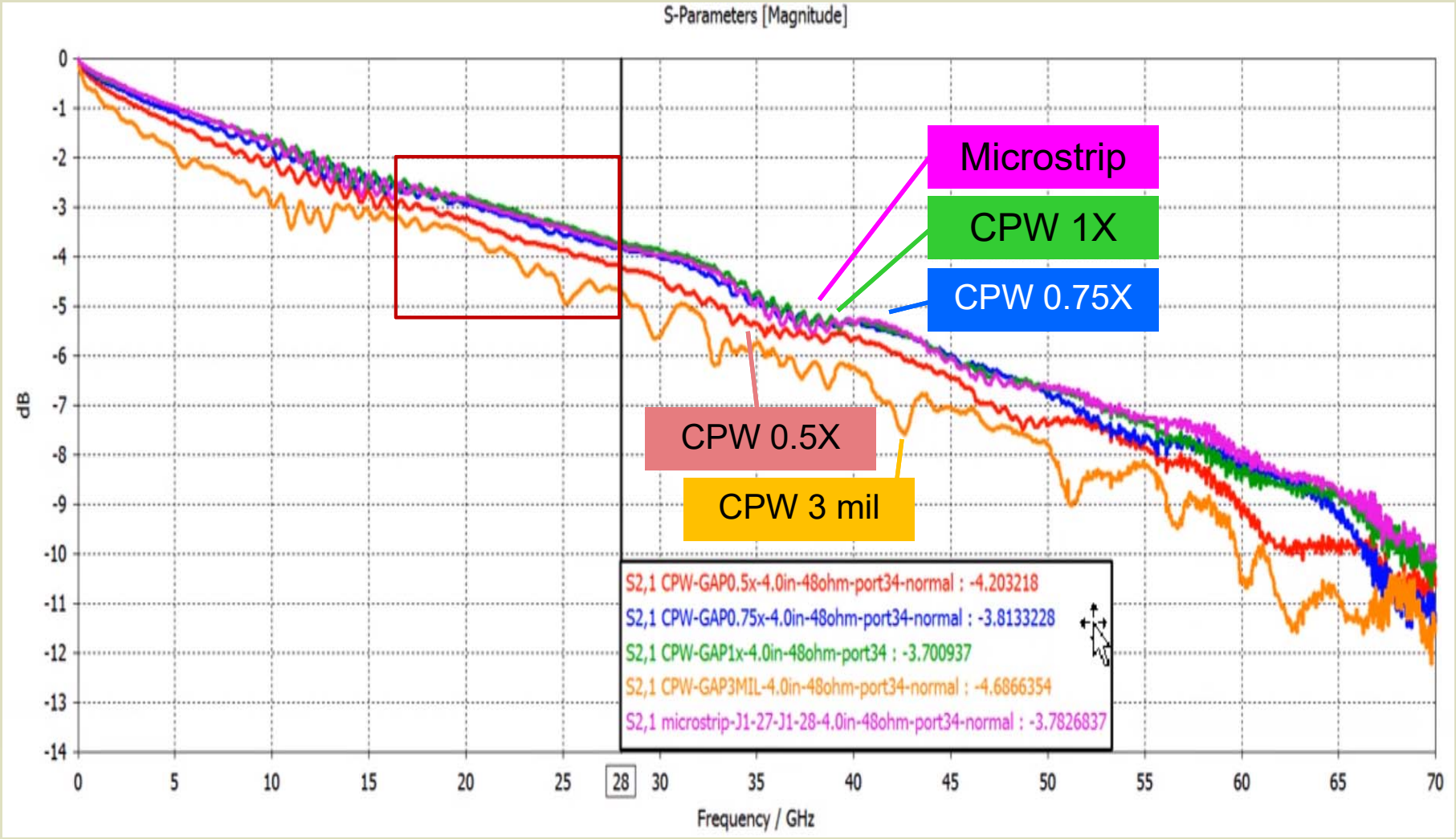
CPW 0.75X



CPW 0.5X



CPW 3 mil



Microstrip vs. CPW results

- Microstrip provides lowest loss transmission line for a given stack-up
- Loosely coupled CPW is equal to microstrip
- The closer the CPW spacing is, the higher transmission line loss

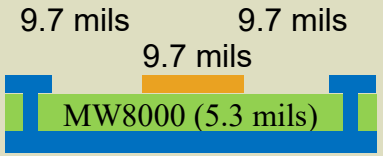
Takeaways:

- CPW's only benefit is in shielding and isolation!
- Target 0.75X or 1X CPW spacing when used

Simulation vs Measurements

- Simulations are based strictly off published specs found in datasheets
- Not all specs are equal and many values are not easily independently measurable
- Real measured loss measures many factors we take on faith:
  - Surface roughness, loss tangent, perfect trace shapes, and accurate loss equations are all required for accurate simulations

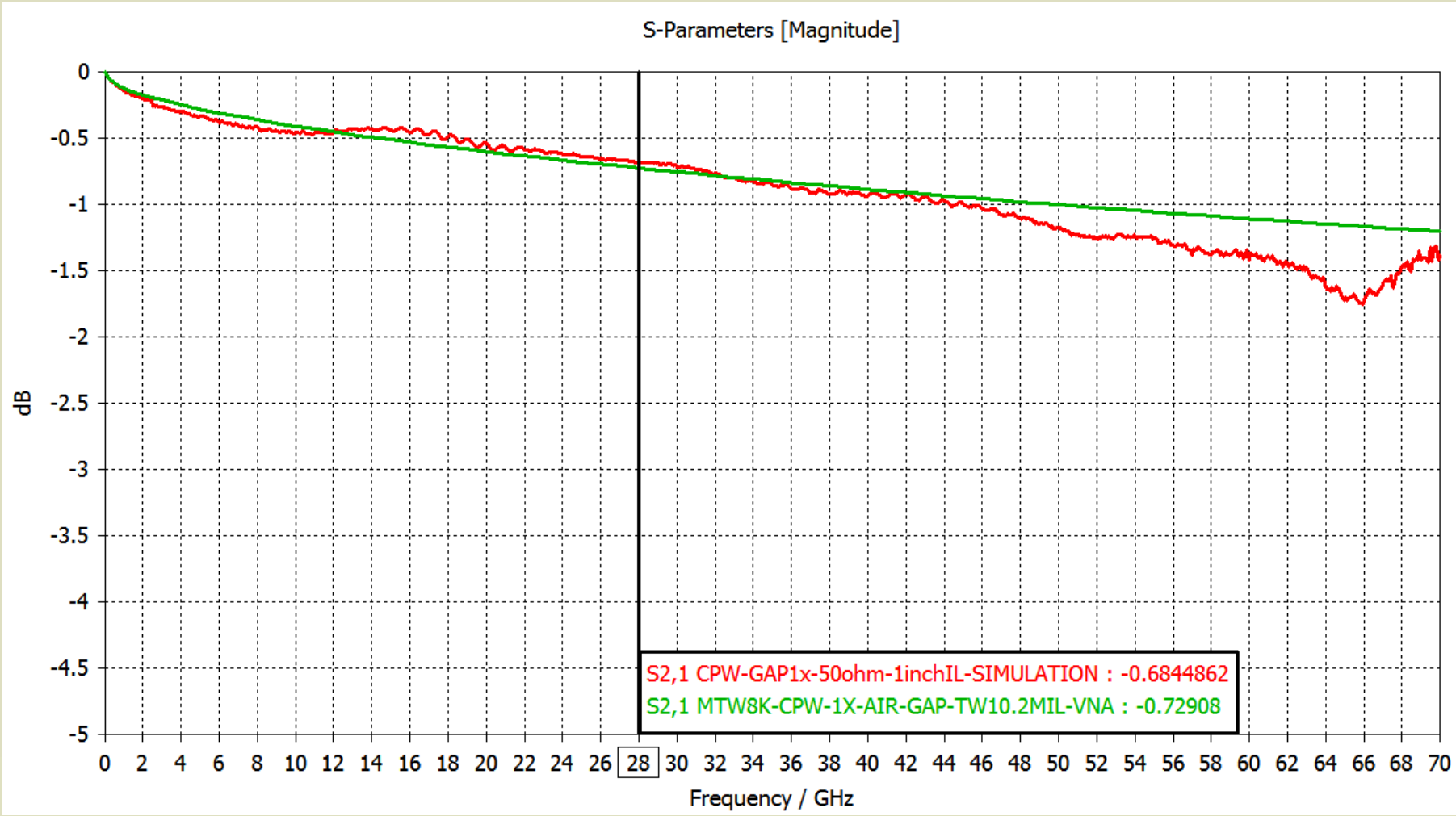
Trace Simulation vs Reality (1)



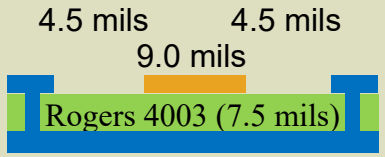
CPW 1X

MW8000 Dielectric

1” Trace Loss



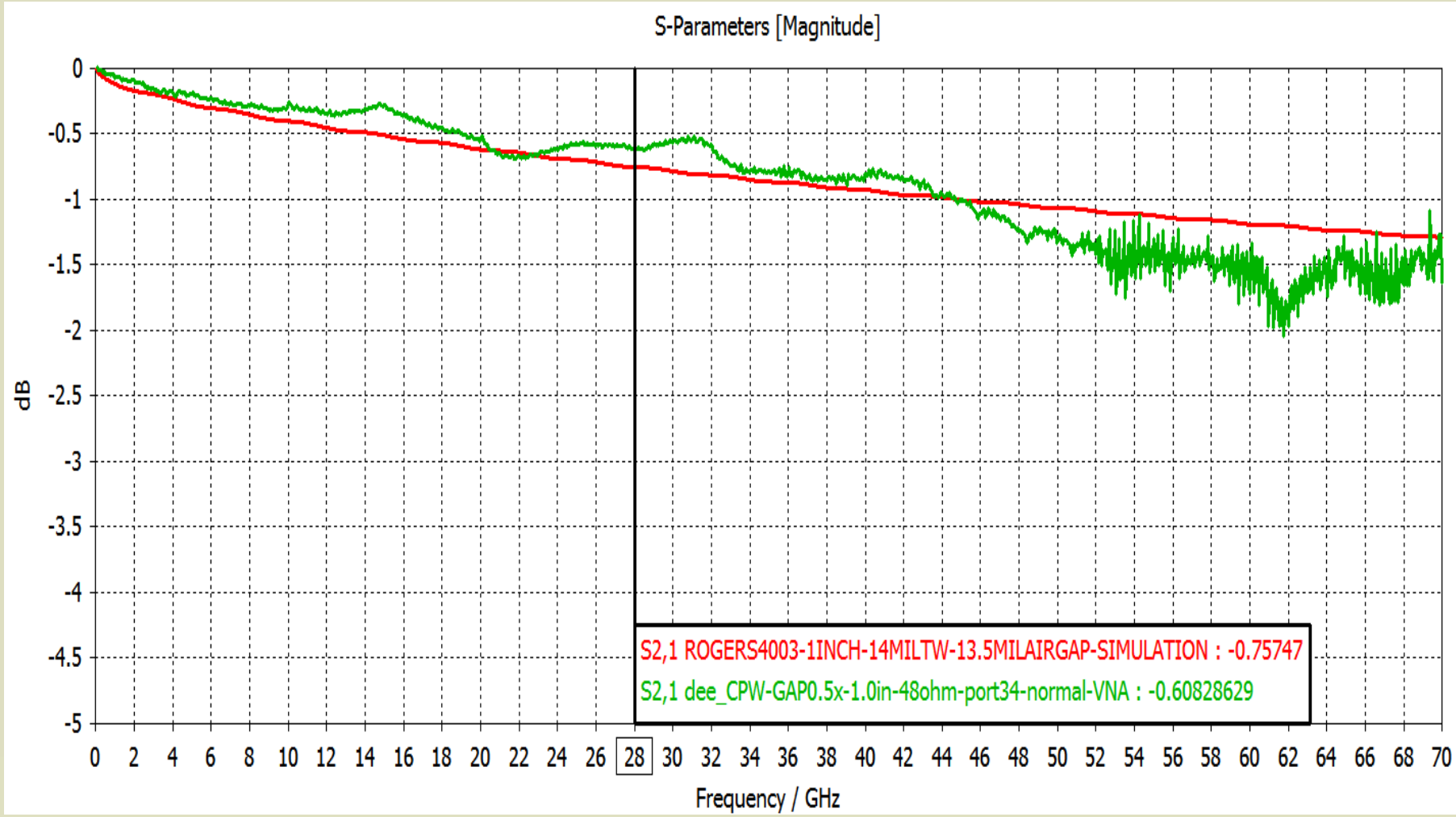
Trace Simulation vs Reality (2)



CPW 0.5X

Rogers 4003

1” Trace Loss



Conclusions

What have we learned so far:

- Trace simulations work pretty well until around 45 GHz where they deviate
- CPW 0.75X is preferred transmission line
- Standard Gold over Nickel are preferred plating. No solder-mask over trace.

Remaining Questions

- How much is transmission line loss affected by etching differences?
- How much is transmission line loss affected by alternate plating options?
  - ENEPIG
  - Wrap plating
- How do other dielectrics compare simulation vs measured? Do other dielectrics out or under perform their simulated performance?
- Best via options
- Best connector options

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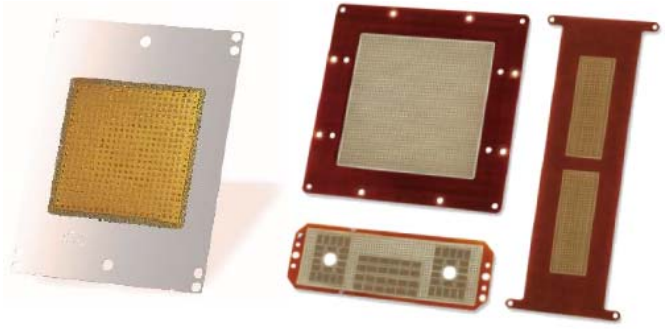
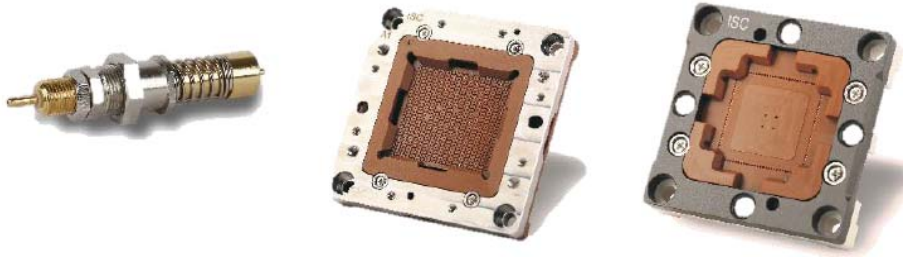


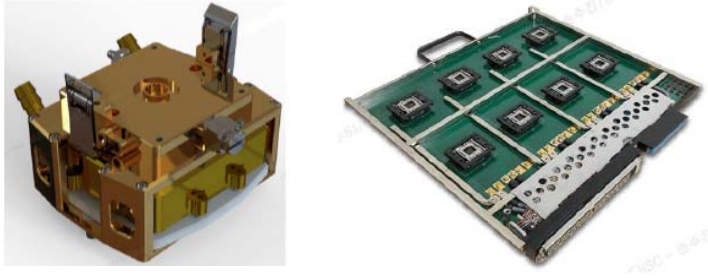
POGO SOCKET SOLUTIONS

- Excellent gap control & long lifespan
- High bandwidth & low contact resistance



THERMAL CONTROL UNIT

- Extreme active temperature control
- Safety auto shut-down temperature monitoring of the device & thermal control unit
- Full FEA analysis & Price competitiveness



BURN-IN SOLUTIONS

- Direct inserting on the board without soldering
- Higher performance BIB solution

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ISC CO., LTD

ISC HQ
Seong-nam, Korea

ISC International
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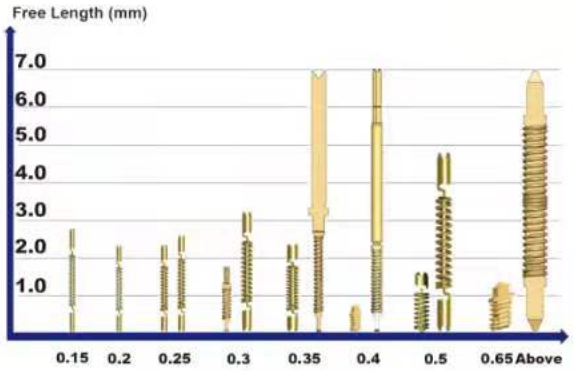
IWIN Co., Ltd. The test probe for high signal integrity at extremely high speed test

Spring probe by stamping



250 kinds of spring probe pin

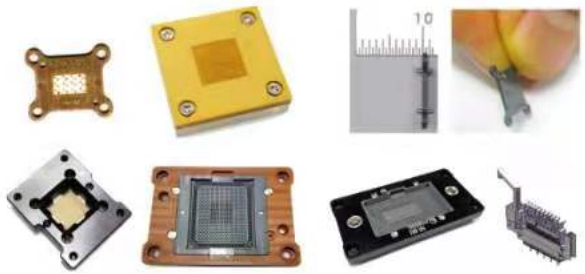
300 kinds of test socket (44,000 Pin count socket possible)

One piece spring probe

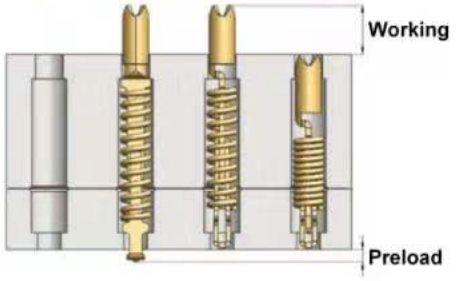
Three piece spring probe

High speed product → 0.63mm free length spring probe pin available

Finest Pitch → 0.15mm Pitch



Spring probe by stamping

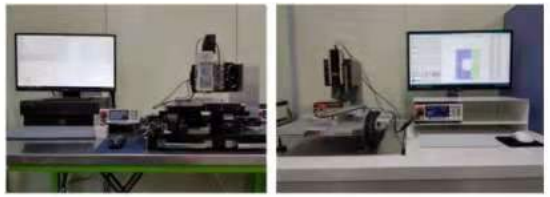


Patented

Pitch(mm)	Free Length(mm)	Current Carrying(Amps)
0.15/0.2/0.25	2.17~	0.5~
0.3	1.5~	1.5~
0.35	2.08~	1.8~
0.4	0.8~	2.5~
0.5	1.5~	3.0~
0.65	1.13~	9.0~
0.8	3.14~	3.0~

Automation

Pin assembly and Quality control



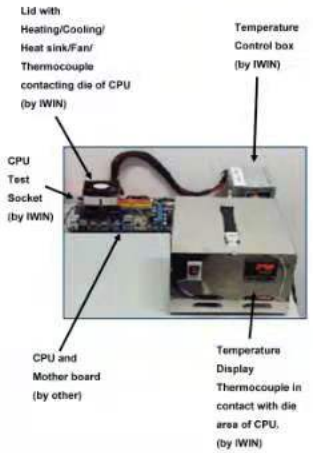
Top Figure: Socket CRES, Force, Stroke test

Bottom Figure: Data displayed

Top Figure: Socket CRES test

Bottom Figure: Data display 5,903 pins socket

Socket and Lid



Pin assembly

(Fully automated machines)

- Stamped piece parts attached to a reel fed into the assembly machine

- Assembled pins can be attached to a reel, or, supply in separate for socket assembly.

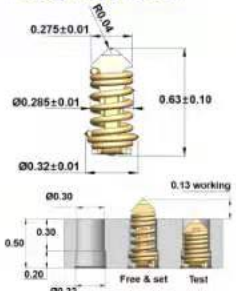
Spring probe pins for High speed

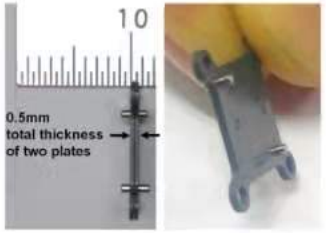
Extremely short spring probes by stamping

One piece spring probe

Three piece spring probe

Design approach





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High Performance Probe solution

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