Next Generation Test Cell / Test Operation

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TestConX中国 China

Virtual ▪ October 27-29, 2020

INTEL CLOUD BASED REMOTE DEBUG

intel

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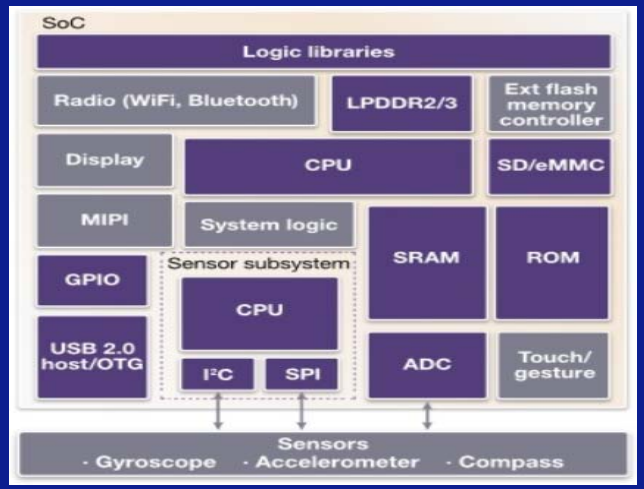
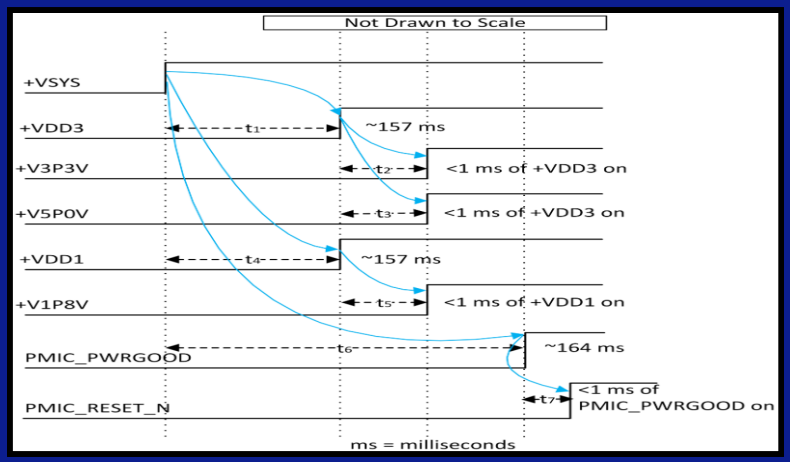
What is Power Sequencing Test?



Example of SoC Block Diagram



Power On Timing Sequences

- **Objective:** Measure Power-On & Power-Down Timings & Voltages for SoC blocks
- **Criticality:** Ensure products functionality

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How to Perform Power Sequencing Test

Scenario	32 Power Rails	8 Ch Oscilloscope	# of Test Cycle
BEST-CASE SCENARIO			× 4 = 1
WORST CASE SCENARIO "Cascade" mode			× 2 = 4

Quality Risk? Acquisitions are taken over multiple power cycles
Caused variations in device characterization

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Cost to Perform Power Sequencing Test

Requirements:

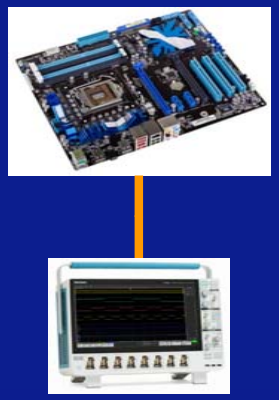
- Oscilloscopes
- Hours to execute power sequencing test
- Engineer/technician head count support

Variations:

- Manual characterization method by using naked eyes
- Result accuracy may vary by person/skills

Current Limitation:

- Long execution time
- High cost to perform the test
- Inaccurate test results
- In-depth technical skills required
- Physical touch support required



OscilloscopeSss…

Engineer or Technician

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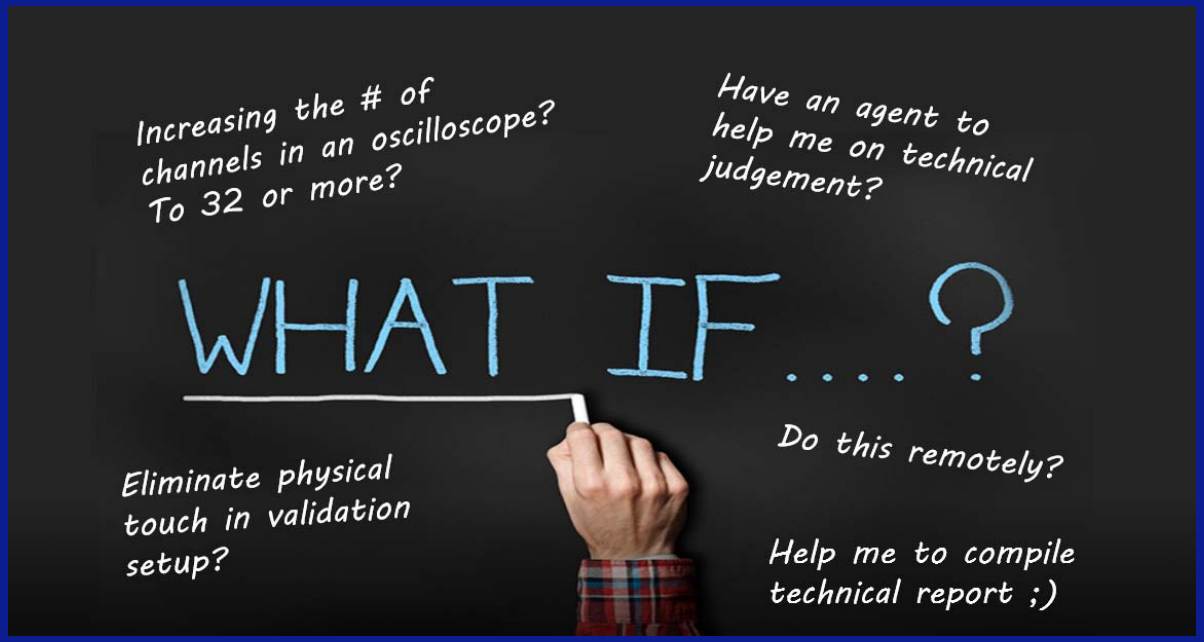
Demand leads to Innovations!



Goal: Automate Power Sequencing Test with automation solutions

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Solution Overview

- Applied Field Programmable Gate Array (FPGA) to construct a customize multi-channels oscilloscope to perform Power Sequencing Test.
- All test results are captured and compared to a pre-defined recipe (pass condition) and report out detail summaries

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Hardware Specifications

- Up to 1MSPS sampling rate per channel
- 36 single ended channels
- 8-bit resolution per channel
- 1Mohm input impedance
- 3 selectable input voltage ranges (0-5V and 0-20V and +/- 10V)
- 1-minute data capture bandwidth per channel
- Simultaneous sampling with same clock for all channels
- 1 selectable single channel edge triggering (rising/falling) with adjustable threshold
- User selectable trigger position (as 0-99% of total capture buffer)

Power Sequencing Tester

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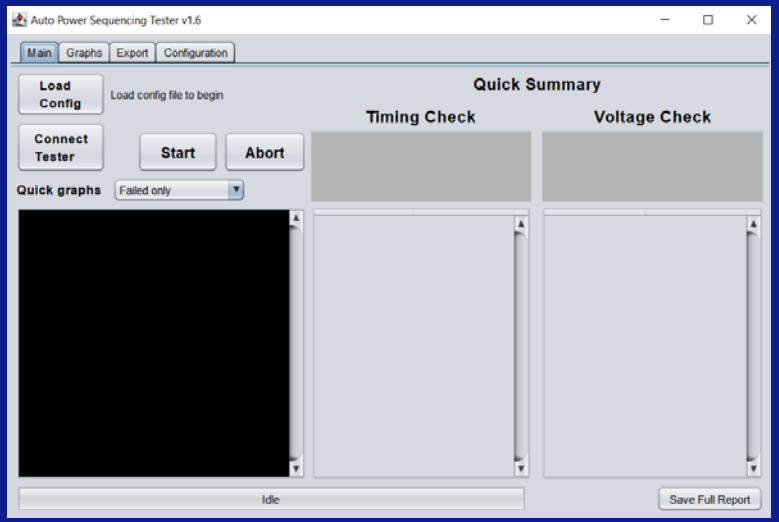
Software Specifications

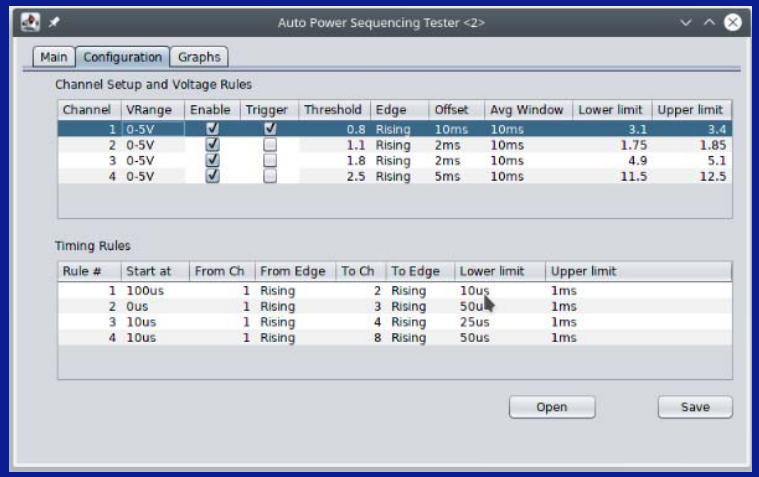
- load config file, save to config file, arm/disarm (start/stop), generate report, save wave data file
- Individual waveform display for each channel, with vertical/horizontal zoom features
- Detail waveform display tool for advance control/settings
- Selectable time range (max 1-minute)
- User defined pass/fail condition, with profile/recipe settings
- Voltage rule checking features



Software GUI

Profile/Recipe Settings and Configuration

- Selectable voltage range for each channel (0-5V, 0-20V, +/-10V)
- Timing checking rules
- Voltage checking rules
- Edge detection for timing check
- User specify triggering channel, edge (rise/fall)
- Voltage threshold and voltage delta selection
- Profile/recipe save features



Profile/Recipe Configurations

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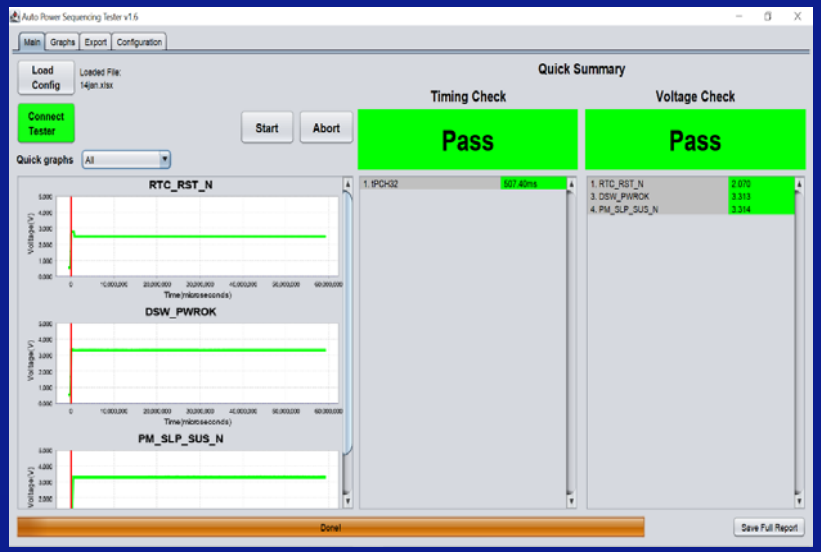
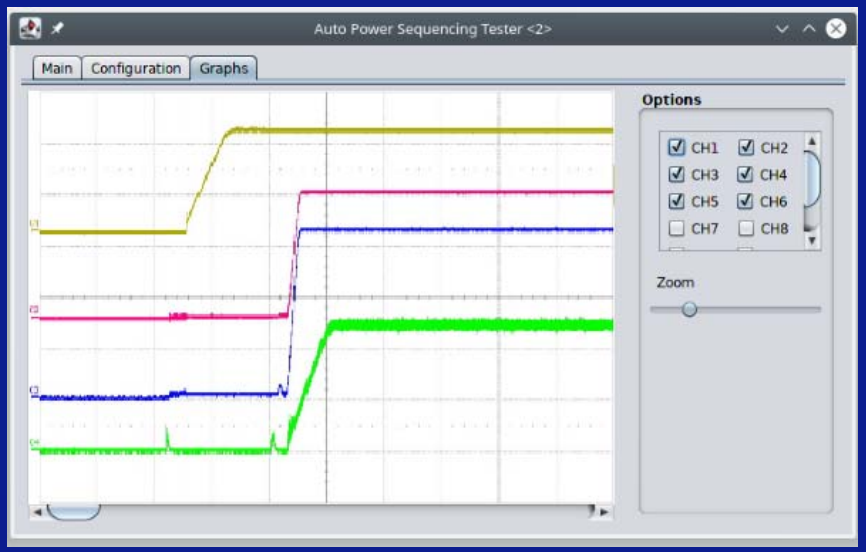
Sample Test Results



Result Summary Page



Signal Level Analysis

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Sample Recipe Configurations

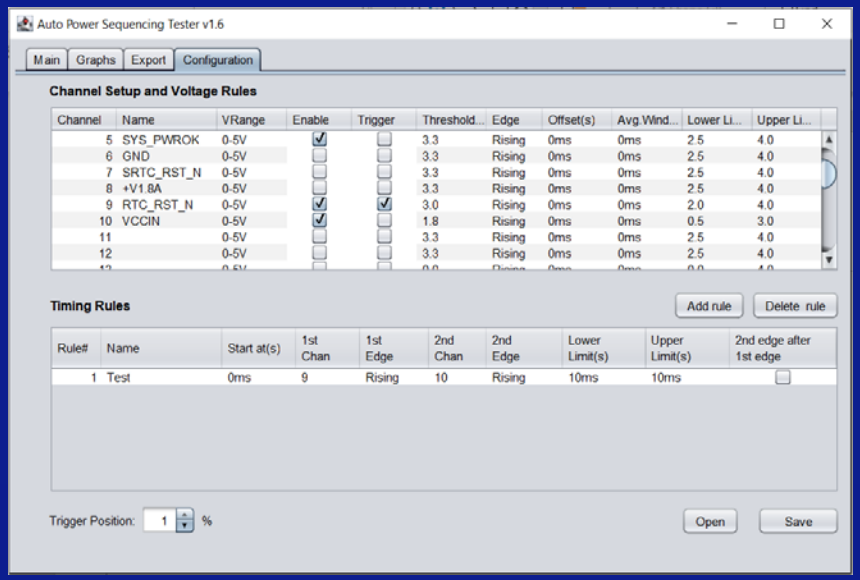
Voltage Rules

Channel Setup				Voltage Checking Setup				
CH#	Vrange	Enable	Threshold	Edge	Offset	Window	Low Limit	High Limit
1	5V	TRUE	2.5V	Positive	10ms	10ms	4V	4.5V
2	5V	FALSE	1.2V	Positive	10ms	10ms	2V	2.5V
[1-36]	[0 to 5V, 0 to 20V, -10 to 10V]	[True or False]	[voltage value]	[Positive, Negative]	[time delay after edge]	[Averaging window]		

Timing rules

Rule#	Start at	FROM		TO			Low Limit	High Limit
		CH#	Edge	CH#	Edge			
1	0us(default)	Ch05	Positive	Ch08	Positive		10ms	20ms
2	58ms	Ch02	Positive	Ch08	Positive		11ms	50ms
[1-99]	[any number at increment till en capture]	[Ch01 to Ch20]	[Positive, Negative]	[Ch01 to Ch20]	[Positive, Negative]			

Test Condition and Setup Sheet



Profile/Recipe Configurations

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Sample Test Report Overview

Power Sequencing Tester Report

Software Version: 1.6
Creation Date: 2020-01-14T14:22:46.7301587+08:00[Asia/Singapore]
Config file: C:\Users\WorkStation 1\Desktop\PST\PST_v1p4\14jan.xlsx
Overall result: Pass
Voltage check result: Pass
Timing check result: Pass

Voltage checking rules and results

Showing only enabled channels.

Chan #	Name	Meas. Voltage Range	Channel Enable	Trigger	Threshold	Trigger Edge	Meas. offset time	Avg. window time	Lower Limit	Upper Limit	Measured value	Result	Fail reason
1	RTC_RST_N	0-5V	True	False	1.5V	Rising	10.0000ms	10.0000ms	2.0V	3.0V	2.097V	PASS	
3	DSW_PWROK	0-5V	True	True	1.5V	Rising	10.0000ms	10.0000ms	2.5V	4.0V	3.314V	PASS	
4	PM_SLP_SUS_N	0-5V	True	False	1.5V	Rising	10.0000ms	10.0000ms	2.5V	4.0V	3.307V	PASS	

Timing checking rules and results

Rule #	Name	Start checking from	From Channel	From Channel Edge	To Channel	To Channel Edge	Lower Limit	Upper Limit	2nd edge only after 1st edge	Measured value	Result	Fail reason	Chart
1	tPCH32	-1.0000ms	3	Rising	4	Rising	95.0000ms	5.0000s	true	1.0212s	PASS		Go

Sample Test Report in HTML form

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Setup & Application Overview

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Power Sequencing Tester

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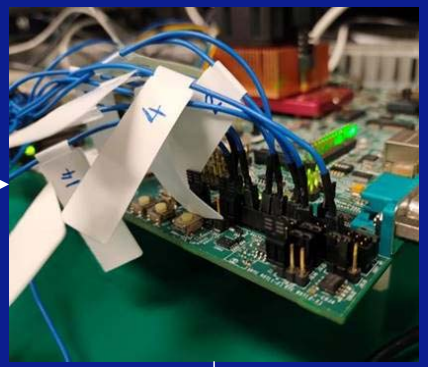

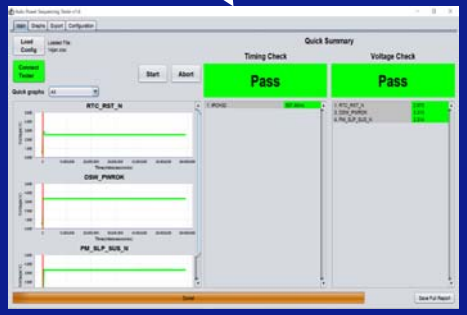

Test Results

Simple, Fast & Accurate

System Under Test

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Summary & Impact of Power Sequencing Tester

Components	Improvements
Hardware Cost	78.57%
Test Time	99.33%
Headcount	100.00%
Characterization Method	100.00%
Result Accuracy	100.00%

Improvement Summary

- **Quality Impact:** Eliminate human dependencies and improve test quality and time
- **Business Impact:** Strengthen Intel's customers engagement with state of art technologies
- **Competitive advantage in SoC validation:** Quality, Accuracy & Speed

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Acknowledgements

- Eric Chan - VP in Intel IoTG (Internet of Thing Group)
- Board of Directors in Intel Malaysia Design Center (MDC)
- Goh, Kean Hean – Engineering Lab Manager
- Ooi, Seong Guan – Product Owner & Staff Technologist

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