RF Simulation Technique for High Speed Test Socket

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smiths interconnect

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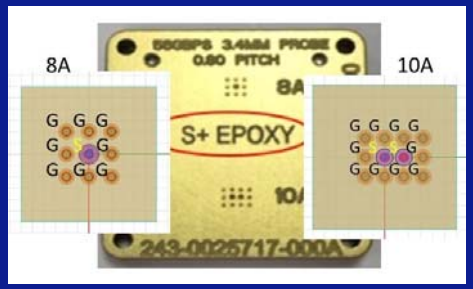
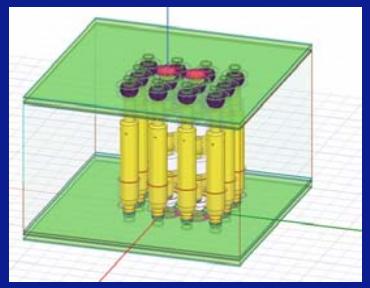
Industry standard for RF Simulation Technique

- Traditional RF Simulation for Test Socket:
  - HFSS or equivalent software is used to simulate socket model.
  - Simple RF test socket with 9 to 12 probes, 8A for Single Ended and 10A for Differential Pair, where A stand for the number of GND probes around signal probe.
  - Simulation model should characterize spring probe design, probe cavity, socket material in a specific pitch, and provide Signal Integrity report based on customer's RF specification.
  - VNA "Vector Network Analyzer" is commonly used with test fixture for actual measurement.





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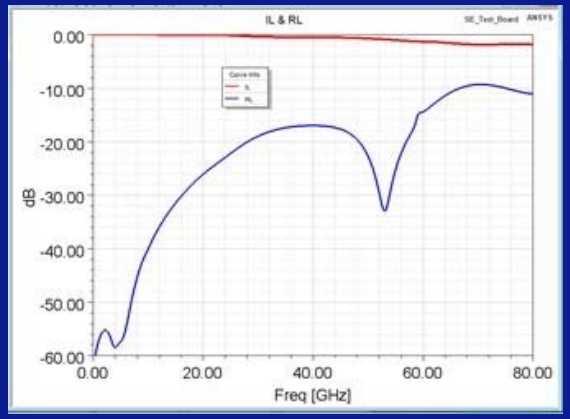
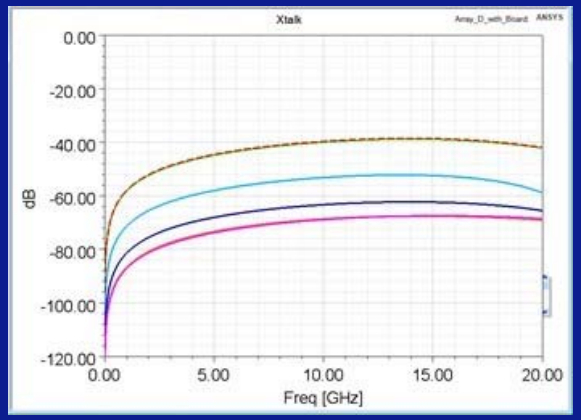
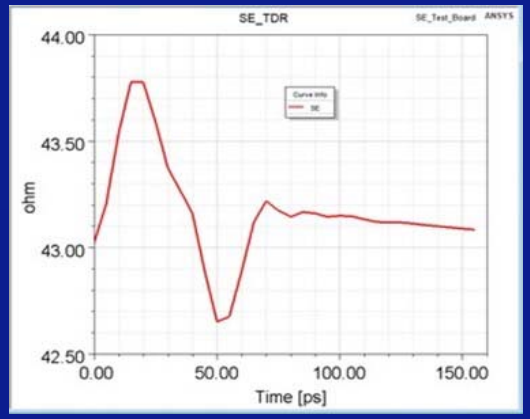
Industry standard for RF Simulation Technique

- Traditional RF Report for Test Socket:
  - IL Insertion Loss
  - RL Return Loss
  - Xtalk
  - TDR Terminal or SE Impedance







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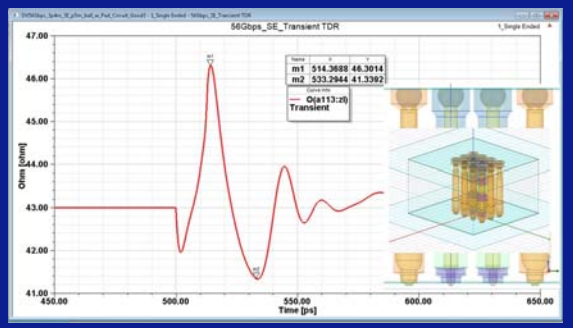
What is the gap and why the need to change?

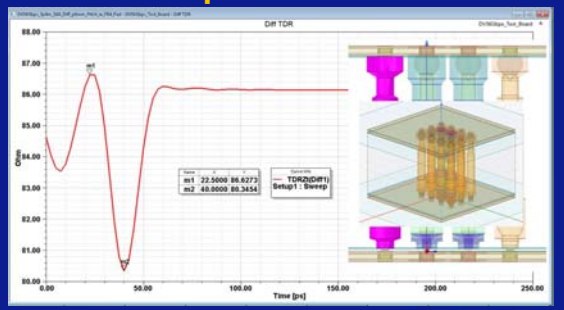
- Current RF simulation gaps:
  - Designing a socket to meet customer target impedance is important, but rather it needs to match customer's test board impedance.
  - Matching impedance needs to be controlled thru out the entire stack-up, to include Device and PCB Contact Interface detail.
  - Simulating 8A-SE or 10A-Diff will show best case scenario for socket performance but will not represent Device RF pin map.

- Why need to change:
  - As data rates and bandwidth continue to increase, more detailed and accurate simulations are needed.
  - TDR plot must be analyzed carefully and adjust design parameter to minimize deviation from target impedance.
  - Simulation result must be validated thru VNA correlation measurement, to ensure future simulations results are accurate.

Without device and bottom PCB



With device pads and bottom PCB



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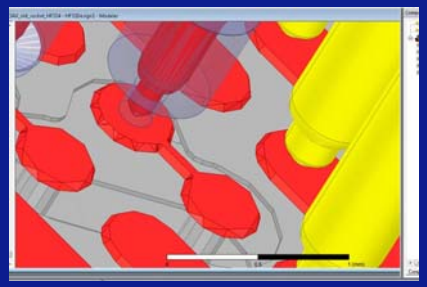
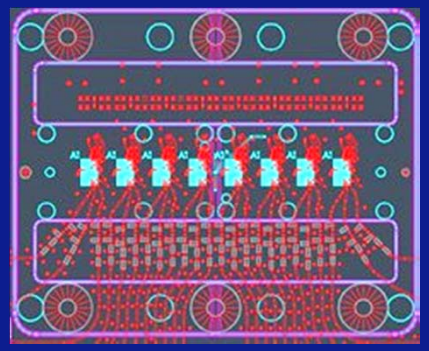
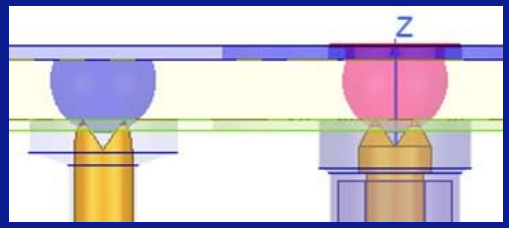
What are the challenges for accurate simulation?

- PCB Top Surface Detail and Fabrication Tolerance
  - PCB top surface detail is not available during socket simulation.
  - PCB fabrication limitation could have wider tolerance than actual design.
  - PCB pad, dog-bone / offset via or microstrip traces would have big impact on SI performance and must be considered and resolved in socket simulation.
  - Device bottom surface detail and spring probe tip penetration to solder ball should be included in socket simulation.







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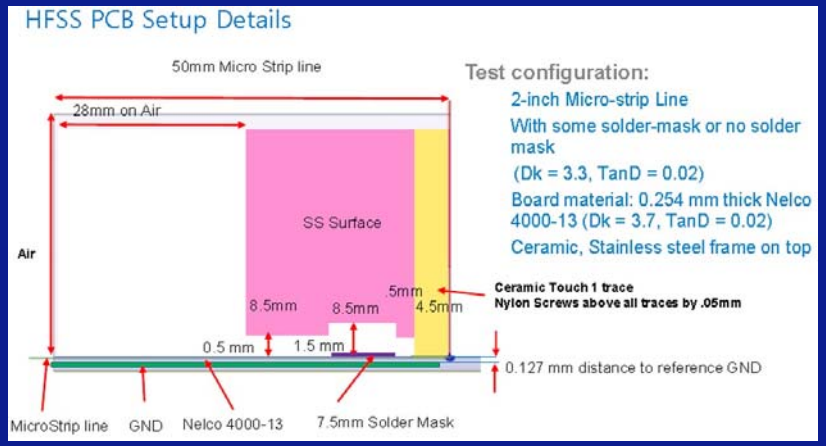
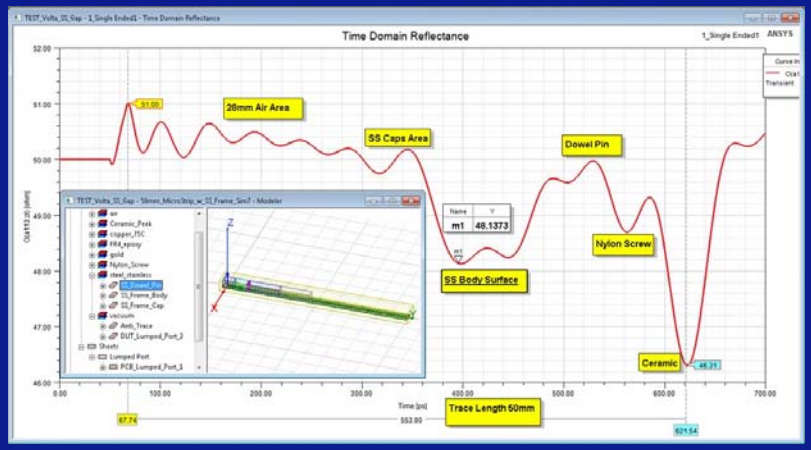
What are the challenges for Accurate Simulation?

- PCB Top Surface Design Detail and Fabrication Limitation
  - Dog-bone / offset via, solder mask, and microstrip traces on PCB top surface need extra attention when mounting standard or impedance-controlled IM socket.
  - Extensive simulation study defines best clearance height for each socket material.





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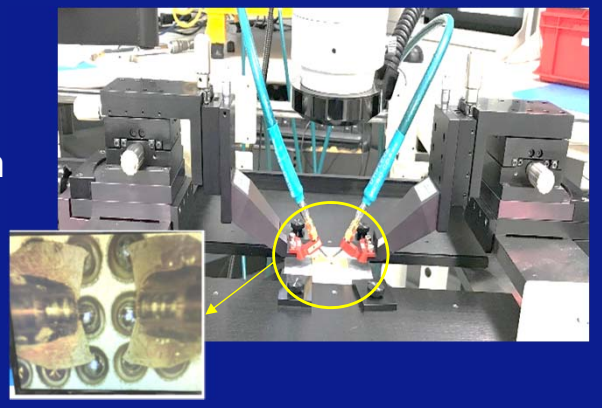
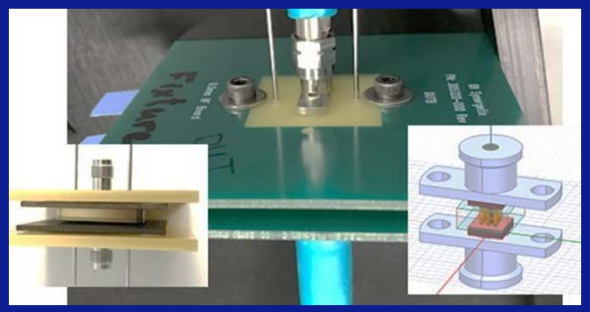
Simulation versus Measurement Correlation

- Measurement Setup
  - Use the standard 8A&10A test socket with device solder ball and bottom test PCB at requested pitch for simulation and measurement.
  - The VNA measures the amount of energy transmitted through the DUT and reflected by the DUT at different frequencies.
  - VNA provides these results in scattering-parameter (S-parameter) of the entire test setup including Fixture.
  - The test socket is then de-embedded to provide basic performance data, such as Insertion Loss (IL), Return Loss (RL), Loop Inductance (L), without the effects of test fixtures and/or PCBs.





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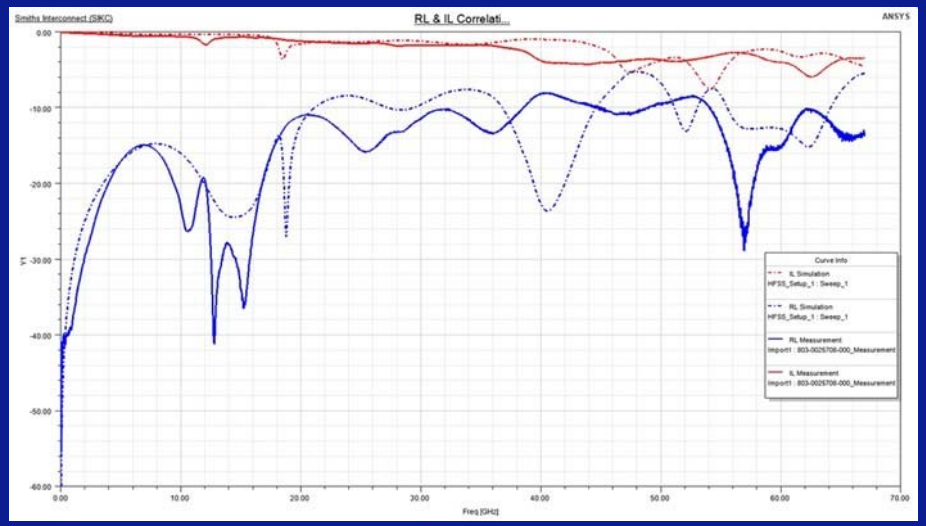
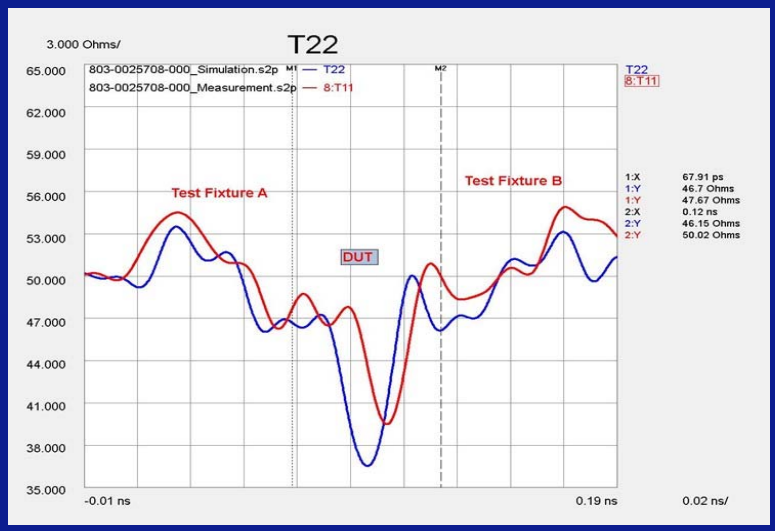
Simulation versus Measurement Correlation

- Measurement Correlation
  - Review result and adjust simulation parameter setup to match actual measurement.





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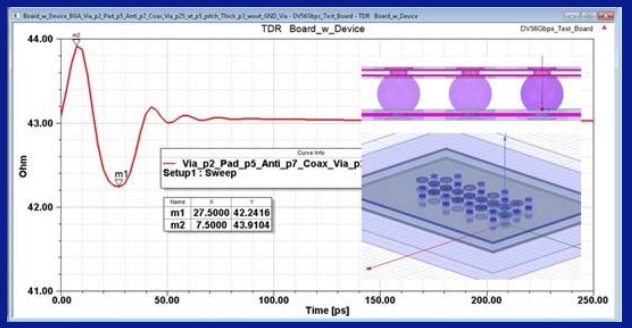
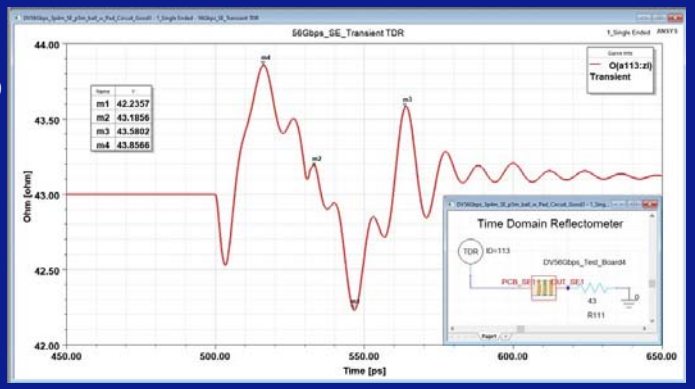
New RF Simulation Technique

- Enhanced Simulation Technique Outline
  - Use customer actual RF pin map.
  - Add device pad/ball bottom interface surface and customer PCB top interface surface to meet customer target impedance.
  - Add probe & cavity and all other components models.
  - Run the simulation up to requested bandwidth.
  - Plot Terminal TDR and optimize model parameter to achieve best performance and minimum deviation from target impedance.
  - Update socket design based on simulation model.





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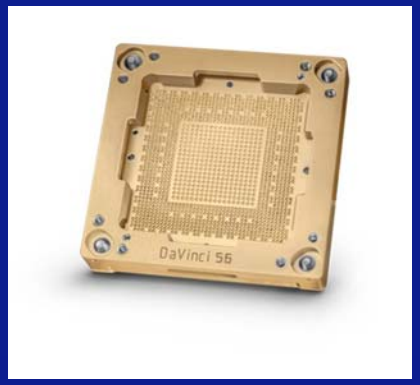
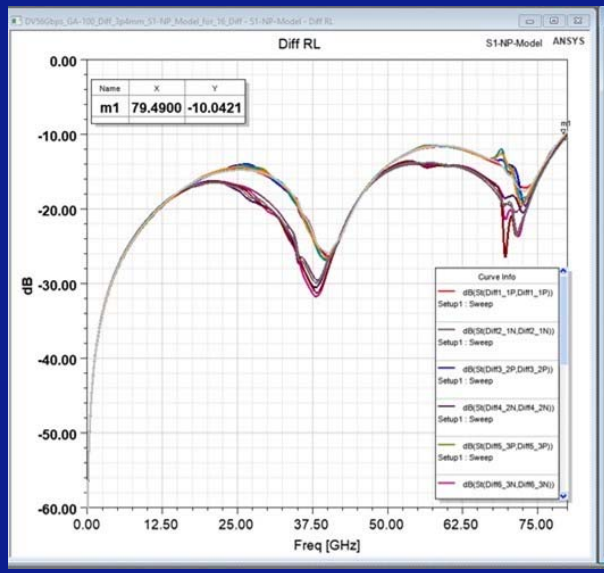
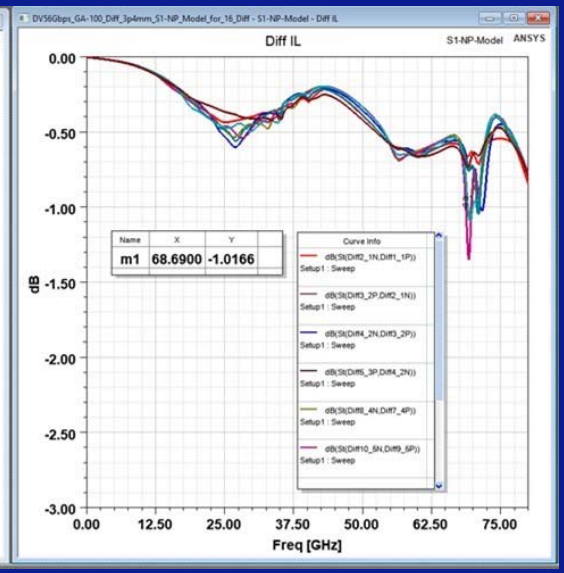
DaVinci 56 Gbps Sample Report

- DaVinci 56G (Impedance Controlled IM Socket) RL/IL







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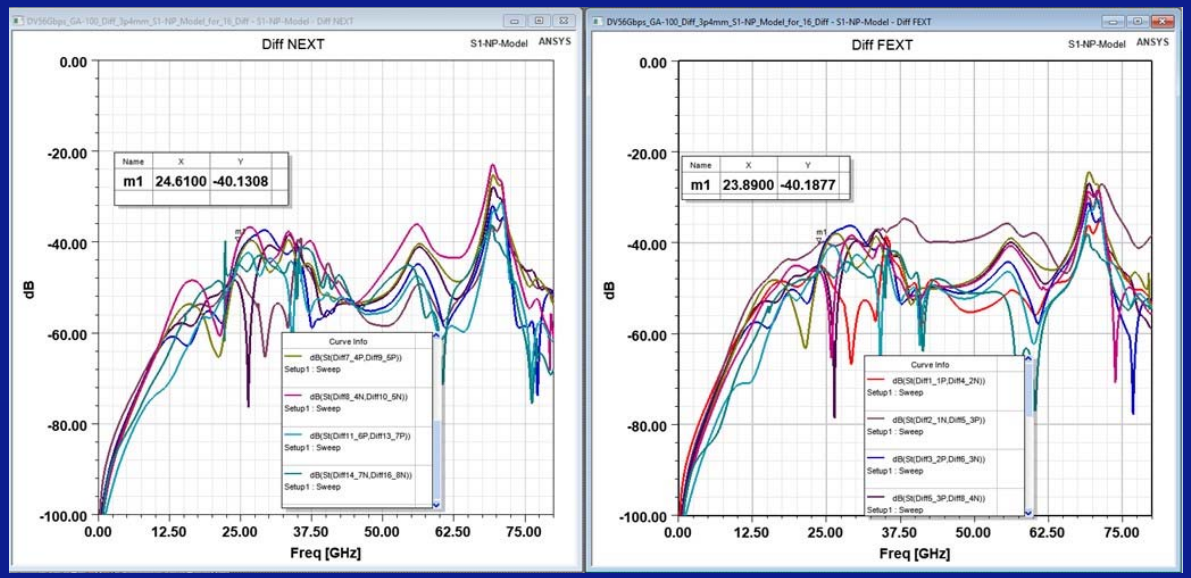
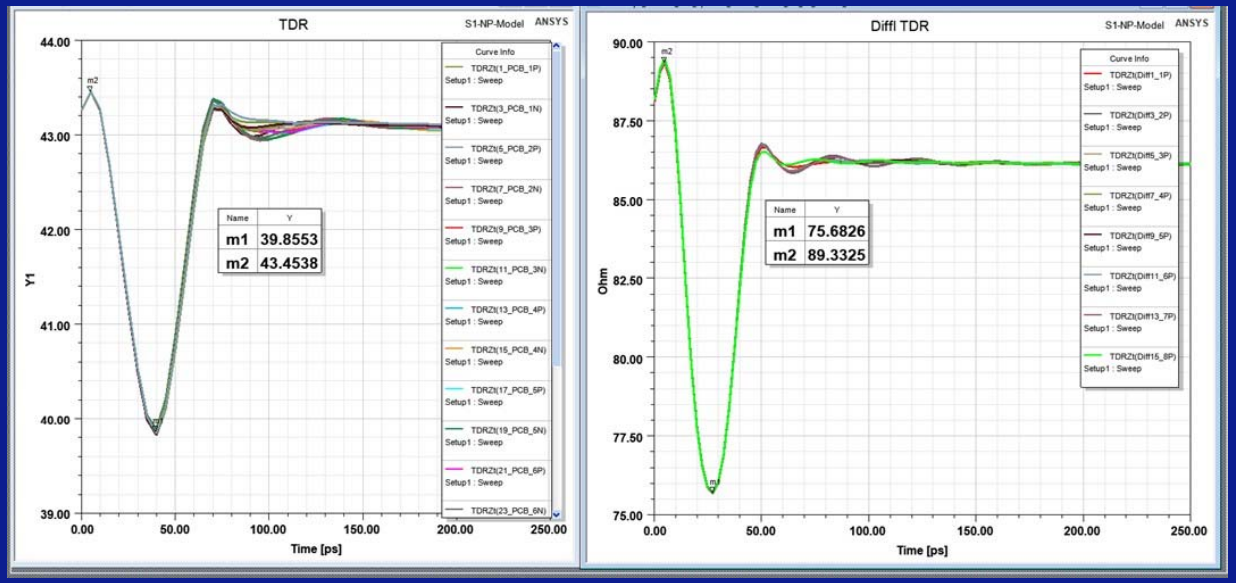
DaVinci 56 Gbps Example Report

- DaVinci 56G (Impedance Controlled IM Socket) Cross Talk



DaVinci 56Gbps Sample Report

- DaVinci 56G (Impedance Controlled IM Socket) TDR



Summary

- SI simulations become very critical in developing new high-speed test sockets.
- Extensive simulation can reduce development time and, more importantly, optimized simulation methodology, by including package and test board structures, can generate more accurate and reliable simulation results.

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