Meeting the Reliability Semiconductor needs of the future

in the Testability, Functional Safety and Security

Luca Moriconi
ELES Semiconductor Equipment

Filippo Giacinti
ELES Semiconductor Equipment

Luca Bensi
ELES Semiconductor Equipment

TestConX中国 China

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ELES

Outline

- Introduction
- What is RETE?
- Shift Left in Reliability
- Synergy between the Design Methodology and the Stress and Test Platform
- Design for Reliability Test
- Learn from Fail
- The future of R.E.T.E.

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What is R.E.T.E. ?

- R.E.T.E. (Reliability Embedded Test Engineering) is the cornerstone of the approach we developed to address the challenges of modern semiconductors
- It is a comprehensive approach (methodology) addressing multiple areas (test, reliability, safety, security) from the design stage, integrating DFT solutions in such a way to standardize and automate the test development and test equipment environment
- R.E.T.E. has been successfully applied on the field to achieve
  - Cost of test reduction
  - Increased failure detection – trigger analysis
  - Faster time to market

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Reliability Shift Left

- R.E.T.E. addresses the shortcoming of the traditional approach where reliability is considered late in the process and often disconnected from the design
- This approach falls shorts coping with the challenges of the most modern ICs and market, both in terms of time and costs
- A shift left is needed addressing reliability and quality together with design and test early in the process

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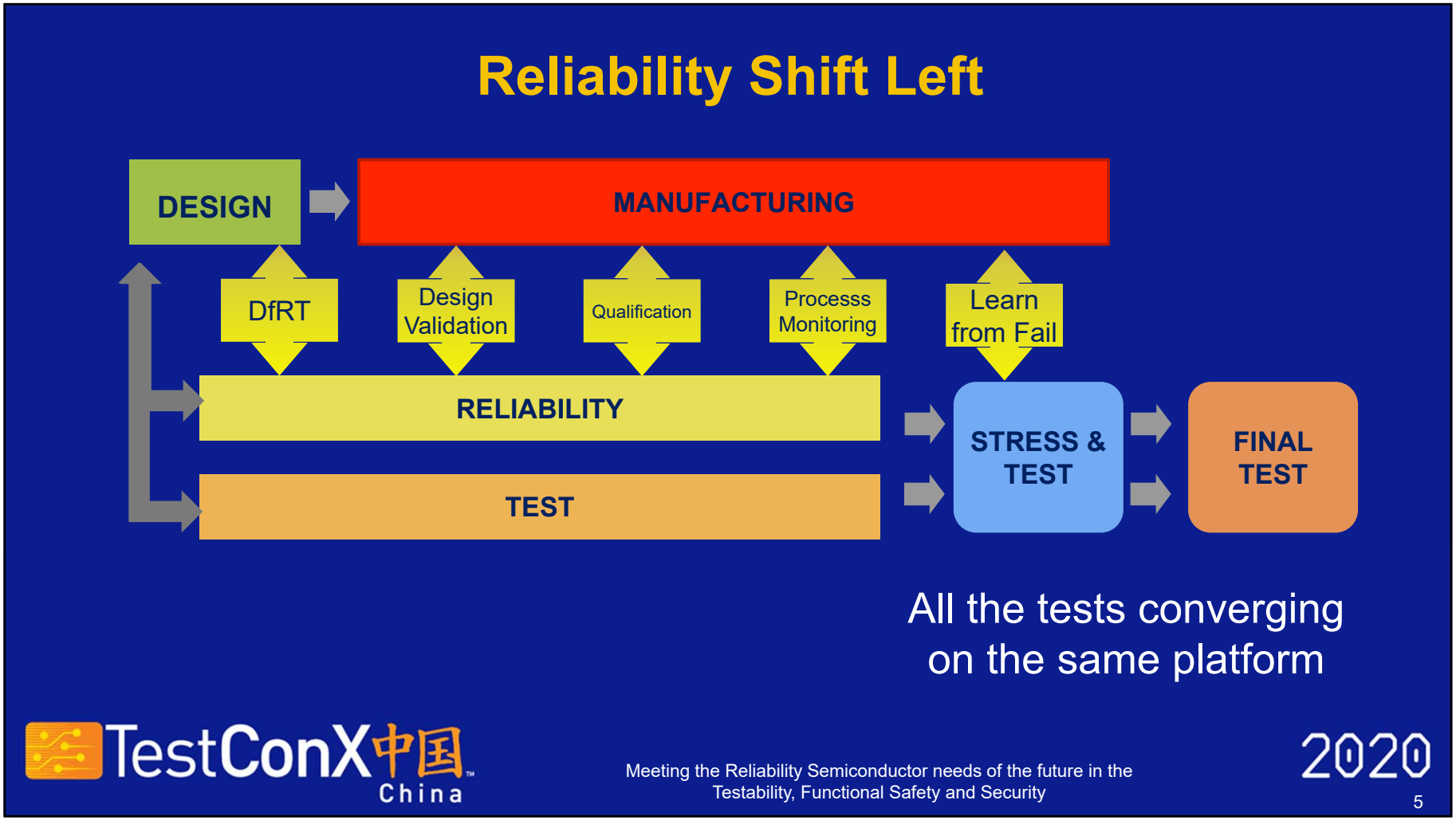
Reliability Shift Left
DESIGN
MANUFACTURING
DfRT
Design Validation
Qualification
Processs Monitoring
Learn from Fail
RELIABILITY
TEST
STRESS & TEST
FINAL TEST
All the tests converging on the same platform
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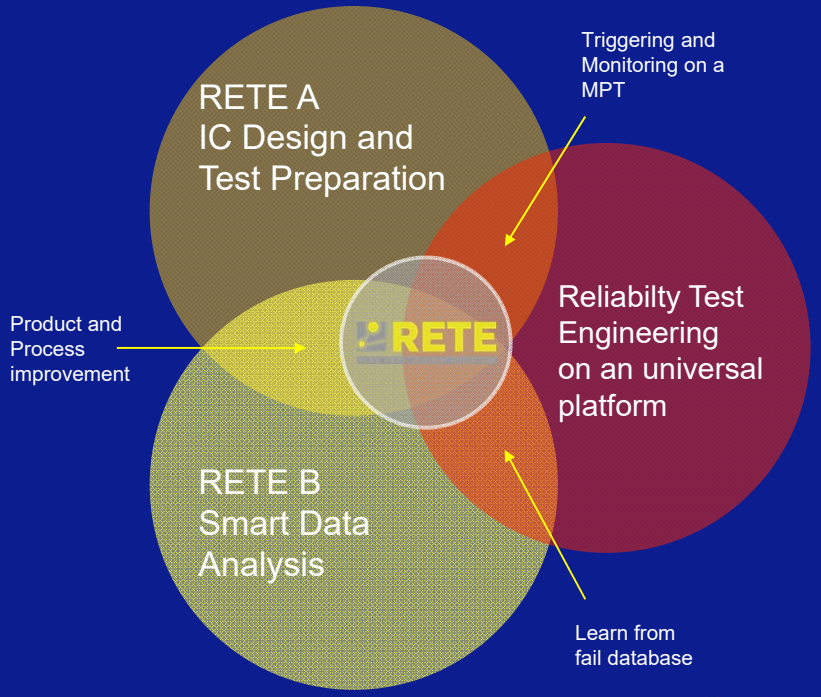
Synergy between design methodology and massive parallel test platform

- At the core of R.E.T.E. there is the coordinate synergy between:
  - the design methodology addressing test and reliability challenges early in the design
  - the use of a universal test platform.



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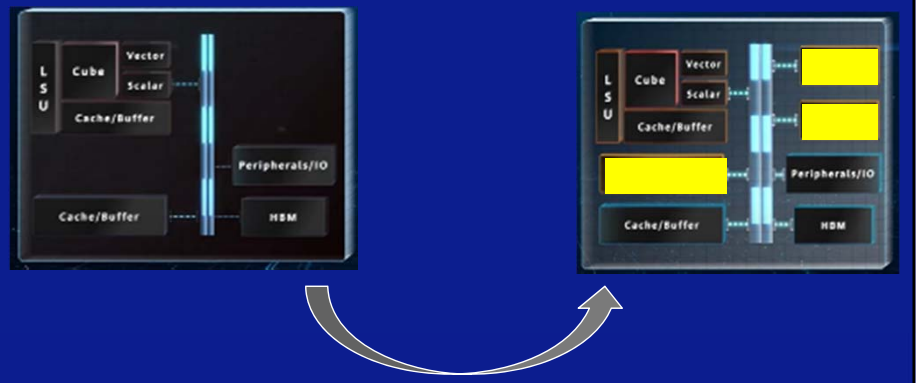
Design for Reliability Test

- **Design Analysis**
  - Determining the required features with respect to the type of device and required reliability targets
- **Finalization of the DfRT Plan**
  - Creates the guidelines for the insertion of the required functions
- **Introduction of the necessary IPs** according to mission profile and family of devices
  - Enhanced fault triggering
  - Enhanced fault detection and testability



RETE

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Design for Reliability Test

R.E.T.E. IPs

- Temperature and current sensors
- Analog/Digital Converters
- Analog/Digital BIST
- Memory BIST
- Configuration and communication features
- BOST Technology if there is no possibility to embed further functions
- Soft BIST
- Monitoring features available in the ART platform libraries

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Recommended Embedded Functionalities for each type of test trial

		Qualification Trial			Manufacturing trial
		Life Trial	Characterization Trial	Static Trial	
Mode selections	Test Mode	++	++	++	++
	Low Power Mode	o	o	++	o
Comm. Interfaces	SPI	++	++	++	++
	I2C				
	JTAG				
Traceability	Unique DIE ID	++	++	++	++
	Wafer coordinates	+	+	+	+
Diagnostic	Diagnostic Register	++	++	o	++
	Status Register	++	++	o	++
Sensors	Current	+	+	o	+
	Voltage	+	+	o	+
	Thermal	++	++	o	++
MUX	Internal analog nodes selection	+	+	o	+
	External analog nodes selection	+	+	o	+
A2D	Analog nodes measurement	+	+	o	+
DFT functions	Logic BIST	++	++	o	++
	Analog BIST	++	++	o	++
	Memory BIST	++	++	o	++
	Unique Scan Chains	++	++	o	++

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Design for Reliability Test

If the IC Circuit was an entire car…

WITHOUT RETE

STD APPROACH

The Car has alarm…!

From where comes the failure?
How to fix?
How to improve?

WITH RETE

The Car has alarm…!

Many information are available, we can focus the design and manufacturing process on the weak parts!

From which one you are getting more information?!

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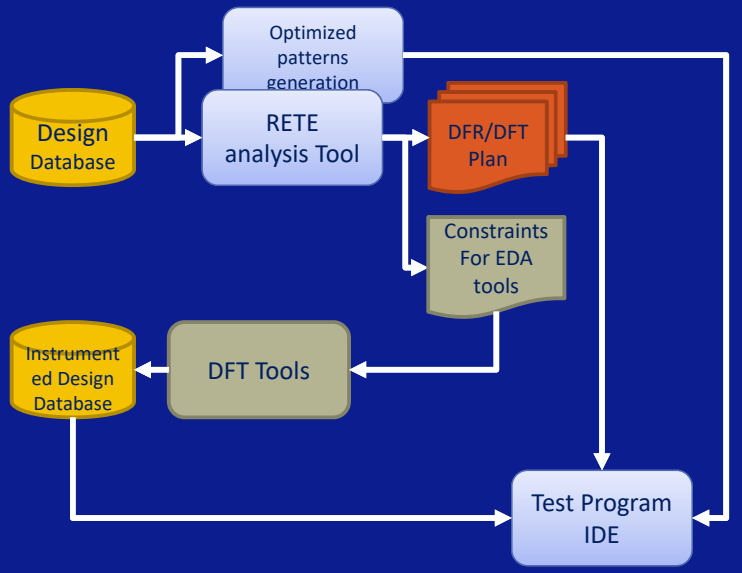
DfRT Automation Tools

- The R.E.T.E. Analyzer carries out the necessary DfRT steps:
  - Review of the original design
  - Compliance with respect to the DfRT requirements
  - Identifies the missing features
  - Creates the DfRT plans with the proposed improvements to the design
- Integration with EDA Tools to automate the insertion of DfRT Features
- Automatic generation of triggering vectors optimized for the specific technology
- Leveraging of "design for" features to address multiple areas at the same cost (testing, reliability, manufacturability, safety, security)



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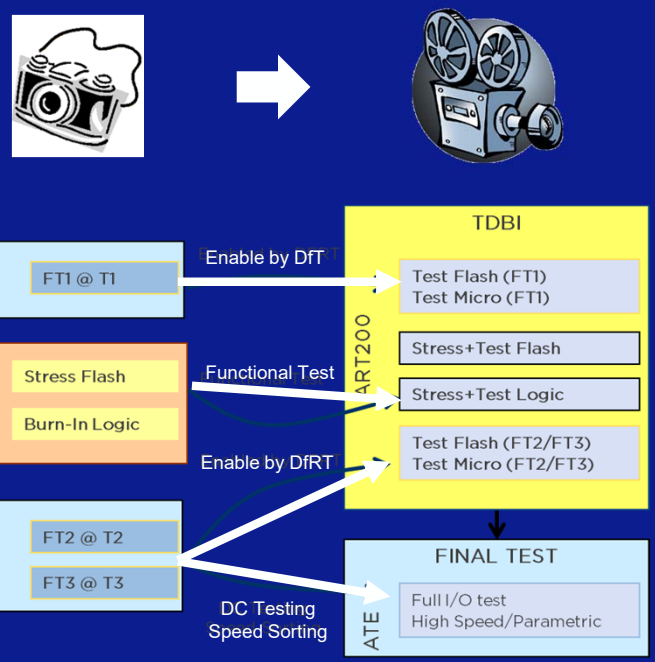
Universal Platform

- Together with the design methodology, the availability of a universal test platform is the other cornerstone of the R.E.T.E. approach
- From Burn-in to Total Test
- Stress and Real Time Monitor in the same step
- DFT Test performed during reliability test flow with failure signature and measurements acquisition.
- All DFT Tests can be moved from std ATE to Universal Platform minimizing the overall CoT
- Real-time continuous drift measurement to trigger extra read-out phase/ failure analysis
- Device working limits characterization (at different time and Temperature) vs. Voltage, Freq. and Temperature



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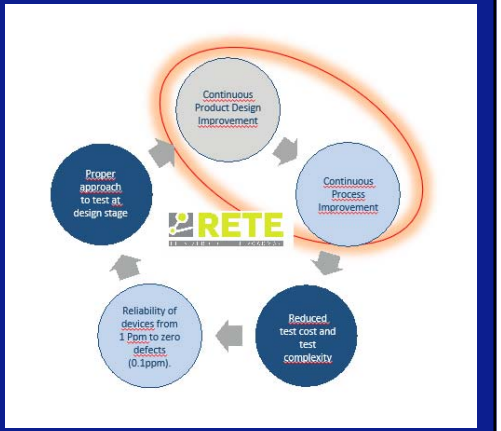
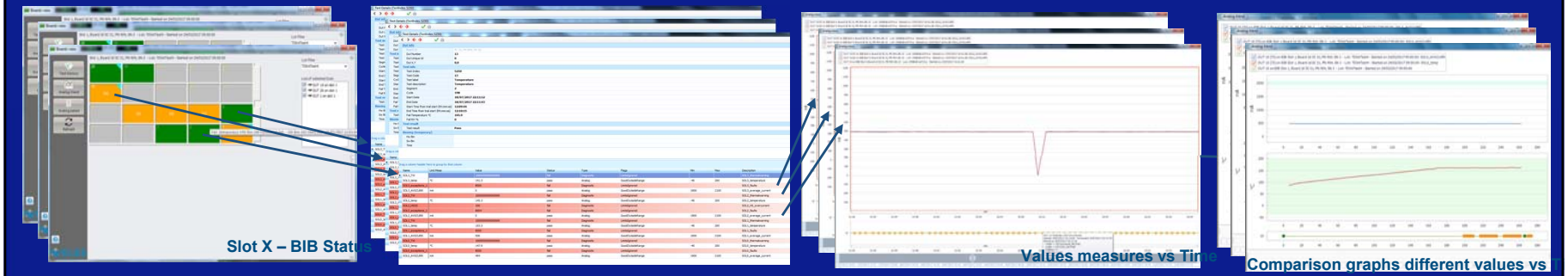
Learn from Fail

- The detailed database of real time failure data collected by the ART platform offers an opportunity to refine the failure analysis
- R.E.T.E. B closes the loop multiplying the value of the solutions adopted with R.E.T.E. A, exploiting the information collected during the test trials to drive a continuous and quantifiable reliability improvement process
- Fundamental step in improving failure rate and decrease early failures





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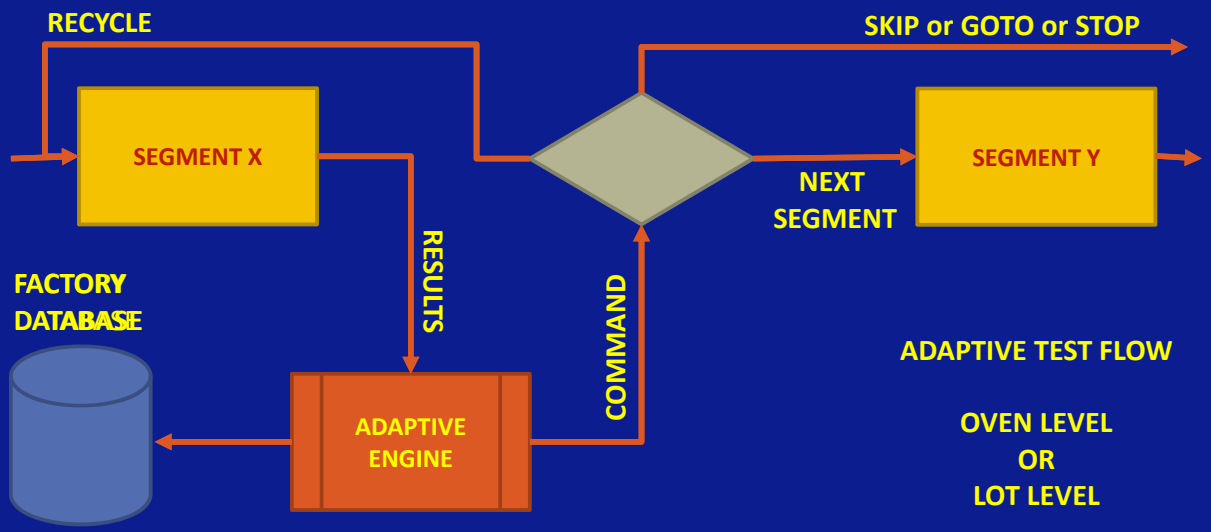
Adaptive Learn-from-Fail (LfF)

The flow of testing can change on the fly based on results or inputs coming from other data sources such as Probe, Final Test, Aging Data Results, Big Data, Non-conforming lots.



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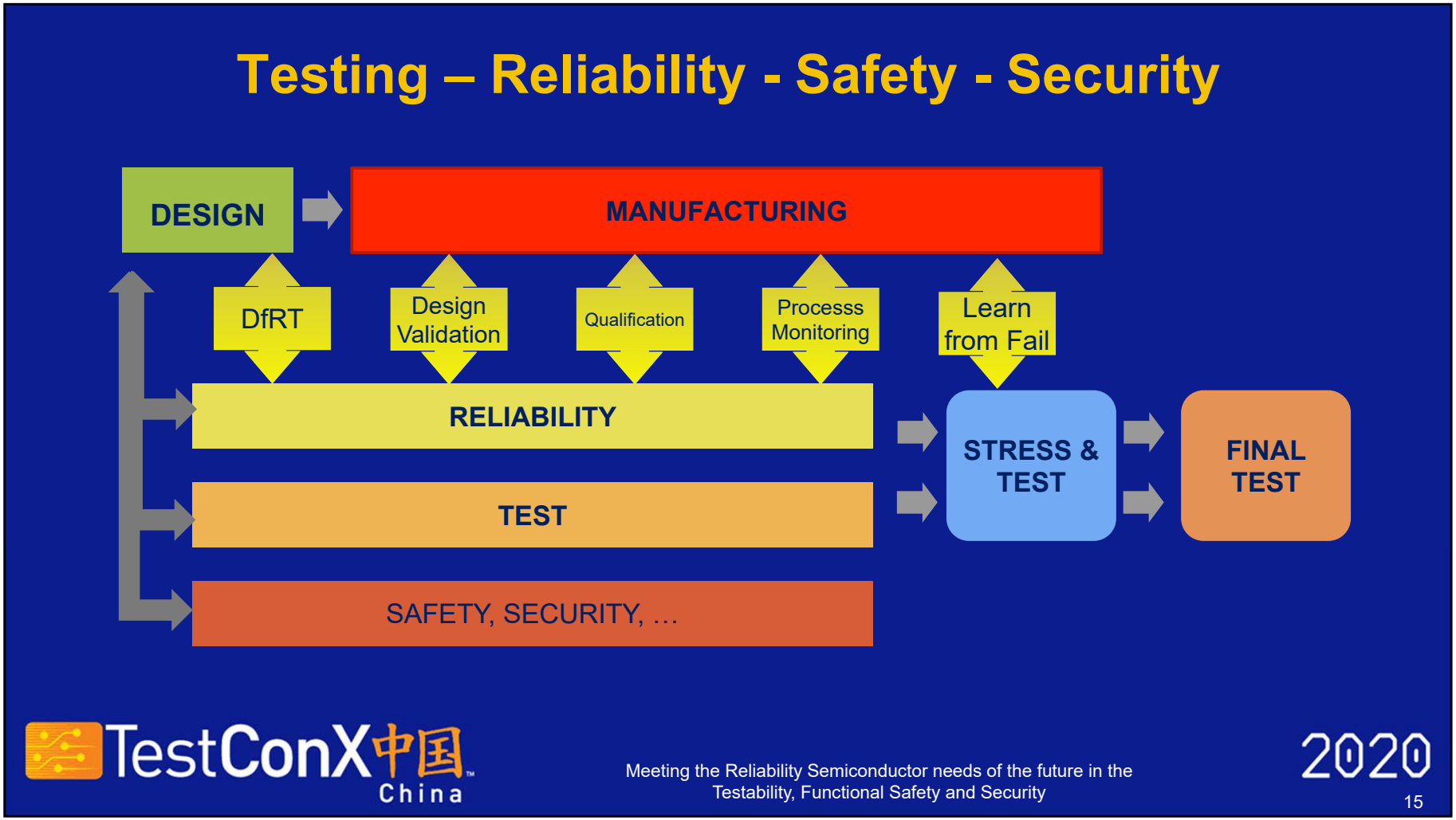
Testing – Reliability - Safety - Security
DESIGN
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DfRT
Design Validation
Qualification
Processs Monitoring
Learn from Fail
RELIABILITY
TEST
SAFETY, SECURITY, …
STRESS & TEST
FINAL TEST
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R.E.T.E. and Functional Safety

- There are several commonalities between reliability and functional safety. They are different angles of the larger concept of dependability, i.e. the quality of the “delivered service” within a certain time period.
- The ISO26262 standard, requires to adhere to a structured testability methodology to address systematic failures, including testability during development, production, service, and operation. This is in line with what is offered by R.E.T.E.
- Moreover, functionalities embedded in the design to address reliability and testing requirements, also play a role as safety mechanism to address random failures.

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R.E.T.E. and CyberSecurity

- R.E.T.E. also addresses the implementation of IPs that can be reused for security as well as for reliability, testing, and safety. For instance, embedded current sensors can play a role in identifying induced soft errors that can be exploited to gain information about of the content of the device and to alter its behavior.

- BIST and other sensors can as well play a role in identifying anomalous behavior that can lead to the identification of a cyberattack both during the test and during the operational life of the device.

- Novel testing techniques can be used to identify the presence of HW trojans. Hardware trojans may induce systematic small alteration of parameters (power, current, etc.) that, with the appropriate sensing circuity may be detected and recorded in a testing environment like the ART platform. The content of the failure database can then be analyzed using statistical techniques to highlight the patterns leading to the identification of the additional structures in the device.

Some Success Stories

- **Cost of Test Reduction for Automotive Products**
  - The combination of R.E.T.E. Approach and ELES Massively Parallel Tester allowed to Stress & Test with the best Reliability & Test Coverage more than 30K ICs in parallel reducing CoT by 70% versus the standard approach
- **Increased Detection on an Automotive SoC**
  - The Qualification Flow allowed Improved Fault Triggering and Detection to capture more defects related to IC analog IP/High Speed interfaces domain
- **Faster Time to Market for High-end Power Processor for Server and Data Center Market**
  - The Test Data collected since the pre-qualification stage allowed an early design improvement, accelerating the path toward Device Maturity and minimizing the TTM in a challenging and demanding market segment

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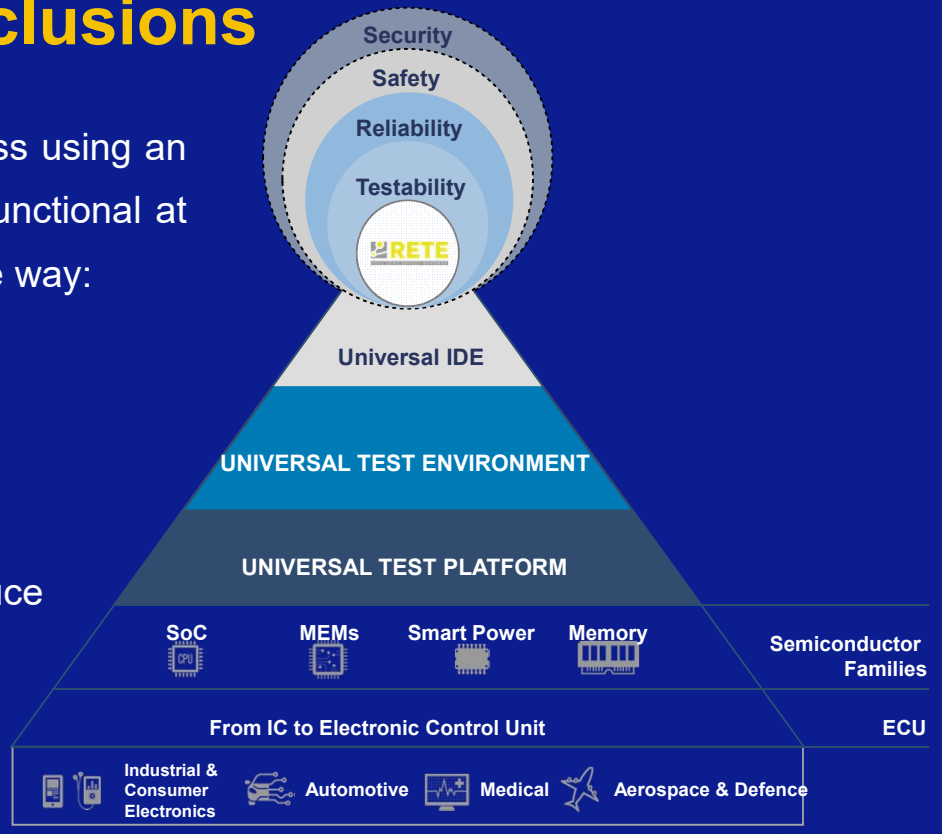
Conclusions

R.E.T.E. allows to optimize the productive process using an approach that is structured, universal and multifunctional at design stage, capable to address in a competitive way:

- the test coverage targets
- the reliability needs
- the functional safety requirements
- the cyber security requirements

aiming to minimize the time to market and to reduce the design and production costs.



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