# Challenges of High Power Processor and ASIC Testing

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# Agenda

- High Power device Test challenge
- Solution:
  - Strong & Flexibility capability to fulfill test demands
  - Static performance: Accuracy
  - Dynamic performance: Cutting-edge speeds & Good Regulations
  - Protections on Test Cell & Fixtures

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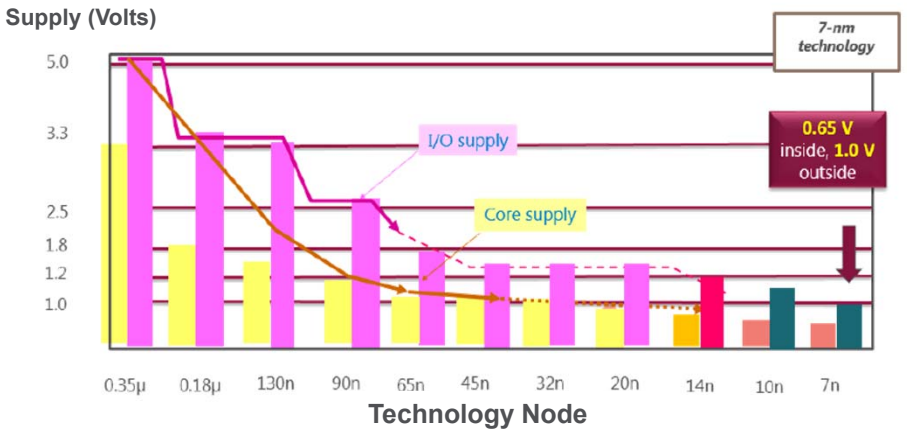
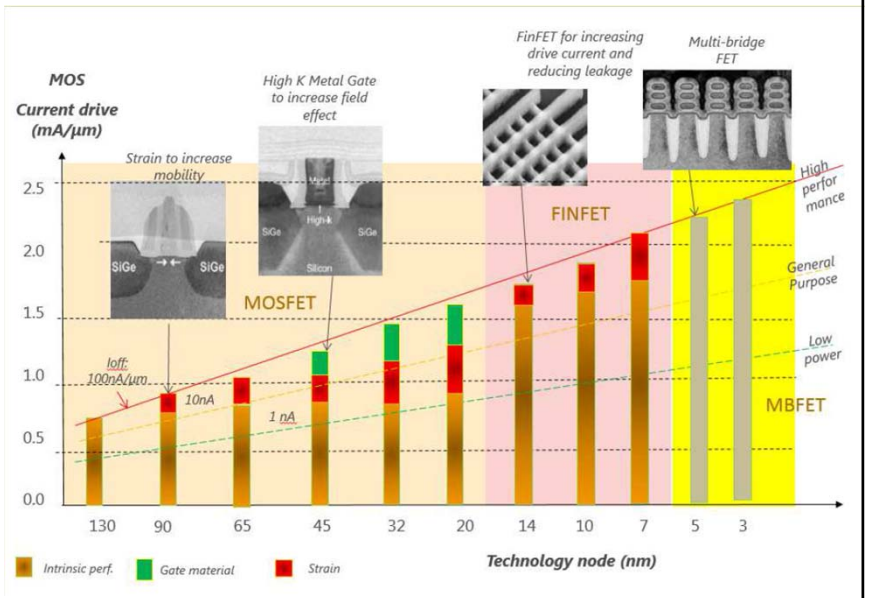
# Challenge: voltage/current trends

- **There is No surprise with node developing**
  - Vdd is going down
  - Idd is going up per/Area




Source: microwind.org

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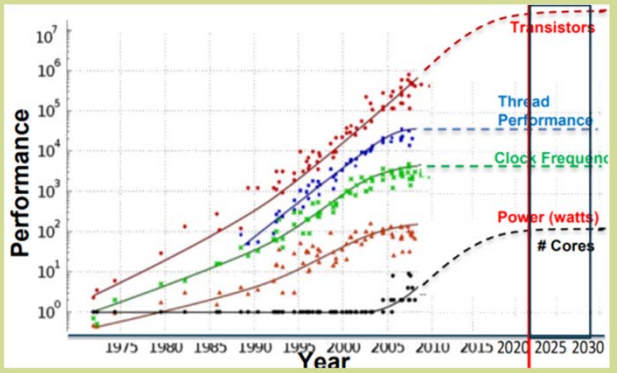
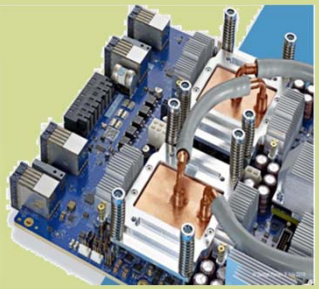
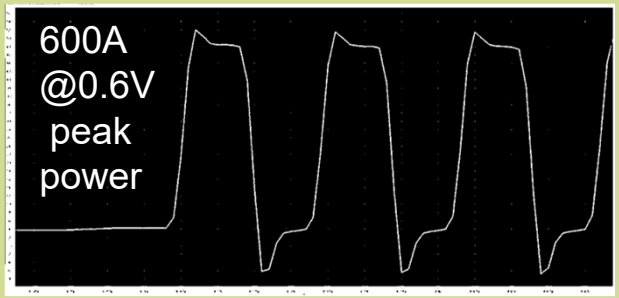
# Challenge: high power push known limitations

- Massive power requirement
  - Server designs thermally limited to 150W-400W in systems
  - Scan test engage high toggle rates, consuming 2-4X power than Function in short term
  - Need perfect regulation to minimize Vdroop
- Integrated Power Regulation
  - Reduce pin count
  - Better transient loop BW
  - Need more accurate Power



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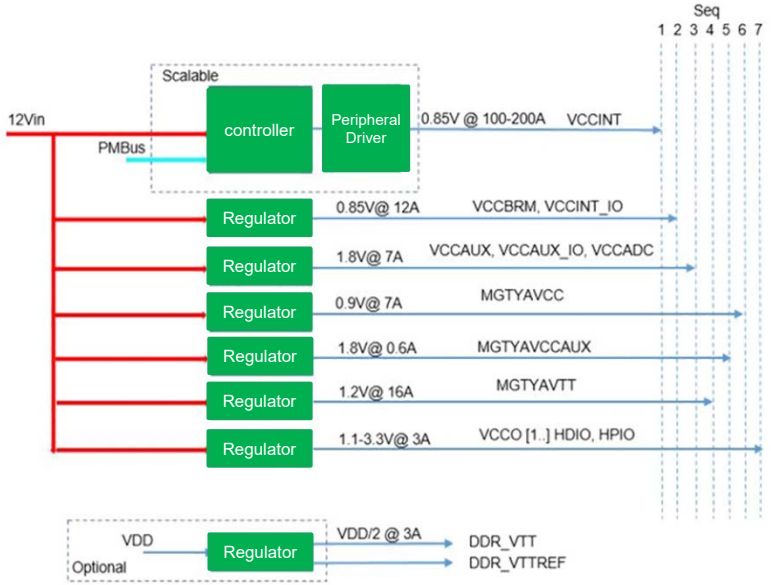
# Challenge: high power push known limitations cont.

- **Advance ASIC own complex power rail**
  - Need multiple phase of voltage supply
  - Power up seq with soft start
  - Also Capability to provide high power at same time
- **Test fixture & interface is getting more complex**
  - Site parallel Large Power approach tester limit
  - Power Envelope need Test cell integration
  - Expensive fixture need robust test solution

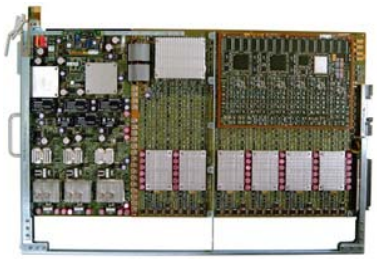



**Processor probe card complexity**

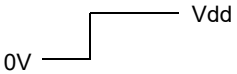
| | 2010 | 2014 | 2019 | 2020-> |
|---|---|---|---|---|
| PADs | 2000 | 3000 | 6000 | >7000 |
| Power rail | 12 | 16 | 24 | 30 |
| Probe pitch(um) | 150 | 120 | 90 | <80 |
| components | 2000 | 4000 | 8000 | >10000 |
| layer | 40 | 50 | 60 | >70 |

# So what should be in an ATE Tester to test it?


Digital Instrument
- Hundreds of pins
- Gb of pattern memory
- Precise timing and frequency
- High speed pin electronics
- Fail capture memory
- Protocol Aware capability



DC Power Supply
- Makes a DC Voltage




**This one is way more important here!**

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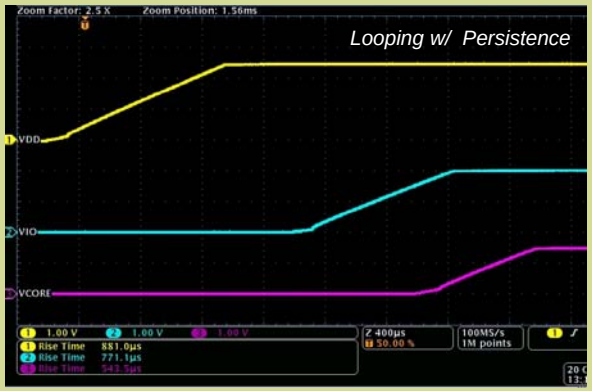
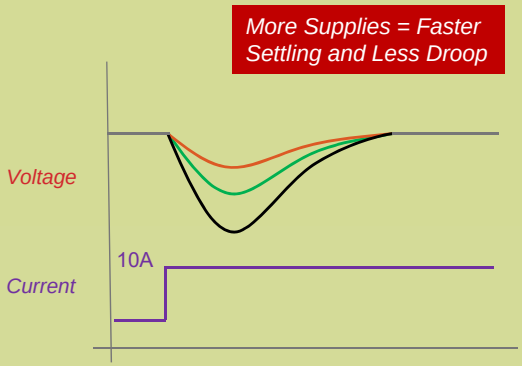
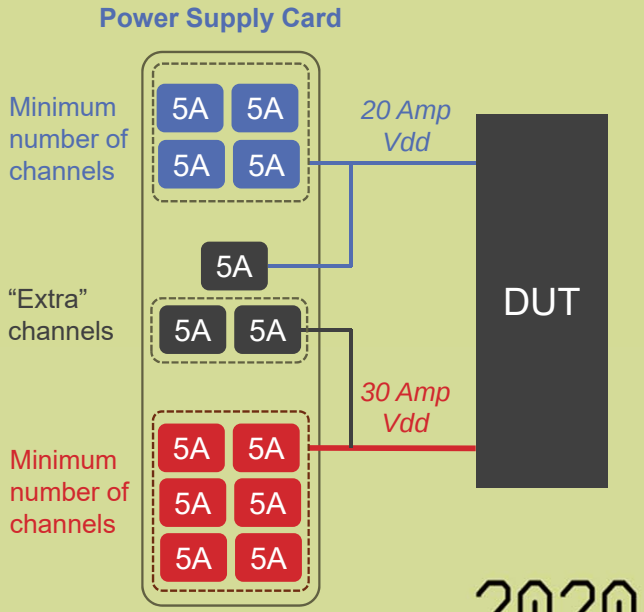
# Solution

# Flexible power supply in test concept phase

- Voltage Source Granularity & unlimited merge make test strategy more flexible
- Also allows “Extra” channels to be used to improved performance
- Customized & repeatable power sequence

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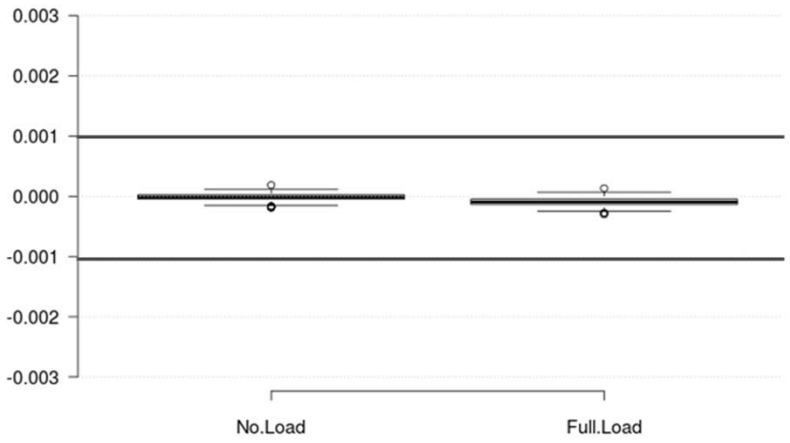
# Excellent force voltage accuracy

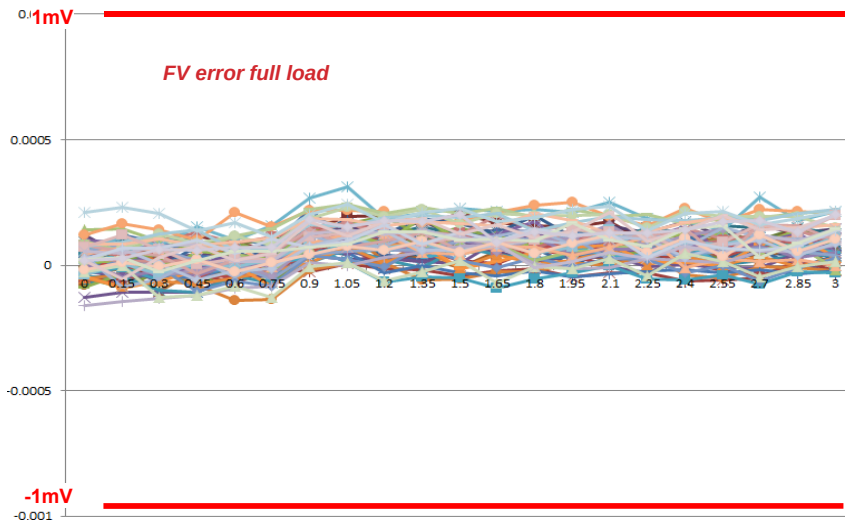
- ✓ Pass more good parts
- ✓ Tighter device specs

**STABLE & ACCURATE Supplies**

Stable under **any load** across the voltage range

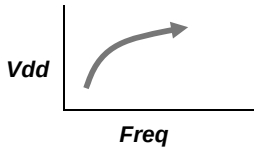
Wide margins to the **guaranteed** instrument spec

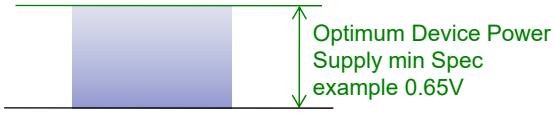


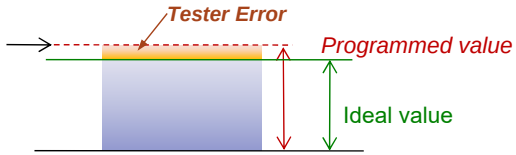
# DC accuracy = better yield + better device specs

*Problem: I spec my device as a function of Vdd and performance… but no tester is perfect*




The supply be programmed to higher than nominal to ensure highest yield…




*…My customer isn't happy because Vdd must be spec'd higher*

*…also, test time is longer because I have to slow down patterns to keep the part from getting too hot.*

…or it must be programmed lower than nominal to get optimum quality


*…I could be throwing away good devices, so yield will be reduced, and the people you work for will be unhappy.*

***Millivolts Matter!***

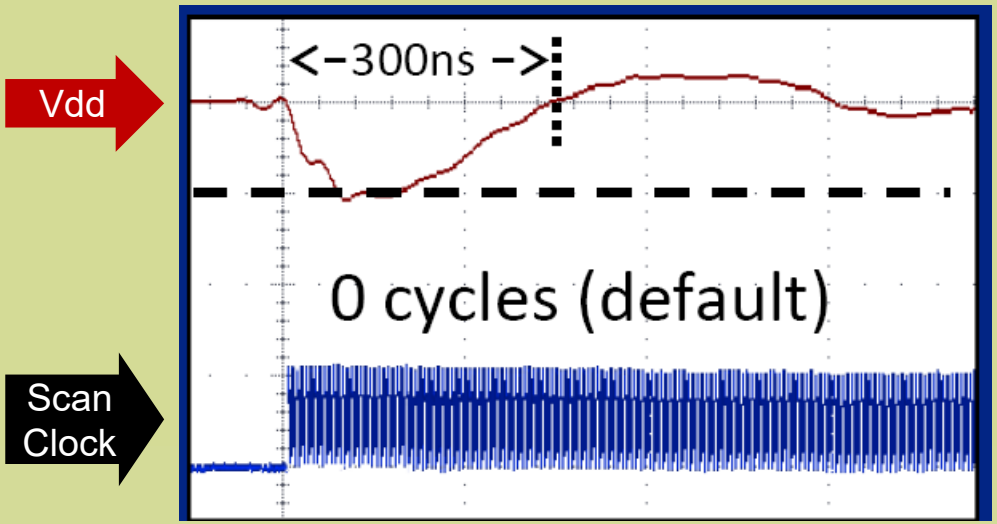
## Power supplies are not static… they tend to move around

When you start a scan pattern,
a lot of transistors all start toggling

The result is an Idd increase of
possibly HUNDREDS of amps

If the power supply droops enough,
the device will fail.

Same problem as static accuracy,
***but more severe and less predictable***

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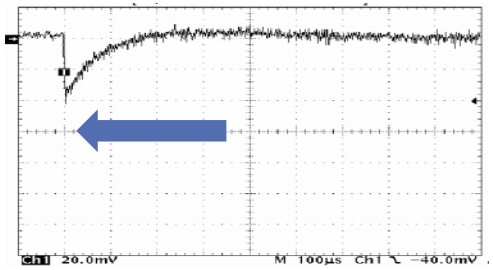
# Shmoo plots tell the story

## Power Supply Stability Example

All device supplies will have some momentary "droop" when scan patterns are started.

*Too large a "droop" will cause good parts to fail, reducing yield*



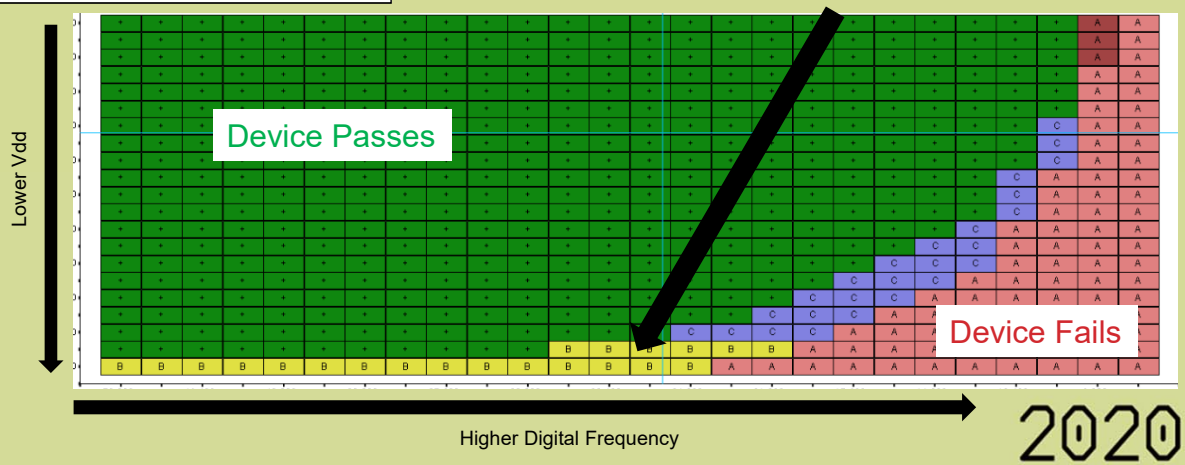

Goal: Lower Test Time by increasing shift rate

Conflict. Can't have fast test time & good quality (?)

Problem: Faster Shift Rate = bigger Power Supply "droop" and poor device quality

Highest Performance at lowest voltage = better device specs

DUT power supply stability is key

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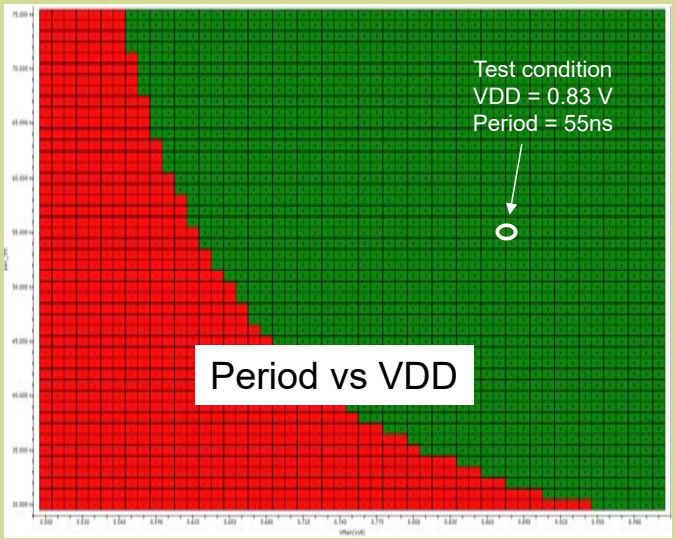
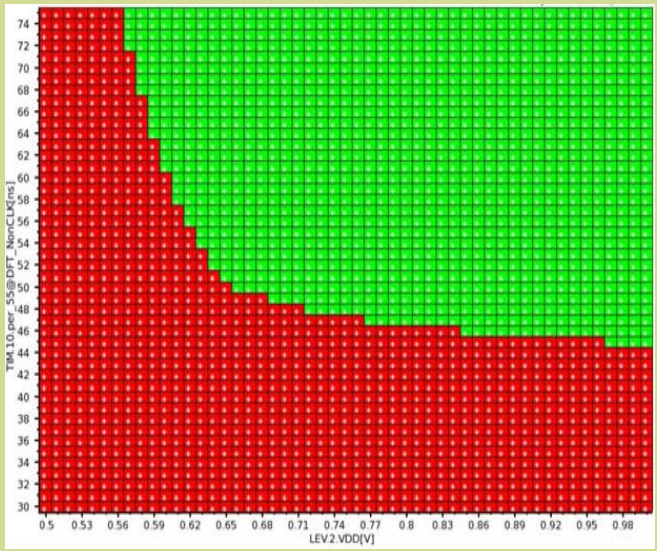
# Shmoo comparison: Which one looks better?

- Recent 7nm ASIC device

Tester #1




Tester #2

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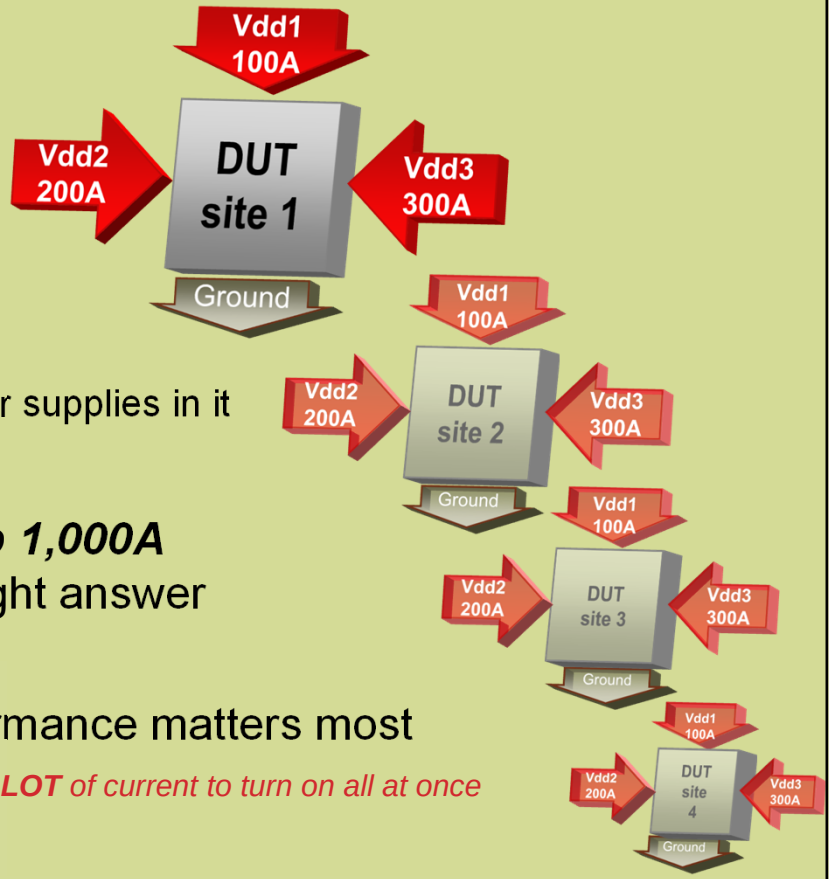
## How much power does your ATE have?

- "Tester can support 1,000A" doesn't mean anything
  - Lots of tester can have a large number of power supplies in it
- "Tester can support ***a current step of 0 to 1,000A system wide*** and still meet spec" is the right answer
- Static accuracy is nice, but dynamic performance matters most

*(100A + 200A + 300A) * 4 sites = a **LOT** of current to turn on all at once*

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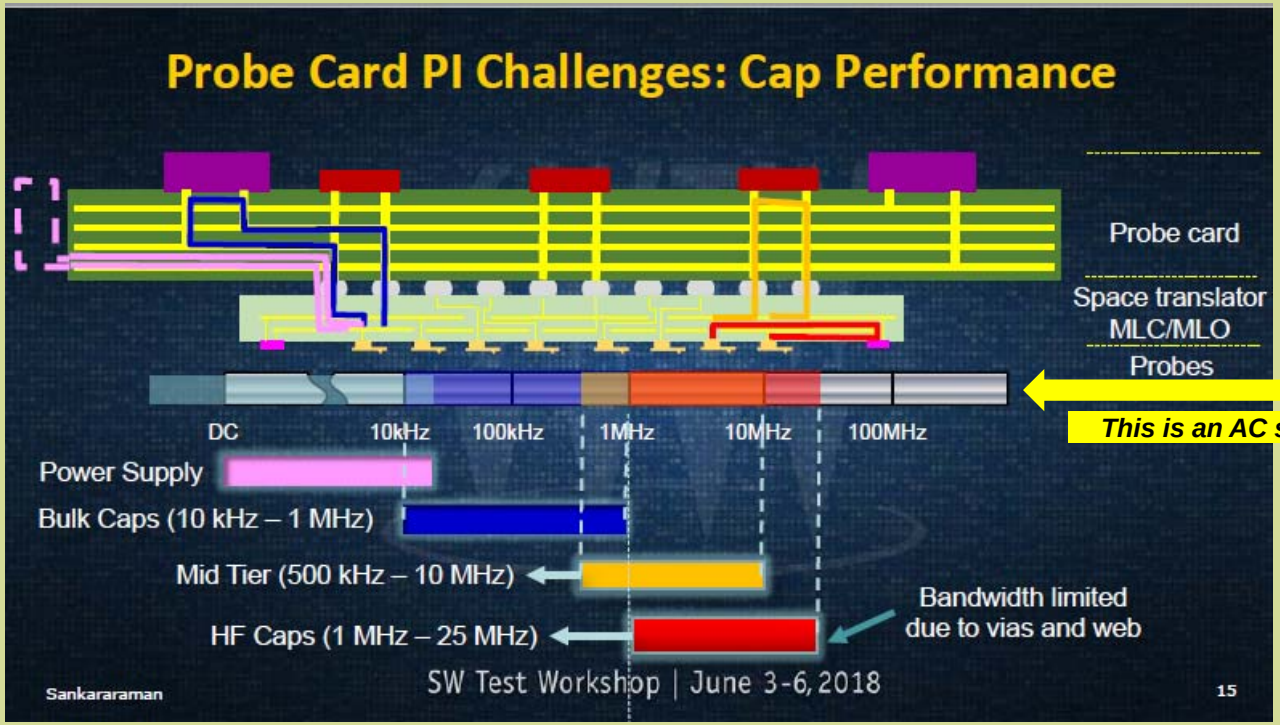
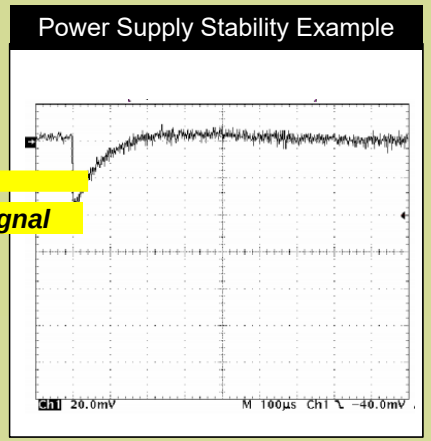
# The AC problem of DC supplies

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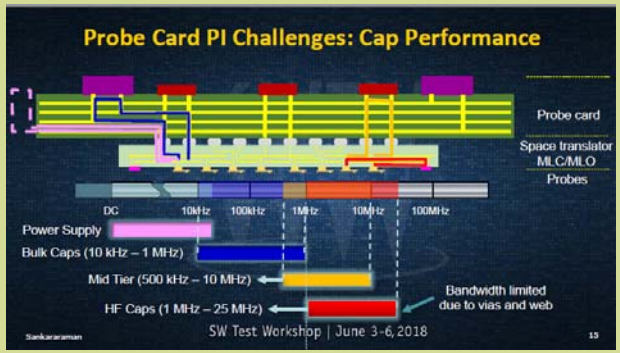
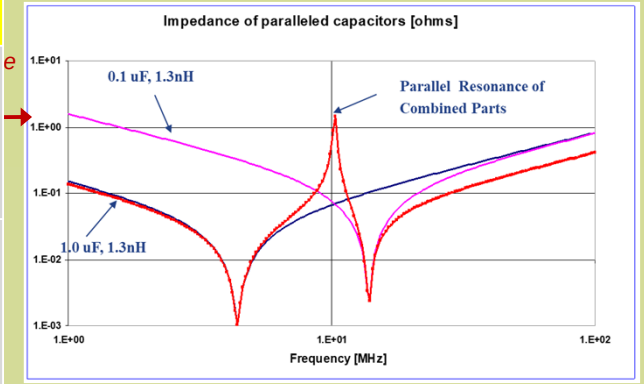
# This is why having a fast, stable DUT supply matters

| Frequency | Traditional Solution | Better Solution |
|---|---|---|
| DC to 100KHz | Typical ATE power supply | ***A really good ATE power supply*** |
| 10KHz to 1MHz | **Bulk capacitance** on DIB | ***A really good ATE power supply*** |
| 500KHz to 10MHz | **More Ceramic caps** on DIB | Ceramic caps to solve ESR/ESL spike |
| 1MHz to 30MHz | **More Caps** in DUT package or probe hardware | Get lowest ESL caps available and use as many as will fit |

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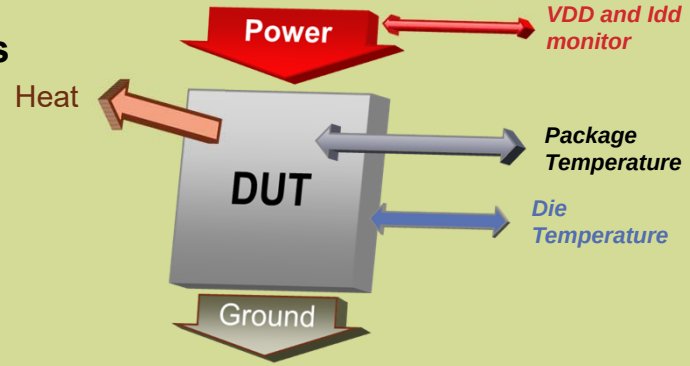
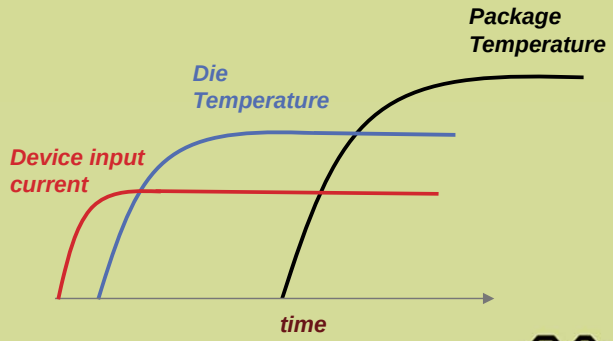
# All that power has to go somewhere…

**How to test the part without having it burst into flames**

- Remove heat from the DUT
- Keep die temperature as stable as possible
- Automatic Temperature Control (ATC) equipment does this one of three ways

1. DUT Power Monitor
   - Pros: Always available *if the tester supports it natively*
   - Cons: Correlation to die temperature is not exact
2. Die Temperature monitor
   - Pros: Tells you exactly what you need to know
   - Cons: No standardized implementation
3. Package Temperature Monitor
   - Pros: Handler can just do it by itself
   - Cons: Long propagation time

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# Alarms mechanism better your shipped quality

***Identify Fake-pass devices show flaws with No addition effort***

**Situation**: Fixture Unexpected High Resistance

**If no real time alarm, Results in:**

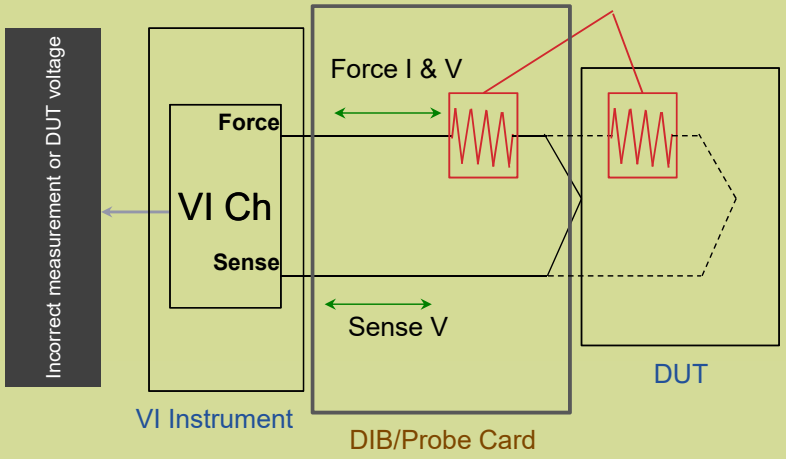
If an issue with device, VI measurement could still pass with critical issue.
If an issue with DIB/Probe Card in production, testing will continue with instrument sourcing the incorrect voltage.

- **INCORRECT VI MEASUREMENTS**
- **DAMAGE TO DUT/SHORTENED LIFE SPAN**

➔ **TEST ESCAPE!**

Realtime hardware based alarms is needed,

to provide true background monitoring of all power pins



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