Lowest cost per Amp for a Modular & High Fidelity broadband DPS

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TestConX中国 China

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- AEM's Approach To address The Technical Challenges at affordable cost
- Summary & Closing

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Abstract

- “The wide spectrum of SOC and SiP devices are driving a large range of DUT power supply requirements. Power supply requirements range from low power less than1 Watt per device with up to 5 different voltages to high end GPU/Processors with switching requirements from 10 Watts to more than 300 Watts within a few microseconds.
- Mu-Test, an AEM company, is addressing these challenges by developing a unique Power supply module that covers low power/high accuracy and high power/high accuracy device needs while maintaining the required signal fidelity at an affordable cost.”

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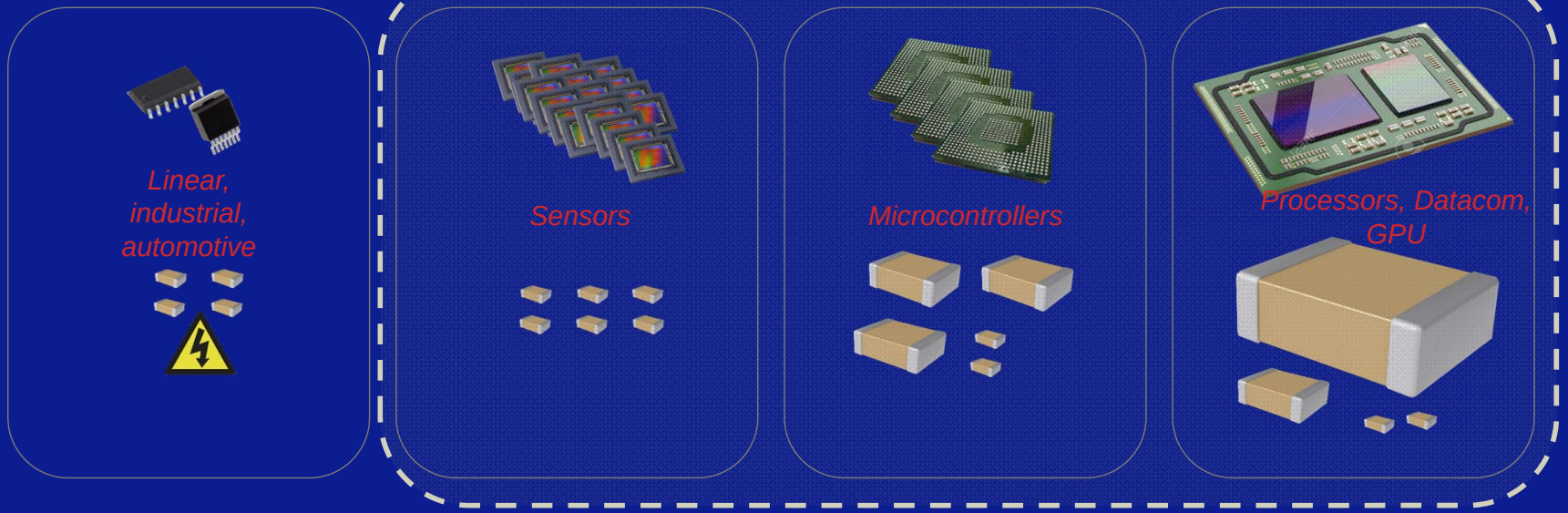
Needs for Unified DUT Power supply solution



The wide spectrum of SOC and SiP devices are driving a large range of DUT power supply requirements. Power supply requirements range from low power less than 1 Watt per device with up to 5 different voltages to high end GPU/Processors with switching requirements from 10 Watts to more than 300 Watts within a few microseconds.

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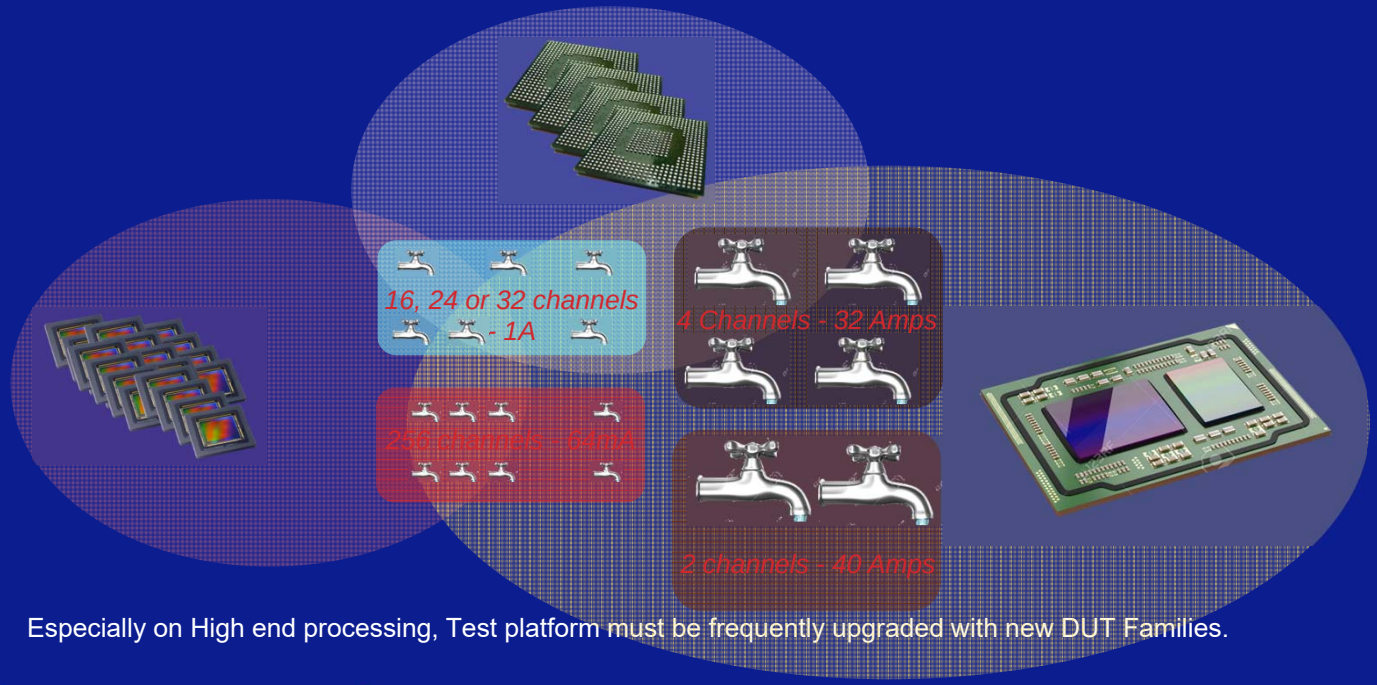
Needs for Unified DUT Power supply solution

Current Market DPS offering



Especially on High end processing, Test platform must be frequently upgraded with new DUT Families.

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Needs for Unified DUT Power supply solution

AEM DPS broadband DPS offering

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Needs for Unified DUT Power supply solution

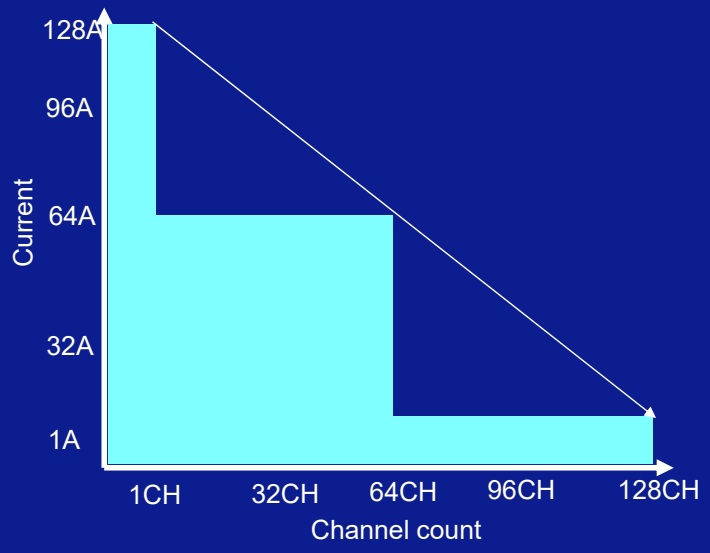
Price usage and customer expectation

Customer expectation

- In mid to low end SOC platforms, DPS cost is embedded in the platform cost structure.
- AC performance requirements for High current normally drive expensive DPS options.

Flexible Usage

- Cost per channel for ganging < 32 Amps
- Cost per A when ganging > 128A
- Cost per instrument same irrespective of power
- Gang up to 3 instruments for 3* flexibility



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Unified DPS specification objectives

Sales and Market expectation

A single instrument covering:

- SOC's,
- sensors,
- High End processing (data, images, computing)

Reduce Known Good Product cost through

- Improved integration
- Unique Amplifier design covering all requirements through flexibility
- Design for high reliability

A single instrument provided with the added requirement of all DUT categories

- 128 DPS channels, 1 A each
- Voltage from -2V to 6.5 V, 9 current ranges: 5uA to 1000mA
- Max total current 128A per instrument
- Inter-instrument ganging capability (objectives: 512 A)
- 4 quadrant operation mode
- 16/18 bits DAC/ADC
- Gang mode: 2 to 128 channels
- Gang max 3 boards, max current 384A
- Programmable Current/Voltage Clamps
- Programmable slew rate
- Dual PSRR test noise injection option
- Histogram mode per channel
- Isolation/Enable per channel

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Technical Challenges to meet specification objectives

Device Layout, modularity analysis

Theoretical Max instrument capability:
270 Cells, 270 Amps

Manufacturing constrains:

- First Pass Yield = F(# of DPS Cell)
- # of max LGA/BGA device change per electronic assembly
- Tradeoff between # of module type and integration/repair simplicity

Cost constrains:

- Unique and large PCB is unaffordable
- Cost = F(# modules, connectors)

Inventory constrains:

- Minimize item value in Stock
- Minimize spare board stock value world-wide

Engineering Constrains:

- Characterization effort = F(# of channel/module)
- NRE cost = F(# module type)
- Reliability = F(θ_{jc})

→ Limiting to 128 Amps/Instrument

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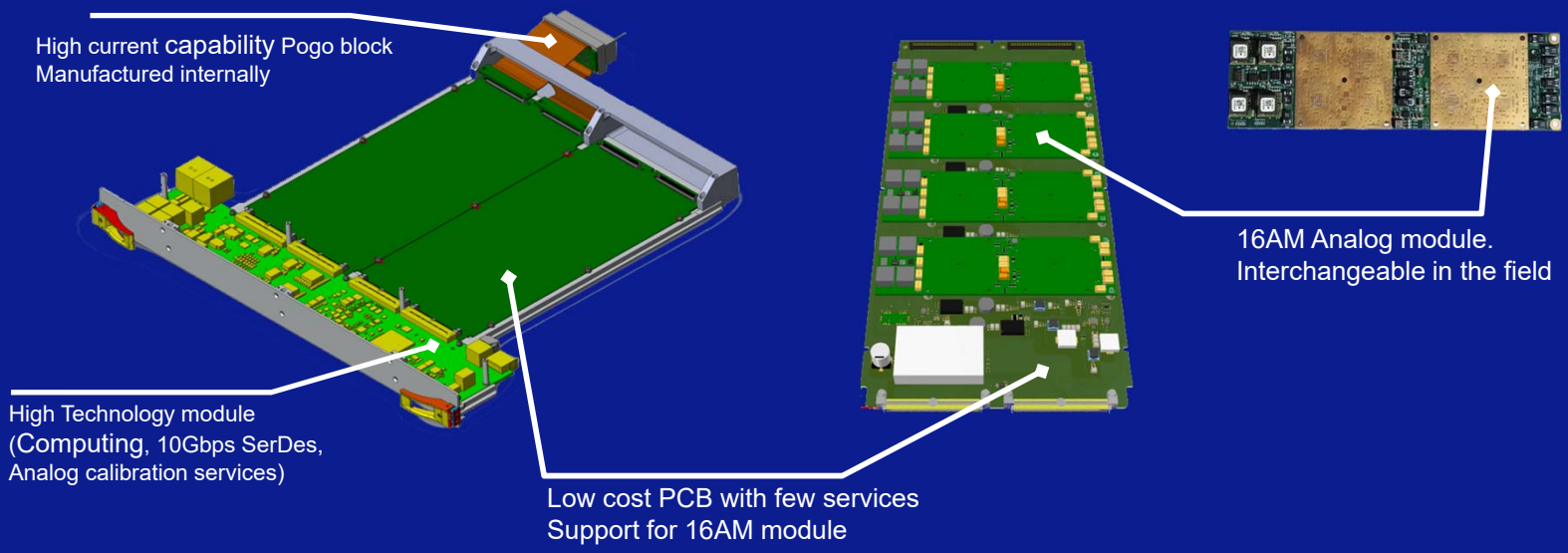
Technical Challenges to meet specification objectives

Device Layout modularity analysis



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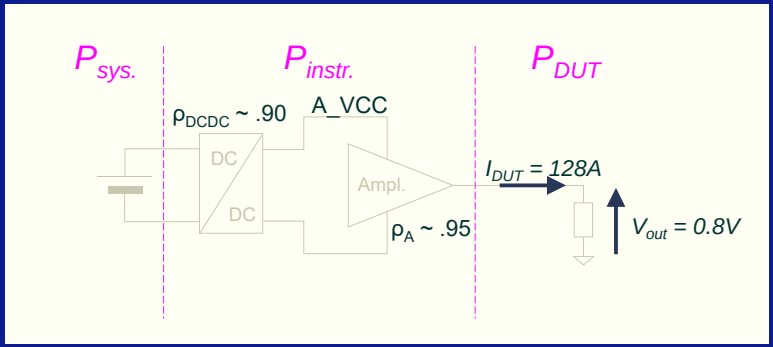
Technical Challenges

Power yield & cooling analysis



Worst case is Low voltage on DUT, eg 0.8V for processor core. With A_VCC = 8V

- P_{DUT} ~ 100W
- $P_{ampl.}$ ~ 970W, eg 7.6W per amplifier
- $P_{sys.}$ ~ 1200W ρ ~ 8.5%

➢ Standard linear implementation makes no longer sense

Mixed PWM / LDO design implementation significantly improves those figures

- P_{DUT} ~ 100W
- $P_{ampl.}$ ~ 300W, eg 2.3W per amplifier
- $P_{sys.}$ ~ 450W ρ ~ 23%

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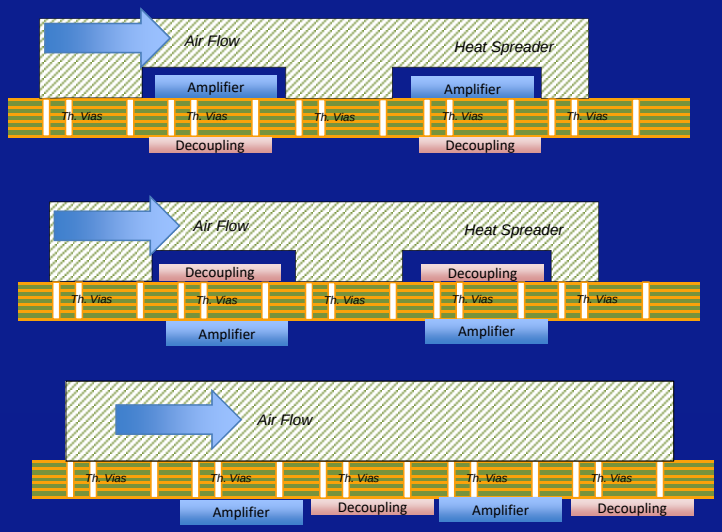
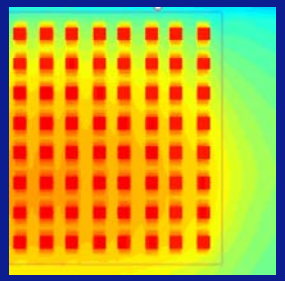
Technical Challenges to meet specification objectives

Power yield & cooling analysis



Many different configurations are simulated in order to predict the junction temperature. The parameters are mainly:

- Number of thermal via's
- Type of thermal pad
- Via fill ?
- Heat spreader design, air speed
- Number of heat conduction layers



Among the few acceptable solution's, the pcb cos and assembly process was the key decision maker

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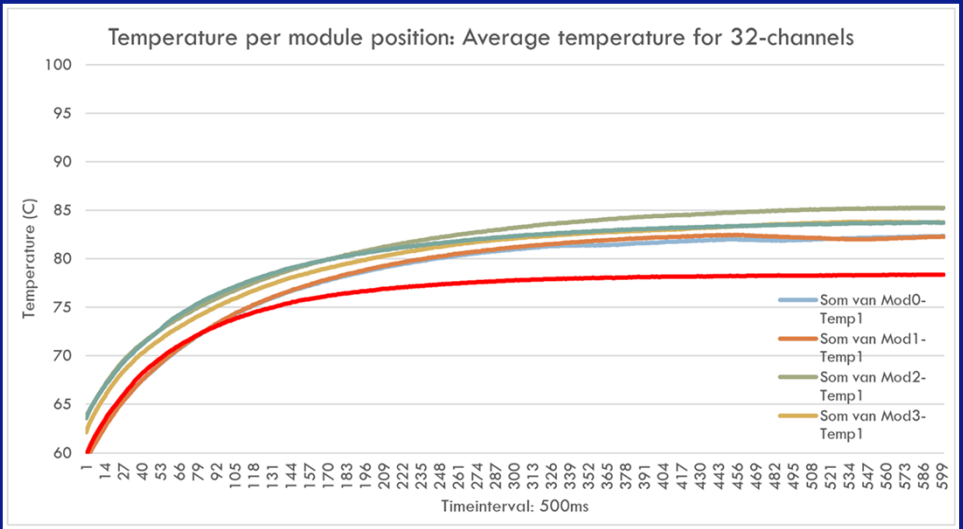
Technical Challenges to meet specification objectives

Power yield & cooling analysis



With 2 * 16AM modules in worst-case scenario configuration, the results on the Hardware are showing better than expected Juntion Temperature

- Target max junction temperature 100ºC
- Simulated: 90ºC
- Verified: 85ºC

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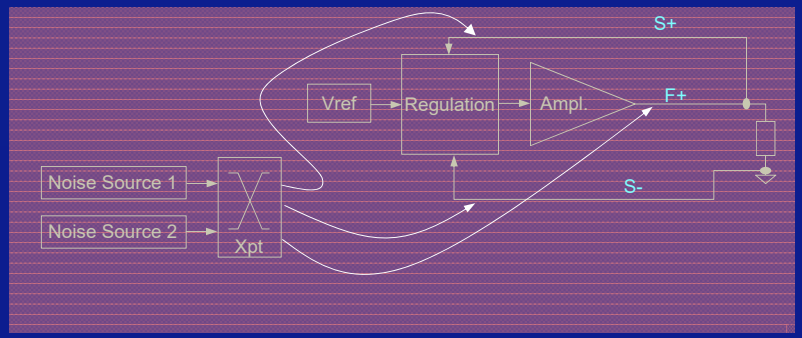
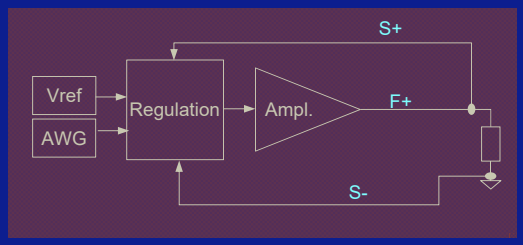
Technical Challenges to meet specification objectives

Power Supply Rejection Ratio

- Noise source option
  1. Independent source with switch matrix
  2. Per channel source
- Noise injection options
  1. SP coupling
  2. SM coupling
  3. F+ coupling





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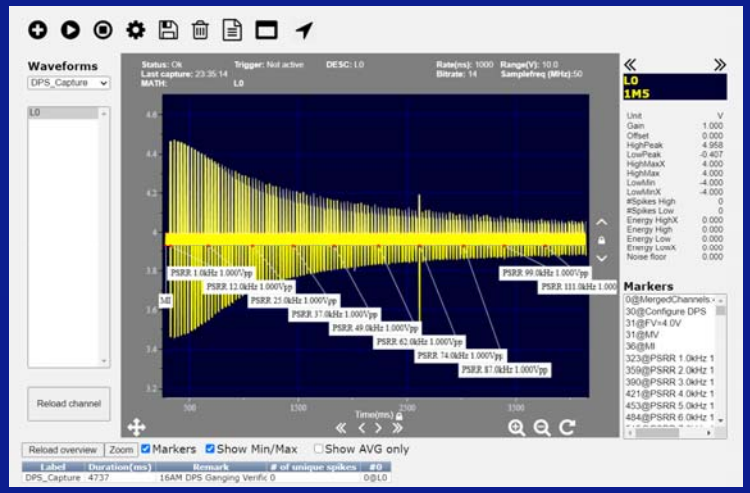
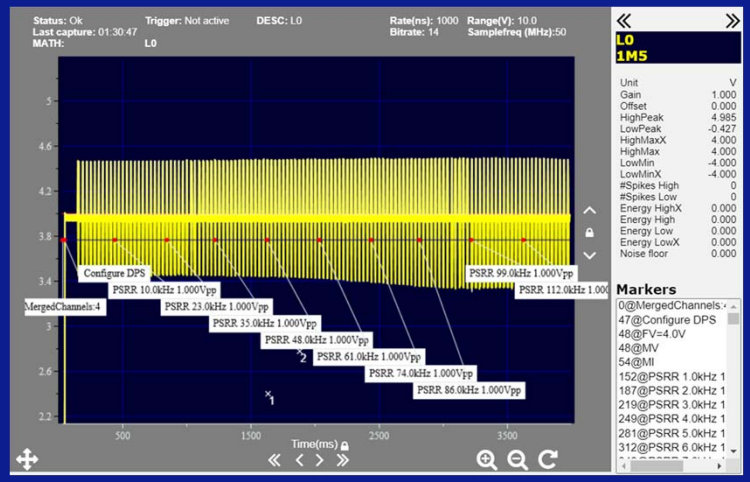
Technical Challenges to meet specification objectives

Power Supply Rejection Ratio

Retained solution is improvement of the Voltage reference transformed into AWG, characterize the path and proceed with correction table G=F(Freq)





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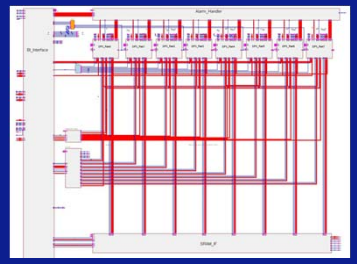
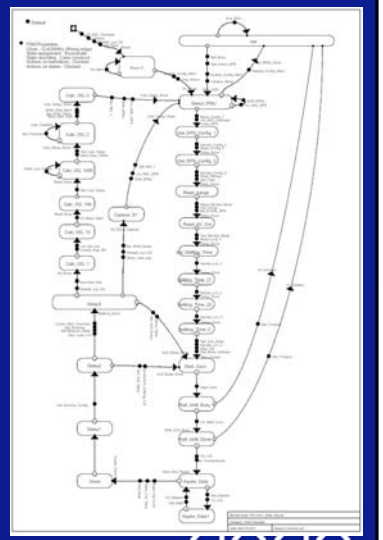
Technical Challenges to meet specification objectives

Parallel efficiency





Requirements for parallel processing

- No microcontroller on hardware
- Use FPGA with replicated State parallel state machine
- The FPGA's on HDPS128 performs many functions normally done in software:
- Forcing values, range settings, protection
- Measuring values, averaging
- Calibration, single/multi segment, range dependent
- Result processing pass/fail limit checks
- Tempco guarding/adjustments
- Failing DUT handling
- Each done in full parallel per DPS on one board and synced with multiple boards

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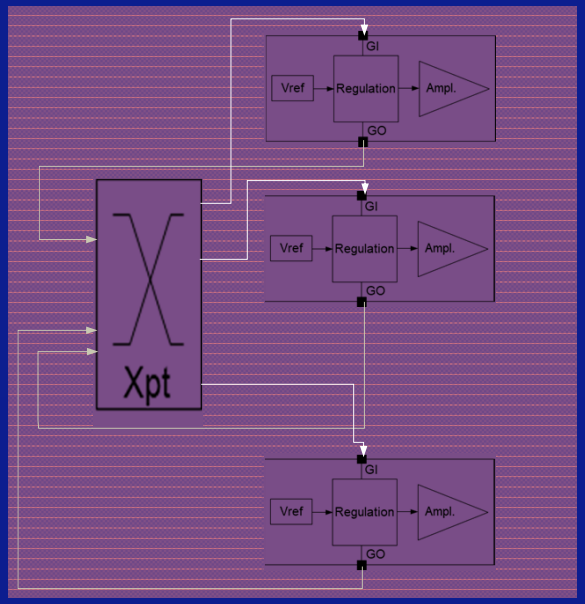
Technical Challenges to meet specification objectives

Gang capability

Original Design



Implemented solution

Measurements, dynamic behaviour, cost analysis has driven to a better compromise:

- 1 GO/GI every cluster of 4 channels
- Local 8x8 Crosspoint with 8 x 8, 500MHz
- Maximum 2 Xpoint level

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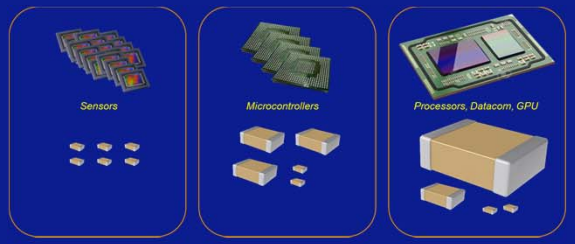
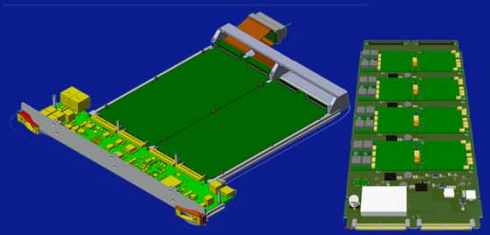
Moving Forward





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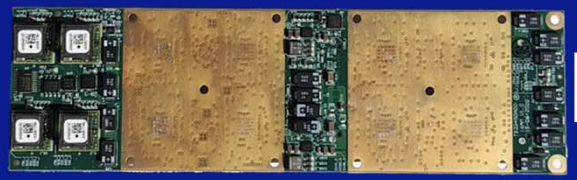
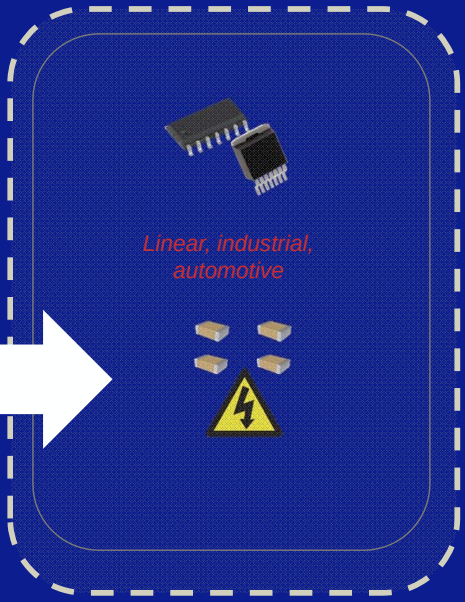


New “HV” VI module



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Summary & Closing

- Single DPS instrument that is scalable, flexible and gang-able from low to high power 1A to 128A per instrument.
- Instrument maintains dynamic performance in all configurations.
- FPGA flexibility for application specific requirements.
- Provides scale to enable high performance cost effective DUT power solutions.

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