Advantages and Opportunities with MEMS wafer level final test

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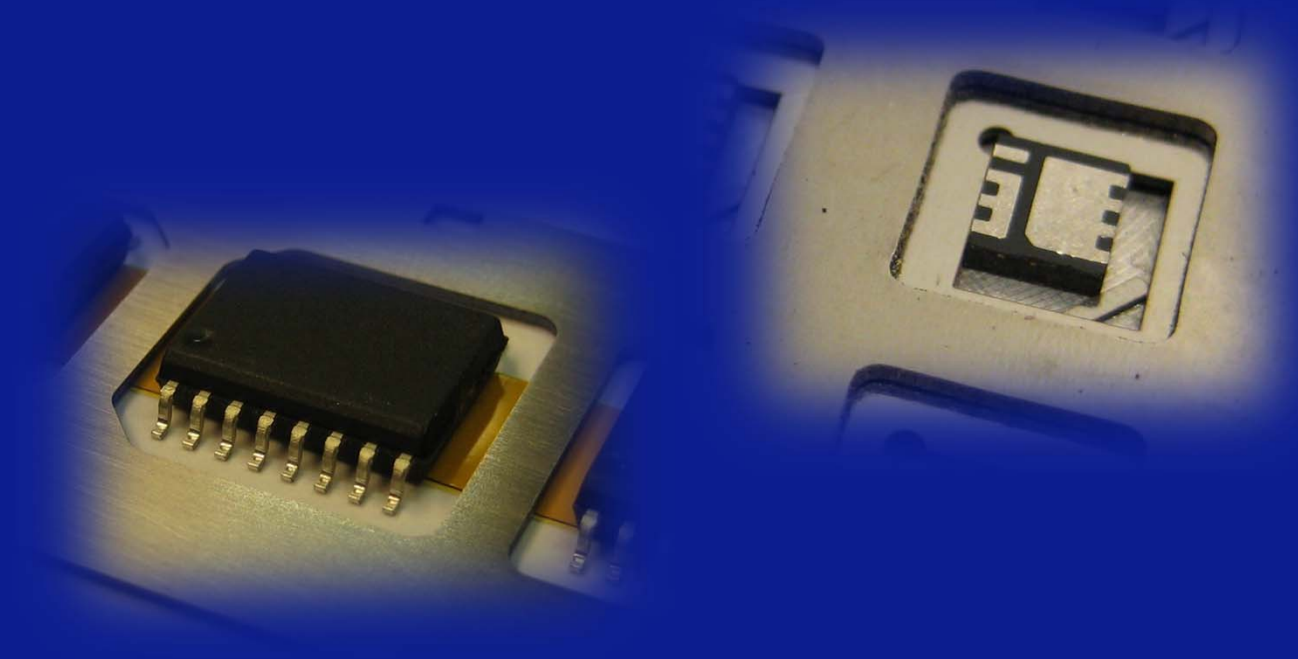
Contents

- Traditional MEMS packages
- Typical test / packaging flow
- Advanced package types
- Challenges and opportunities
- Solutions available today
- Conclusion

Traditional MEMS packages

- SOIC
- QFN
- LGA
- Metal cap



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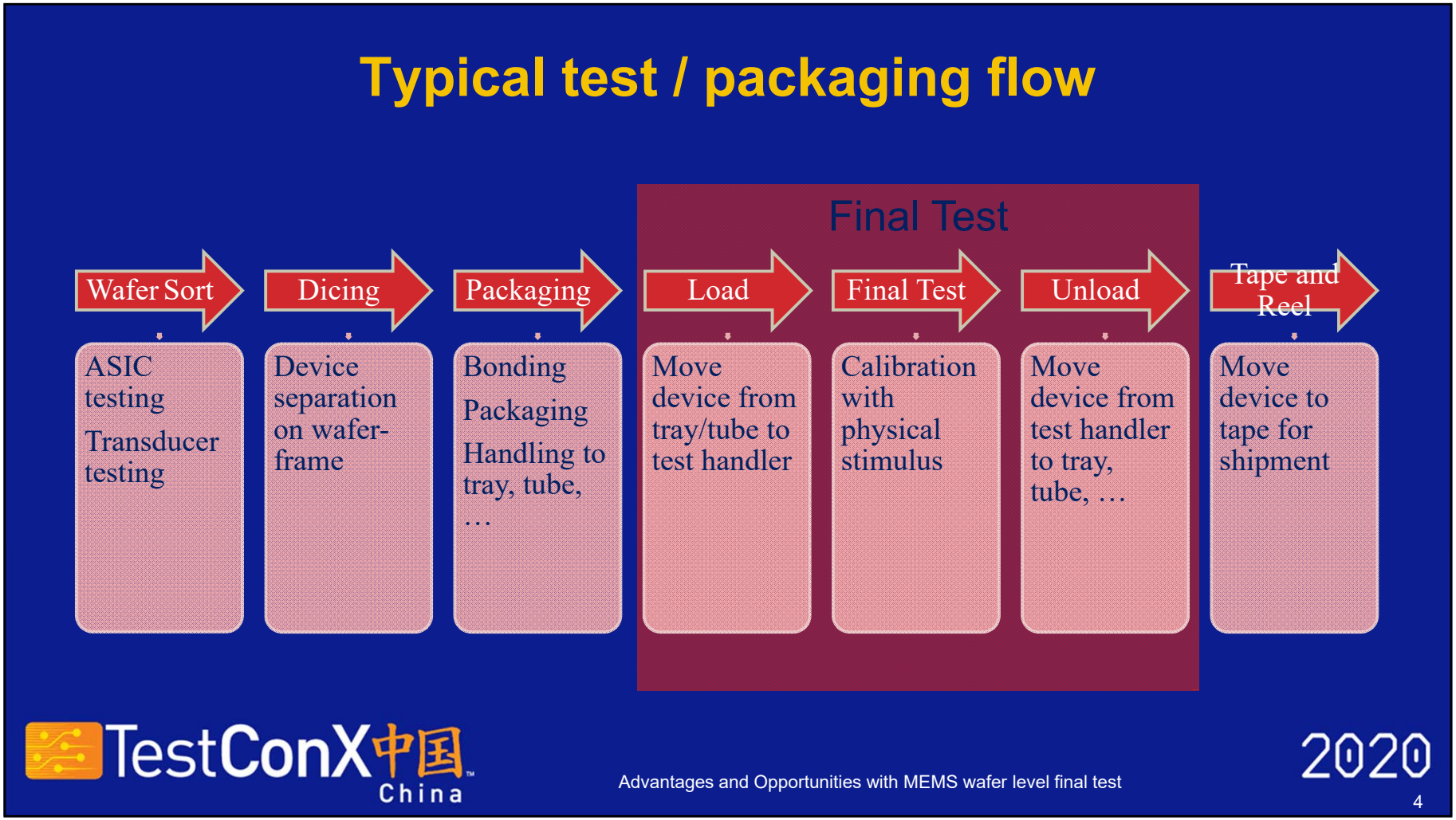
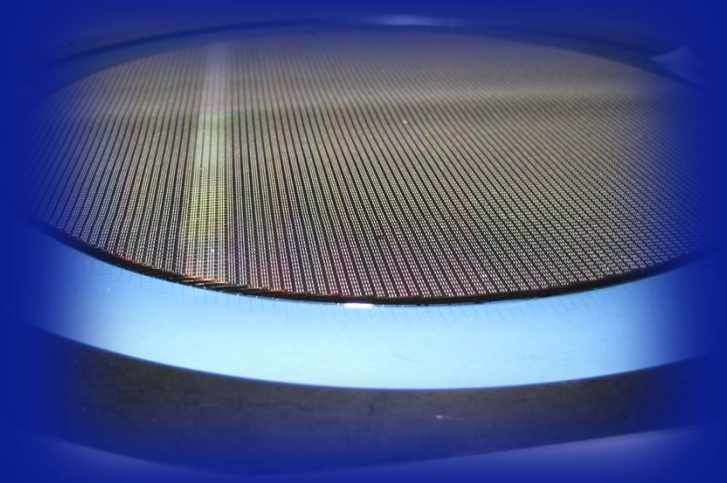


Advanced package types

- WLP – Wafer Level Package (FO-WLP, WLCSP, …)

- SiP – System in Package
- SoC – System on Chip



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5

Challenges and opportunities - WLP

- Size – often 1 x 1 mm or below
  - Difficult to handle separated devices properly
  - Mechanical alignment to stimulus (i. e. inertial sensors) and contacts challenging
- Low weight
  - Makes handling in trays difficult without additional support
- Fragility
  - Mechanical stress during conventional device test handling may cause damage to device

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- ASIC and sensor join at wafer level
  - Opportunity to combine three separate test steps to one

How to move forward

- Improve available technology to allow handling of smaller parts and reduce mechanical stress
  - Possible, but issues will return as dimensions continue to shrink
- Reduce number of process steps including device handling operations
  - Requires change to existing process flow
  - Offers potential to streamline operations

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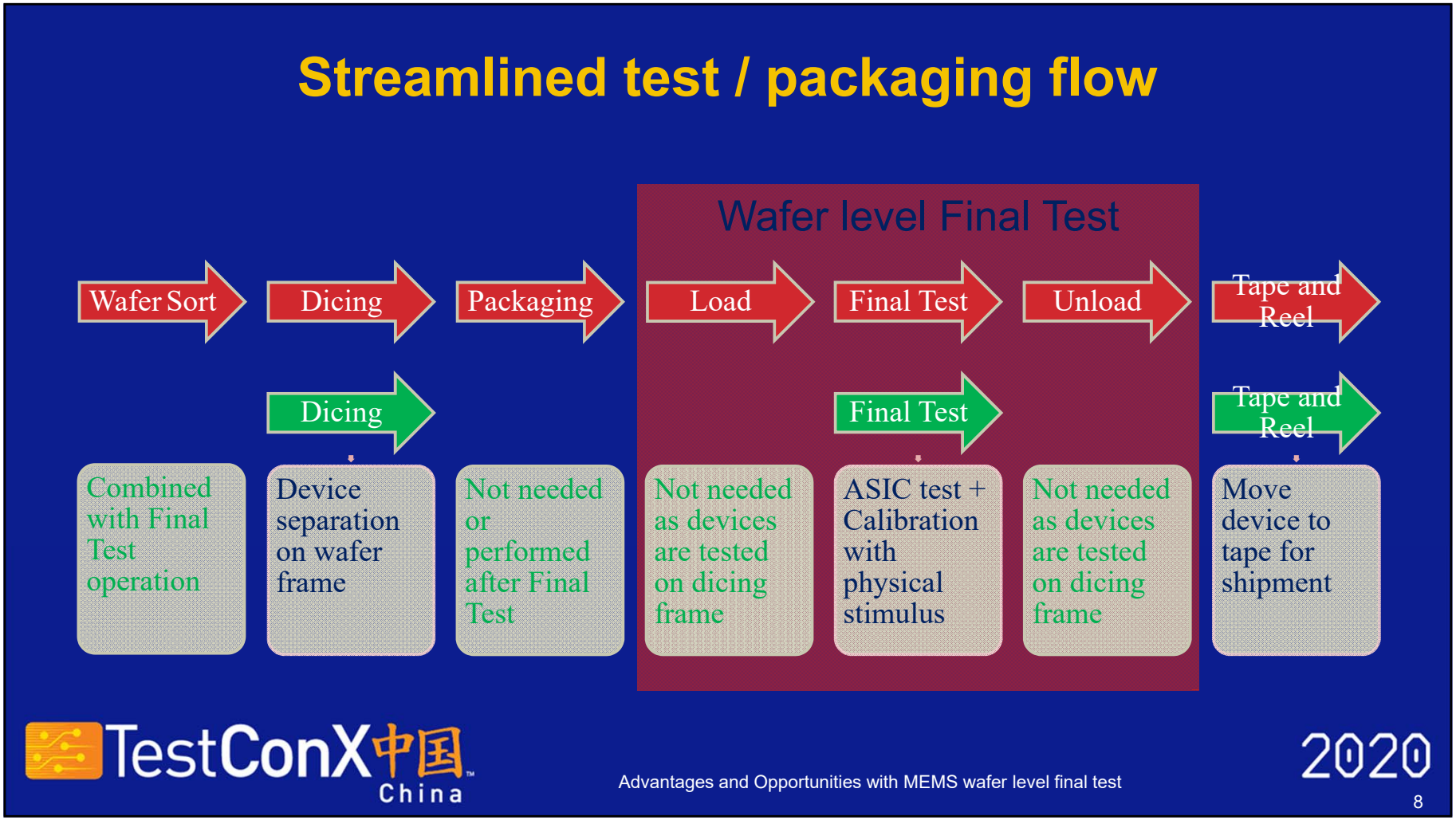

Advantages

- Elimination of several device handling and process steps
  - Reduced associated risks and yield losses
- Possibility to optimize test sequences as all components can be tested at once
  - Eliminate one sensor test step
  - Combine ASIC test with sensor test
- Reduced number of operator tasks
  - Less potential for error
  - Lower labor cost
- Reduction in floorspace

Challenges and opportunities- SIP / SOC

- Fragility of single components
  - Can cause components to fail due to handling stress
- System cost vs. sensor cost
  - Relatively cheap defective component can cause system to fail

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- Gives opportunity to optimize test flow depending on component cost and complexity

How to move forward

- Sensor test and calibration at system level
  - Risk of SoC / SiP failures due to sensor malfunction
- Known Good Die approach for sensor testing
  - Test sensors after dicing to ensure stress relieve before calibration
  - At wafer level on dicing frame to avoid unnecessary device handling
  - Potentially adding short sensor verification to system level test of SoC/SiP

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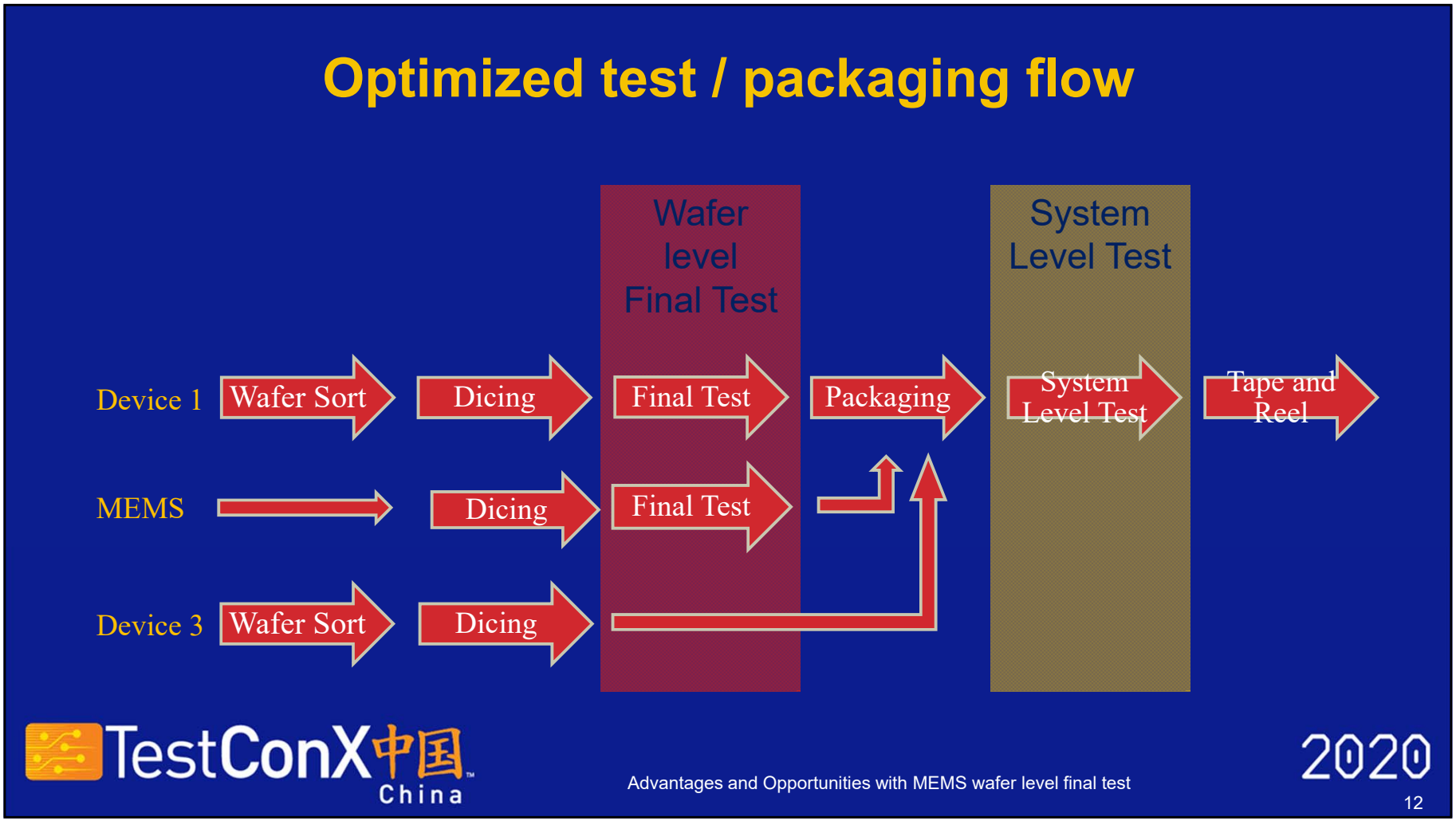

Advantages

Optimizing the process flow around test and packaging allows:

- Minimizing yield losses due to bad components at system level
- Best utilization of Known Good Die at system level
- Optimizing Cost of Test by minimizing test steps where possible

Solutions available today

- Probing of environmental sensors for
  - Pressure
  - Humidity
  - Gas concentration
  - …
- ➢ Using a production probe station with environmental chamber

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Solutions available today

- Probing of motion sensors like
  - Gyroscopes
  - Accelerometers
  - Magnetometers
  - Combinations
- ➢ Using a production probe station with motion stimulus capability

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15

Conclusion

- Overview to current MEMS final test handling strategies
- Challenges introduced with advanced packages

- Shown improved MEMS test handling strategies by
  - Combining wafer sort and final test for WLP
  - Replacement of wafer sort with wafer level final test for SiP/SoC

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