Bias-Stress Testing of Ultra High-Power Integrated Circuits: HTOL and ORM

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Virtual Event • May 11-13, 2020

Acronyms

- HTOL = High Temperature Operating Life
- ORM = Ongoing Reliability Monitoring
- BTI = Bias-Temperature Instability
- HCI = Hot Carrier Injection
- UHP = Ultra High-Power
- MCM = Multi-Chip Module
- FIT = Failures in 10^9 device hours

Introduction

Key Points.

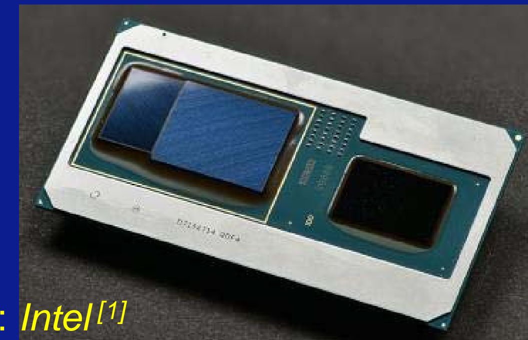
- Loss of 10-year reliability margin in FinFET silicon.
- HTOL stress levels are critical to assuring adequate activation of underlying aging mechanisms.
- Critical new role for ORM.

Ultra High-Power Integrated Circuits consume > 130A at JEDEC HTOL stress conditions (JESD22-A108).

- Tj = 135°C
- V_stress = 1.4x V_nom
- Dynamic toggling using functional test vectors

UHP ASIC Attributes

- Die sizes in the latest Si technologies have reached the constraint of the wafer mask reticle.
- Satellite die (Chiplets) are being added to the package, creating SiP (System in Package) products that challenge the equipment capabilities and test methodologies for new product qualification.



Source: *Intel* [1]

Leakage Power at Stress Conditions

- IC leakage power increases exponentially with temperature.
- Large monolithic die assembled in MCM and 2.5D packaging, comprise leakage power at HTOL stress conditions that consumes or exceeds the power capability of traditional HTOL systems.

Source: [9]

Dynamic Power at Stress Conditions

- Dynamic power from functional stress patterns adds further to the power delivery challenge for biased-life reliability testing (HTOL).

Source: *[9]*

Key challenges and considerations for biased-life stress testing for ultra high-power IC products.

- HTOL for new product qualification.
- HTOL for ongoing reliability monitoring (ORM).
- Latest IC packaging (MCM, 2.5D) and silicon (FinFET) technology.
- Reliability modeling.

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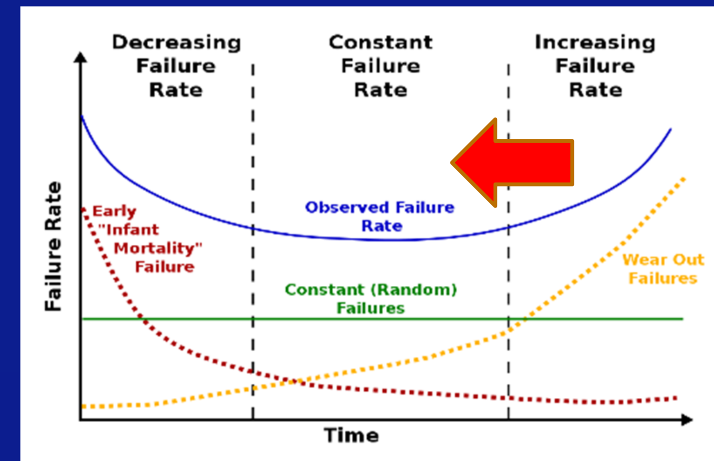
Challenges

- High power is a key challenge to biased qualification testing.
- Loss of lifetime margin.
  - Notably, electromigration, T_{DDB} and transistor aging mechanisms.
- Reduction of thermo-mechanical tolerances.
  - Si / Packaging stress interactions



Source: [8]

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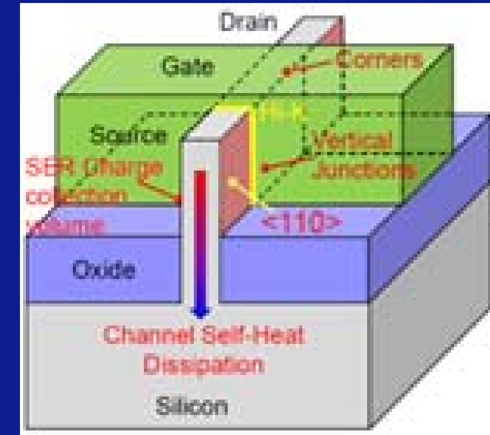
Key FinFET Aging Mechanisms

- BTI / HCI Vt instability.
  - <110> orientation is more susceptible to trap generation; NBTI worse, PBTI is more robust [2,3].
- FinFET self-heat.
  - Cross-sectional area for heat flow to Si is less than with PlanarFET.
  - Multiple fins exhibit thermal gradient; Central fins can be up to 50% hotter than adjacent fins[4].

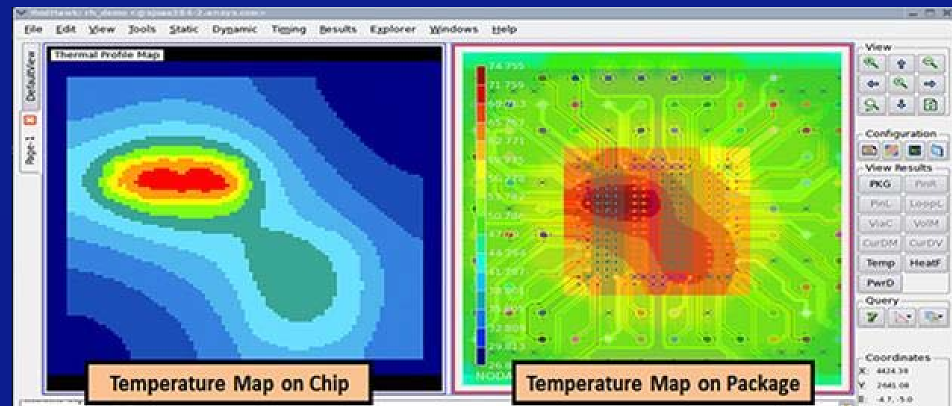


Source: [8]

Key Issue with UHP Devices

- Global thermal gradient: exacerbates local FET heating.
- Electromigration lifetime has significantly less margin[5,6].
- For 7nm, Tj_max for 10-year lifetime has been reduced (industry-wide) from 115ºC to 105ºC .

➢ This may not be enough.



Source: *ANSYS* [7]

The Issue

- This reliability margin erosion has a bearing on how much stress is required to:
  1. Demonstrate and predict reliability at product use conditions (qualification), and
  2. Monitor reliability variance over a product's production life cycle.

One can no longer be satisfied with short duration stress, or reduced stress.

An HTOL qualification plan must preserve stress levels so that stress duration can be a reasonable indicator of reliability and lifetime at use conditions.

- IC products of the type referred to here typically have the expectation of 10-year lifetime.

The trend in the industry has been to compromise on stress conditions for high power ICs, ostensibly due to power constraints of the HTOL system and overall cost of qualification, by:

- Reducing Tj_stress.
- Reducing V_stress.
- Reducing the frequency of functional stress vectors and DFT-delivered stimulus.
- Running stress patterns sequentially, allowing some circuits to be idle while other circuits are toggled.

Consequences for HTOL

When stress temperature (Tj) is reduced, to reduce leakage and dynamic power…

- Thermal activation of thermally-activated reliability mechanisms is reduced by ~2x for every 10-degree reduction (assumes 0.7eV).
- A stress configured to demonstrate 10-year lifetime, only demonstrates 5 years when Tj is reduced by 10°C.

-10°C → 2x → 5 years

Consequences for HTOL

When stress voltage (Vdd) is reduced, again, to contain power…

- Voltage acceleration is reduced by ~3x (assumes a gamma factor of 15 V^{-1}). A stress configured to demonstrate 10-year lifetime only demonstrates 3.5 years when Vdd is reduced by 10%.

-10% → 3x → 3.5 years

Compensating for the reduced acceleration factors by extending the duration of a 1,000 hr HTOL is not practical.

- For the stress reductions used above, a 1,000 hr stress plan would have to be increased to over 6,000 hrs, for 10-year equivalency.

Expensive because of tying up equipment and delaying product launch.

1000 hrs → 6000 hrs

Ongoing Reliability Monitoring

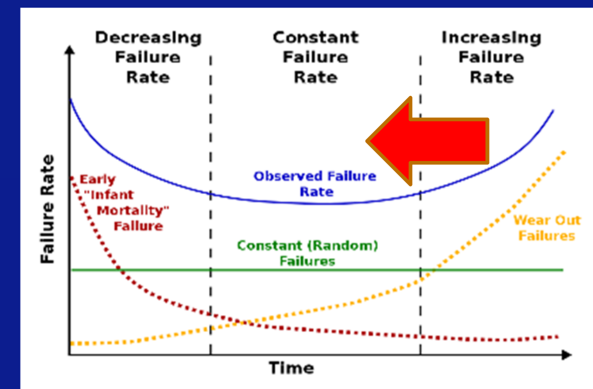
- ORM over an ASIC's production manufacturing life cycle is the allocation of randomly selected production parts to reliability testing, with regular (usually quarterly) reporting.
- ORM today does not assess wear-out reliability margin. Instead it reveals latent defects not activated and screened by production test

Considerations for ORM

- When wear-out / aging failure modes have greater than 10-year lifetime margin, ORM is not expected to be a demonstration of lifetime or assessment of lifetime variability.

Considerations for ORM

- UHP ASIC products using latest Si technology have consumed this reliability lifetime margin to the point where previously tolerated manufacturing variances can now manifest as lifetime limiters within the 10-year expectation.



Considerations for ORM

- This reliability margin erosion has the concerning consequence that manufacturing process variances (eg Si buildup layer variances and packaging tolerances) that once had lifetime margin, no longer enjoy that margin and can manifest as early wear-out and/or increased FIT during the product lifetime.

Considerations for ORM

- In the face of reliability margin erosion, ORM takes on a ***critical new role***…
  1. To demonstrate that manufacturing variances are not producing a compromised reliability population of product in the field, and
  2. To identify trends and the underlying mechanisms for process control feedback.

Considerations for ORM

- **Small Part Quantity:** Since Manufacturing and materials variances are systemic, and not random defects, a small part quantity for ORM is judged to be sufficient.
- **Stress Duration / Level / Coverage:** Instead of part quantity being paramount, stress duration (hours in stress) stress level (thermal and voltage stress) and stress coverage (at-speed pattern coverage) have become key factors.
- **A single 1,000-hr Read Point:** Since ORM is not a product qualification, but instead a reliability monitor, ORM does not require multiple ATE read points. A single read point can suffice for defect and wear-out monitoring.

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A solution for UHP ICs

An HTOL system with the following design attributes is required to reach and safely sustain the HTOL / ORM voltage and temperature stress levels and functional coverage required for effective acceleration.

- Eliminate the back plane and provide per-DUT test resources, to preserve stress pattern signal integrity at high frequency.
- Locate power supplies at the DUT to mitigate voltage droop.
- Provide sufficient memory depth for large stress patterns.
- Support high frequency stress patterns.
- Per-DUT integrated fast-response cooling block.

Takeaways

High power ICs require a high power HTOL and ORM solution.

Previously tolerated manufacturing variances can now manifest as lifetime limiters within the 10-year life expectation.

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