Implementation of WL-HTOL for Early Reliability Assessments

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Acronyms

- WLBI – Wafer Level Burn-In
- RT – Room Temperature
- HT – High Temperature
- HVS – High Voltage Screen
- DVS – Dynamic Voltage Screen
- ELFR – Early Life Failure Rate
- HTOL- High Temperature Operating Life
- WL – Wafer Level & PL – Package Level
- ERA – Early Reliability Assessment
- HF - Hard Fail, SF - Soft Fail
- DOE – Design of Experiments
- CPI – Chip to Package Interaction
- RO – Readout (pre/post) test
- AQL – Acceptance Quality Level
- LPTD – Lot Percentile Tolerance Disposition
- CCS – Constant Current Stress
- CVS – Constant Voltage Stress

Abstract

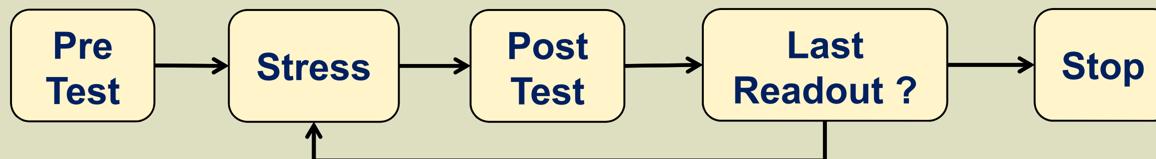
- Industry standard BI and HTOL are done on package level.
- New Scheme: Wafer Level full functional stress for BI & ELFR:
  - At high temperature and voltages.
  - Saves Time: 6~8 weeks;
  - Huge Cost savings: BIBs w/o full WLBI Systems.
- This concept can be used where faster feedback is needed:
  - Early Reliability Assessments on circuits / products
    - For Process changes and New Product Introductions (NPI's)
  - For Process DOE's, Kinetic studies and HVS/DVS etc.,
    - During product/process development.

Purpose

- Reliability qualification need package stresses. e.g. ELFR, HTOL
  - Long setup times & costs: Bumping – bump masks.
  - Packaging: Substrate Design, tooling: 12~15 weeks.
- WLBI Systems: High costs & long design time 6-9 months.
- **New scheme:** Done at wafer level, full circuit functional stress.
- Implemented with high temp. probe cards and existing tester/s.
- Stress to meet early qualification needs: done in @2-3 weeks.
- Reduces high costs of BIBs, WLBI systems & long lead times.

Methodology: WL HT Stress

- New wafer level functional scheme is executed using:
  - Multi-site probe cards for test & stress.
  - At elevated stress voltage and Temperatures.
  - For pre-determined stress durations.
- **Generic Flow**: Same as package level stress.



- This new scheme can be implemented by:
  - Using 1 or 2 multi-site probe cards and tester/s.
  - Test & stress hardware should be high temperature tolerant.

Execution Flow and Types

Flow types depends on Testers & Probe Card's availability:

Stress & Measure in Sequence (SMS): One Tester

- One probe card sufficient but two better.

One Stress One Measure (1S1M): Need two testers.

- One test & one stress in parallel: w/ 2 probe cards.

One Stress, One Measure per Temp (1S1MT): Need >2 testers.

- Different temps. tests & stressing in parallel
- ≥ 2 probe cards needed for faster throughput.

Test & Stress Optimization

Test & Stress optimization factors:

- Depends on type of flow & rotation.
- Bandwidth allocated for:
  - Number of Testers and
  - Number of Probe Cards
- Minimize stabilization time, before start of temperature tests.
- Minimize test temperature change time: for >2 temperatures.
- Maximum throughput.

Prior Requirements

Before full implementation of the scheme:

- A correlation study to be run
  - Wafer level and Package level.
  - To compare, correlate & validate results.
- Statistically significant equal number of parts for legs.
  - Standard LPTD or AQL tables can be used.
- Die locations: from all zones & across wafer.
- Dies from >3 wafers: wafer-to-wafer variability.
- Wafers from >1 lot: lot-to-lot variability.

Checks & Guidelines

- Probe cards suitability at high temp. continuous stress.
- Use same set of parametric and functional tests as BI.
- Same stress: voltage, temperature & speed etc.
- If IR drop & self heating issues exists:
  - Stress Voltage & Temp. levels to be adjusted.
- When used for DVS/HVS and burn-in:
  - Set adequate levels of voltage & temperature.
  - Validate with stress results after screens.

Experiment 1: Wafer Vs Package Level Study

- Split runs on two legs of stress planned:
  - Package level and Wafer level.
  - At high temperature & voltage stress.
  - Equal & statistically significant number of parts

- The two legs were run upto 48hrs with:
  - Same temperatures for test and stress.
  - *Same voltage & temperature for stress.
  - Same or equivalent stress durations.

*Stress voltage and junction temperature on both legs are made equivalent by using same overall acceleration factor.

Test Results Comparison:

The wafer level and package level stress results are compared:

- Total # of fails at T48 compared for both legs.

Stress Duration	# of fails on Package level Burn-In	# of fails on Wafer level HT stress test
4hrs	3HF+1SF	2HF+2SF
8hrs	1HF+2SF	2HF+1SF
12hrs	2SF	1SF
24hrs	1SF	1SF
48hrs	-	1SF
Total Fails	4HF+6SFs	4HF+6SF's

- HF is hard fail and SF is soft fail.

Package Level Results Analysis

- Package level stress test results are plotted:

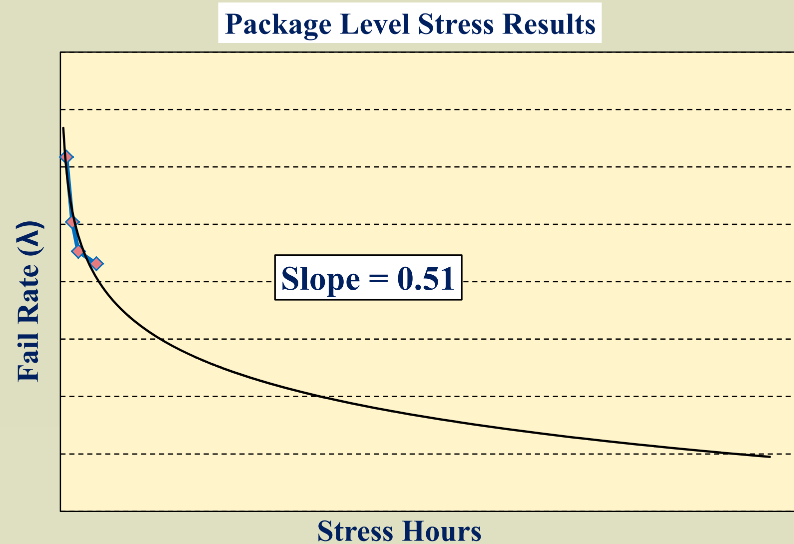


Fig-1:Package Level Stress Data

- Analysis shows slope of Fail Rate curve is @0.51

Wafer Level Results Analysis

- Wafer Level stress test results are plotted:

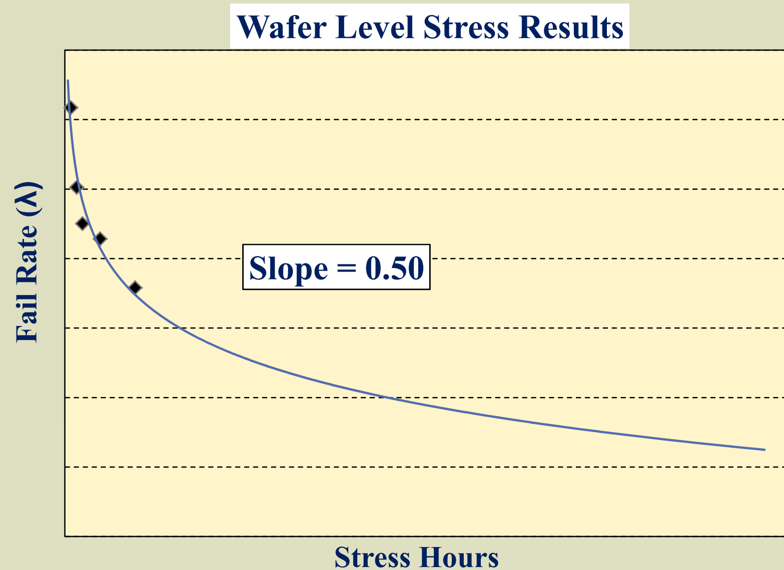


Fig-2: Wafer Level Stress Data

- Analysis shows slope of Fail Rate curve is @0.50

Experiment-2: HVS/DVS DOE's

- The wafer level test concept was used for
  - DOE's for HVS / DVS screen studies.
- To compare and optimize for
  - Suitable stress levels (voltage & Temp.)
  - Stress duration and conditions.
- To validate effectiveness of wafer level screens
  - By Wei-bull curve slopes of the failures.
  - Comparison of other statistical parameters.

HVS DOE Study Results:

1st HVS DOE study done:
- During early process development stage.
- Wafer level high voltage screen (HVS) stress.
- Different stress durations: 2,4,6,8 secs.
- At fixed stress voltage.

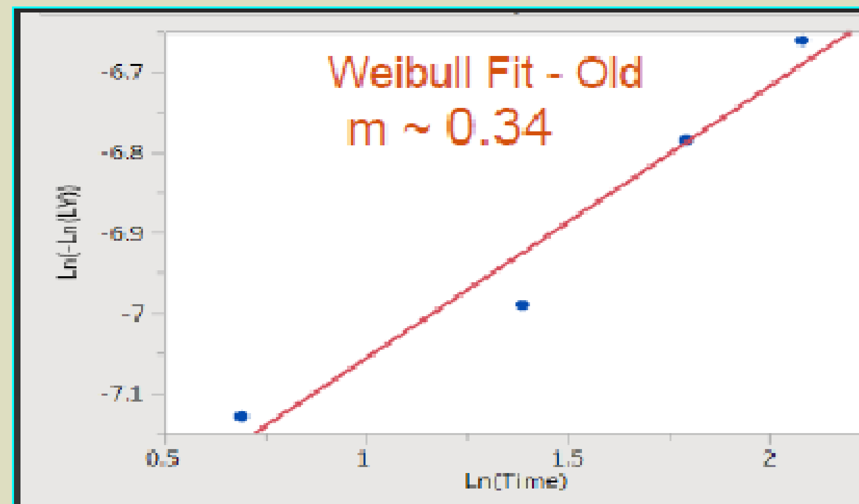


Fig-1: HVS Weibull: Early Study

Analysis: Weibull slope on fails Vs time was ~0.34
- Indicating there is still room for improvement on screens.

Study Results: Process Improved

Experiment repeated with:

- Wafer level stress
- Same process different stage
- Same stress as before on:
    - Voltage
    - Temperature
    - Durations.
- To assess the improvement.

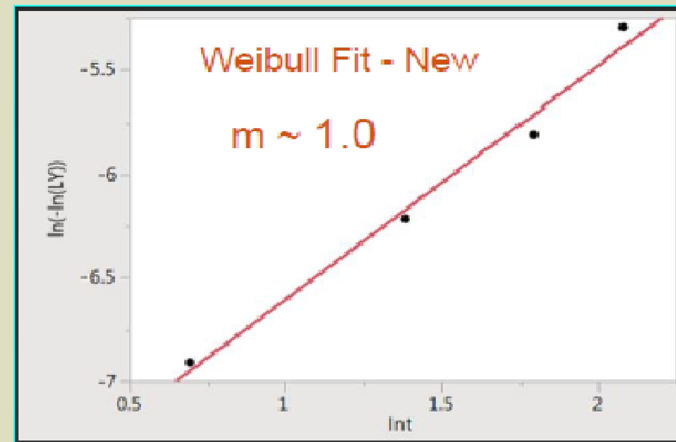


Fig-2: HVS Weibull - Improved

- The Weibull slope is improved to ~1.0 from earlier round.
- Also indicates that the HVS screen is more effective.

Cost & Cycle Time Savings

Various advantages of this method are:

- Demonstrated on different experiments done.
- Implemented on multiple technology nodes.
- As a replacement for package level BI & Screens.
- At different stages of process and
- Product's maturity stages.

The application purpose, probe card types, cycle time (CT) and cost savings Vs package level burn-in are listed.
All the details are compared to estimate cost Savings ➔

Projects Implemented & Cost Savings

Cost savings from different projects implemented w.r.t package level are:

Tech. Node	Test Chip & Purpose	#of PC sites	Stress Details	Cycle Time Days	Relative savings % to BI
1	SRAM ERA	4	Tj:125C 24h+24h	7	42%
2	eFuse Qual CCS & CVS	25	@85C, 36h+36h	12	51%
	SRAM ERA	9	Tj:125C, 24h+24h	9	54%
3	SRAM ERA	4	Tj:125C, 24h+24h	12	48%
	SRAM HVS DOE	4	25-85C, 24h+RO	12	46%

- Average of @50% cost savings achieved with this WL stress scheme.

Cycle Time Savings

Cycle time comparison: Package Vs Wafer Level

Conventional Package Level Burn-In Flow (at Module Level)	Typical TAT		Wafer Level Burn-In Flow (at wafer probe)	Typical TAT
Fabout Sort & Data Review	3 days		Fabout Sort & Data Review	3 days
Ship to Bump House	4 days		Receive & Queue for tester	0.5days
Bumping, Post Bump Sort/HVS	7 days		Setup Tester & Stabilize at HT	0.5 days
Sort review, Wfr slection+OQA	2 days			
Ship to Assembly House	4 days			
Packaging TAT at Assembly for FC	21 days			
Ship to Test House/Lab	4 days			
Handler/Tester setup FT@3Temps	3 days		T0 FT at 3 Temperatures	2 days
Load, Run 24hrs & Unload	2 days		Load, Run 24hrs & Unload	1 day
T24 FT at 3 temperatures	3 days		T24 FT at 3 temperatures	2 days
Load, Ramp & Run 24hrs & Unload	2 days		Load, Ramp & Run 24hrs & Unload	1 days
T48 FT at 3 temperatures	3 days		T48 FT at 3 temperatures	2 days
Verifications & Report	2 days		Verifications & Report	2 days
Converntional Burn-In TAT	**60 days**		**Fast Wafer Burn-In TAT**	**14 days**

- Gain of @6~7 weeks using WLHT Scheme.
- Very useful during process development stage.
- Faster feedback to process changes or improvements.

Advantages

- Enables fast, in fab (EOL) or at Test Lab execution.
- Circuit level quick functional assessments.
- Fast to setup with existing infrastructure
- Lower costs and lead-time Vs to commercial WLBI.
  - Unlike WLBI, uses lower cost probe cards.
  - That can be acquired in shorter time
  - Use of existing infrastructure for probe card repair.
- Limited test development with fast turnaround time.
  - WLBI need longer design time & 1-2 months.
- Enables usage of existing Fab database and
- Existing data analysis tools can be used.

Limitations

Longer stress times & larger part counts call for:

- Tester/s dedication and bandwidth [6].
- Probe cards with high temperature design.
- Swapping between stress and test modes.
  - if single tester used, increased total time.
- Stress might limit to 12hrs or 24hrs intervals.
  - Readout at 12 and 24hrs & continue.
- Prior understanding of Chip Package Interaction (CPI) on fails necessary Vs module burn-in.

Conclusion

- Simple wafer level high temp. stress concept.
- For functional & product stress – w/o full fledged WLBI
- Implemented and experimentally validated.
- Results correlated with conventional package burn-in.
  - For smaller stress hours: ELFR & screens.
- Limitation on longer stress hours >168hrs for HTOL.
  - By design of high temperature probe cards.
- This scheme enables:
  - Shorter learning cycles faster feedback.
  - HVS / DVS screen and kinetic studies.
  - Quick functional reliability assessments.

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